Power Electronics

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Lecture - 37

Power Switch Protection- Snubbers

So, last class we talked about the effect of switching delays that is dead time effect on the inverter output voltage. Then we found that the dead times are introduced to protect the devices and for a PWM operation, because of the dead time, it will introduce a square wave voltage depending on the current direction and it will affect the output modulation index. So, even though the dead time is introduced for the protection of the device, it has a negative effect on the output voltage and how to correct it, we studied last time.

Now, so for we have assumed that the switching transitions switch on, turn on and turn off are instantaneous and the device can take across it any dv by dt voltage rise across it and any current rise di by dt through the device. But for many applications a practical device a semi conductor device will have a limited dv by dt and di by dt. So, how to protect this device during or against this one that is switch protection? Here we will use for switch protection, the whole snubbers and how to design the snubbers; we will talk about that one.

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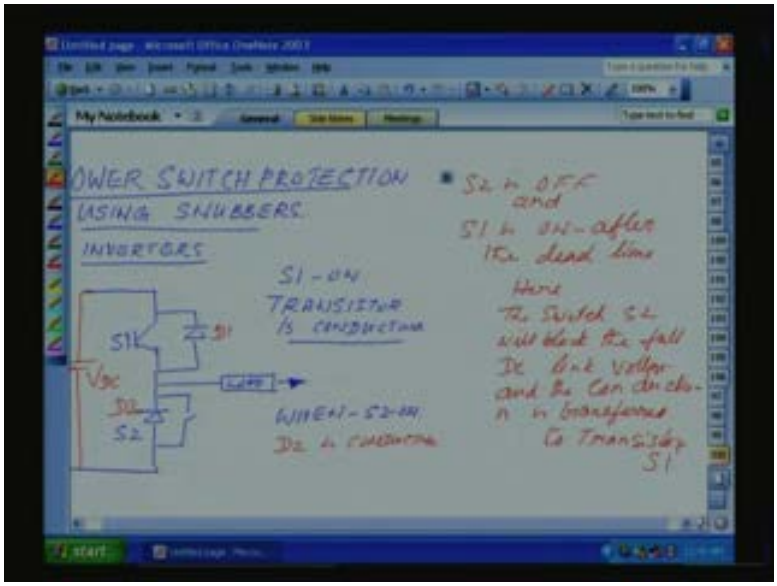

So, the next, the title of this today's lecture is Power switch protection, power switch protection using snubbers. Let us talk about our inverter; we will talk about in the context of dc invertors, the switch protection. Now-a-days because of the advances in the semi conductor technology, we get integrated modules where the device can take care of, it is

packaged such a way it can take of high dv by dt high di by dt. But when we use individual ah devices for a sub device application or for any switching function, we have to … that device that means we have to operate the device such a way that device is operated with in its dv by dt and di by dt limit.

So, what is this problem? Let us analyse that one, let us take the first limb of an inverter; I will represent the switch as a transistor and this is the diode and we have put the diode so that the switch can conduct in both directions, both direction depending on the load current. But the positive, the positive and the negative voltage at the output, we are generating by switching the devices, top switch and the bottom device that is S_1 and S_2 device. But whether the transistor to conduct or the diode to conduct, that depends on the load.

Let us take the current is in this direction. In this conduction, when S_1 is on, when S_1 is on, transistor will be conducting, transistor is conducting when S_2 on, S_2 on means we are giving gate pulse to S_2 but because of the current direction here, D_2 will be conducting; not the transistor. Here, D_2 will be conducting; here instead of the transistor, D_2 is conducting.

When D_2 is conducting, S_1 is off and S_1 has to support the full DC link voltage, V_{DC}. Let us take a condition where we are going from S_2 to S_1. Now, D_2 is conducting and S_2 is switched off. Now, the condition is S_2 is off and S_1 is on; after the dead time td, I will say after the dead time. Now, what happens? It will take a finite time for the or now S_2 is off and S_1 is after the dead time, so what happens? Diode will be switched on instantaneously and S_1 will start conducting.

So now, here the switch S_2 will block the full DC link voltage and the conduction is transferred to transistor S_1, S_1. Now, let us take the condition when the conduction is transferring from S_1 to S_2.

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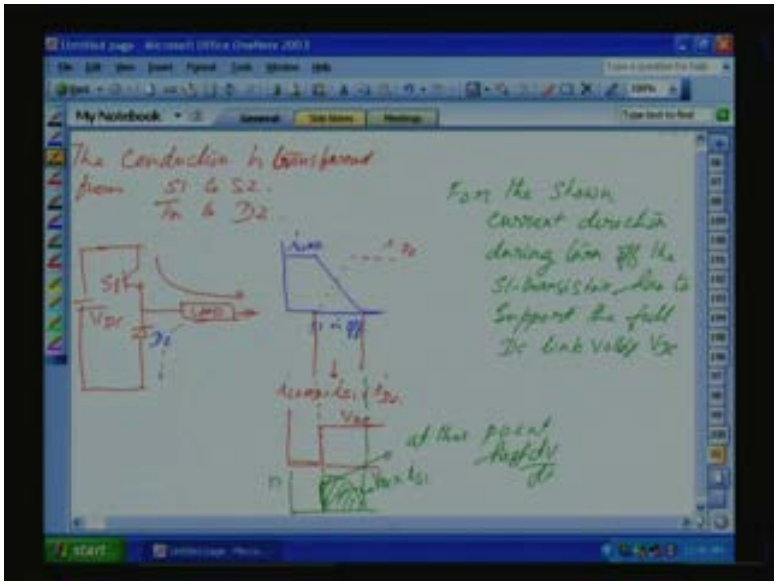

Now, let us take the condition; the conduction is transferred from S_1 to S_2 that means transistor to D_2. So, let us draw only the transistor and the diode. Now, this is our V_{DC}, this is the load. Now, current direction is in this direction, the moment S_1 is off that means let us

take till this point, S_1 is on that means full load current is passing through, this is high load, passing through the transistor S_1. Now here, S_2 is on or S_1 is off; see S_1 is off, here the S_2 on or off is getting affected because diode is conducting, D_2 is conducting. So, moment S_1 is off, what will happen? S_1 is going to switch off that means current will slowly decrease and come to zero. Why?

The moment current is slowly decreasing; current through the D_2 will slowly increase. So, current through D_2 that is iD_2 will slowly increase such that during this period, i load is equal to equal to i_{S1} plus to iD_2. Now here, the current is decreasing, here the current is increasing; but the moment the diode is turned on, the voltage drop across the diode is approximately 0.7 volts. Now, S_1 has to support the full V_{CE}. So, if you see here, the V_{CE} voltage at this point, the voltage across S_1 is V_{CE} till this point, it was only saturation voltage and suddenly here the voltage will go to V_CE that is V_{DC}, this is V_{DC} because diode is conducting, diode voltage is only 0.7 and during the switch off process, S_1 has to support the full DC voltage that is during turn off, for the present current direction, for the present current direction, we will write it, we will bring that; for the shown current direction, direction during turn off, the S_1 transistor has to support the full DC link voltage V_{DC}.

So, what happens? There is a current through the device and the voltage across it, so if you see the power loss during this period that is power during this period, till the switch off is completed, heavy power loss will be there. So, this will be approximately, we can multiply, this will be equal to V_{DC} into i_{S1}. So PWM operation, this happens at every triangular frequency, carrier interval. So, heavy power loss will be there and sometimes it can lead to device breakdown.

So, how to protect the device? Here if you see, the dv by dt is instantaneous, it is slighting high dv by dt; at this point, at this point, the transistor will have high dv by dt and also power loss. So, how to avoid this one? The best way to avoid this one; we should not allow the voltage V_{CE} to rise very fast, we want the V_{CE} to rise very slowly till the turn off is completed. So, what is the best way? Slowly raising during turn off process put a capacitor that means we will put a capacitor across it. We will go to the next page.

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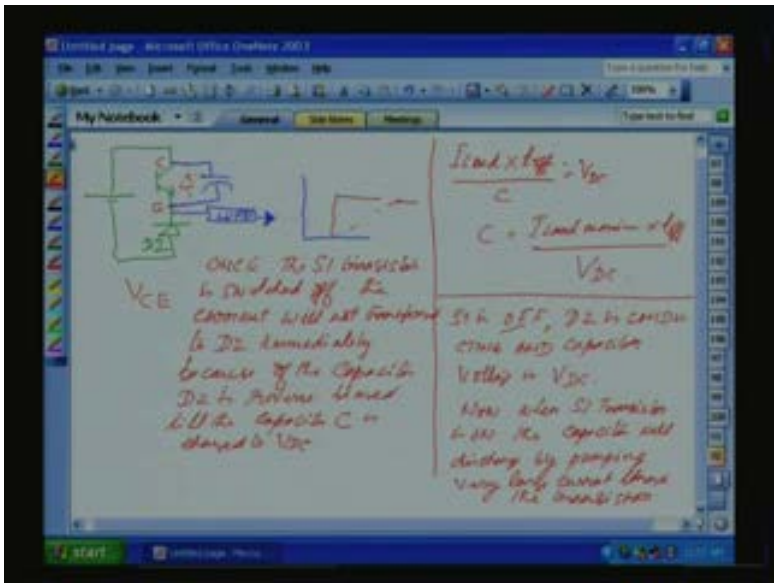

See here again, this is our V_{DC}, this our transistor, then this is our D_2, D_2, there is a diode there, that diode is not coming into picture now; diode is there that we are not talking about the diode. So, to protect the device, protect the device during this turn off period; this is load, current direction is like this, we will put a capacitor across this one so that when the transistor is conducting, the voltage across the transistor is 0, the voltage across the capacitor is 0. The moment turn off process starts, what happen? The V_C will instead of going immediately like this that is instead of V_C going quickly to V_{DC} like this, V_C will slowly go, during this portion it will slowly rise and comes to V_{DC} because of the capacitor. Why?

Assume S_1 the transistor is turned off and the current is coming through D_2. The moment current is coming through D_2, what will happen? The full V_C has to come across the V_C has to come across the transistor. So, because of the capacitor, the full V_{DC} will not come across the transistor now because the current has to pass through this capacitor and charge the capacitor.

So let us say, the transistor is switched off and the current is, now the current is transferred to to the capacitor. So, what happens here? The V_C, the V_{CE} will slowly rise, V_{CE}. So, what is V_{CE}? During the turn off process, V_{CE} is equal to assuming load is highly inductive so that the diode current and the capacitor current, somehow the diode current and capacitor current are equal to load current and the current through in the capacitor is slowly raising. But for our analysis, let us say the current is, the moment it is switched off, slowly the transistor will the transistor current will slowly decrease.

But the problem compared to the previous case, immediately current will not be transferred to the diode. That means once the S_1 transistor is switched off, the current will not be transferred to D_2 immediately because of the capacitor. Why? See, the capacitor voltage is 0 and diode will not conduct immediately because the transistor voltage or across the transistor voltage, the capacitor is not charged, capacitor voltage is 0 and diode is still reverse biased. So, the diode will be forward biased when this DC link voltage is supported by or opposed by the capacitor. So, during turn off, when transistor is immediately turned off, D_2 is reversed biased till the capacitor C is charged to V_{DC}.

Now, what happens? Transistor is turned on, slowly turning on, turning off and here the transistor current will be instead of transferring to diode, it will transfer to capacitor. Let us say, this transfer is immediate, transistor is switched on immediately; so immediately switched off without appearing the full DC across the CE. Now, till the capacitor is charged to full V_{DC}, the diode D_2 will not conduct; till that point the diode D_2 will be switched off, reversed biased. So, how to design the capacitor?

Let us say, the load current is highly inductive and during this transfer process, the current through the capacitor is nearly constant. So, capacitor will be charged with or we can assume the capacitor will be charged with a constant current. So, if you see here, so during this turn off process that is during when the current transfer to transistor to capacitor, approximate design we can say, the V_C or the voltage across the capacitor is equal to capacitor charge is the I_{load}, the capacitor charging voltage is equal to I_{load} into during the turn off process, so let us say T_L turn off time, so we will say t_{off} for a transistor; I_{load} into t_{off} by C will be equal to V_{DC}. So, that means current is transferred to the capacitor, we will assume for the design of the capacitor, first case design the full load current is passing through the capacitor and during the turn off period I_{load} into t_{off} by C is equal to V_{DC}.

For any device, there is a minimal turn off time will be there. So, during the turn off period, we will assume the capacitor is not immediately coming; it is slowly coming to V_{DC} period. So, from this one, for a maximum load current, we can approximately design our C. So, C will be I_{load} maximum into t_{off} divide by V_{DC}. So t_{off}, see how we can or t_{off}, t_{off} we can take t_{off} should always more than the t_{off} minimum of the transistor so that to ensure that till the device is turned off completely, the voltage across the device is not coming to V_{DC} that we can design that C. Now, this problem, turn off problem is taken care of; the switching losses, power distribution during turn off process is we have somehow taken care of, there is another problem happens.

Now, device S_1 is turned on, S_1 is off, D_2 is conducting, D_2 is conducting and the capacitor voltage is V_{DC}. Now, what happens? When S_1 is again turned on, when S_1 is again turned on, this capacitor will quickly discharge the current into the transistor. So, sometimes this current can go because transistor is turned on and the resistance is very minimal and heavy current can go, it can again go above the peak rating of the device and because of the heavy current the transistor can again get damaged. So here, what is the problem?

Now, when S_1 transistor is on, the capacitor will discharge by pumping very large current through the transistor. So, this can also spoil the devices. How to take care of this one? That means the transistor current, see this happens every turn on, see it is a repetitive action during the PWM operation. So, this repetitive current, a transistor will have a repetitive peak current, so repetitive peak current; what are the currents? The load current plus the capacitor discharge current together should be less than the repetitive peak current of the transistor. How to avoid that one? To avoid that or to limit that current; what you have to do? You have to increase the impedance. That means you have to put a transistor or put a resistance. So here, let us see how to avoid that one.

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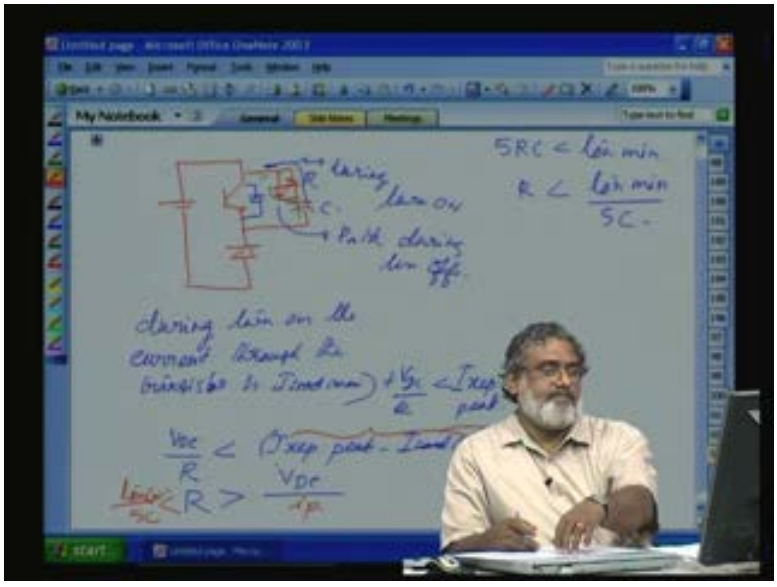

So, let us again draw the V_{DC}, now we will put, see diode is there; now we put a resistance R, R and C. So, we will choose R such that the transistor during turn on, turn on, the current through, the current through the transistor is that is I_{load} maximum we will take it, maximum

plus V_{DC} by R should be less than I repetitive peak of the device. So the R value, we can decide, R should be that means if the repetitive peak is known that is from here, if you see here, V_{DC} by R should be less than I repetitive peak minus I_{load} maximum. This shows taking R to this side, R should be greater than V_{DC} by let us take this current as some I; this current whole thing we will represent as some i_p. So, this should be, R should be greater than V_{DC} by i_p.

See, there is another problem here; we have designed the capacitor so that during the turn off period, during the turn off period, the capacitor should rise slowly. Now, R is also introduced. So, the time constant will increase. So, it will affect the switching, it will increase the switch off switching off delay. So, we do not want the R to come during the when the transistor S_1 is turned off as before. So, how to avoid that one? This I can put a diode like this, here. So, if you put a diode like this, during turn on, current will flow like this; during turn off during turn off, current will flow like this. So, this is during turn off, this is the path during turn on.

So, another problem is also there; during turn on, this RC, so PWM operation, the turn on period of a transistor will vary. Now, if sorry here this is during turn on, this is during turn off, sorry there is a mistake here; this is during turn on and this is during turn off that is what we explained. During turn off, the capacitor should slowly rise due to the load current that time we do not want the resistance to come into picture. So, transistor is switched off, current has to go through like this.

When it is turned on, this RC, this C will discharge through the discharge through the resistance but the problem is, now the time constant is increase so that means because of this turn on, the discharge, capacitor discharge time constant is increased. So, what happens? For many PWM applications, the turn on period of the transistor depend on the sine triangle comparison. So, we should ensure that RC should discharge completely during the turn on period that means during the start of the turn on period itself; before the turn on ends, the RC should quickly discharge. So, how to choose the R?

So, let us take approximately the standard practice is see 5 times RC. The time constant RC or we want to 5 times RC, 5 times RC should be less than the t_{on} minimum that is the PWM measure, turn on minimum. So, the time constant is RC and 5 times RC should be less than t_{on} minimum; this will ensure during the turn on period, the capacitor will fully discharge. This shows that R should be less than t_{on} minimum divide by 5 C. So, here if you see, the condition says R should be greater than V_{DC} by i_p, here if says R should be less than t_{on} minimum by 5 C. So, we can choose an R between these two points, decide.

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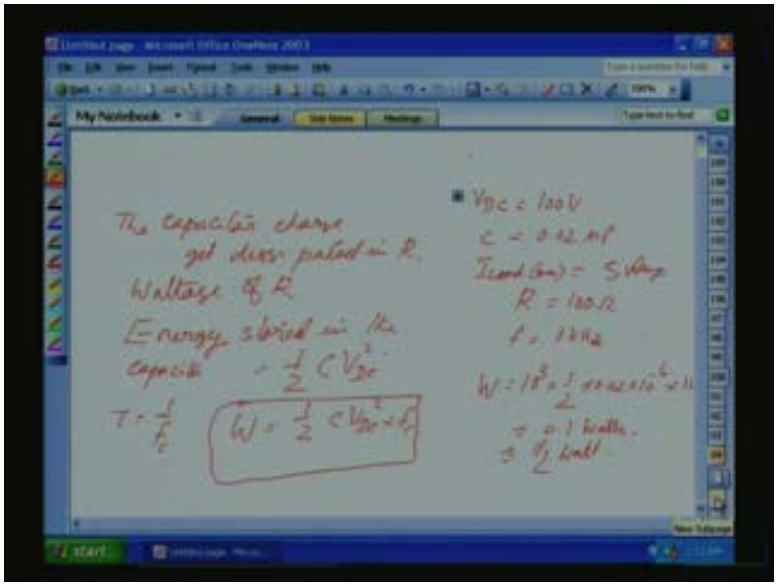

Now, another thing is, see it is discharging through the resistance, the capacitor charge is, capacitor charge gets dissipated in R. So, we have to fix the wattage, the wattage of the R, wattage of R; this is also very important. Otherwise, what will happen? We will fix the right value of the resistance what is available but after sometime we can see slowly the wattage is not proper, the resistance will get heated up, slowly smoke will come from there. So, we have to put the correct wattage.

If you see, the capacitor, what is the energy stored in the capacitor? Energy stored in the capacitor is equal to half C into V_{DC} square. So wattage, the power is equal to energy divide by pi. If you see, if you see here, what is time? Time is equal to 1 by f. What is the f here? f is the cycle, the number of time it happen that is similar to the carrier frequency 1 by fc. So, the wattage should be is equal to half C V_{DC} square into f_c. So, we should choose a resistance with the above value with the wattage more than this one.

Let us take a typical example where V_{DC} is equal to 100 volts, C is equal to 0.02 micro Fahrenheit and I_{load} maximum is equal to 5 amperes, let us take R is equal to 100 ohm, then how the wattage will be? And, the switching frequency let us take f is equal to 1 kilo hertz operation, for this one the wattage will be 10 rise to 3 into half into 0.02 into 10 rise to minus 6 into 100 square. This will be approximately 0.1 watts. So this way, we can design the transistor, the value R 100 ohms and approximately a half watt resistor be sufficient, we can approximate this one to a half watt.

Now, let us take a condition where the D_2 is conducting and we are turning on S_1 that means let us draw that; this is V_{DC}, our transistor turn on, I_{load}.

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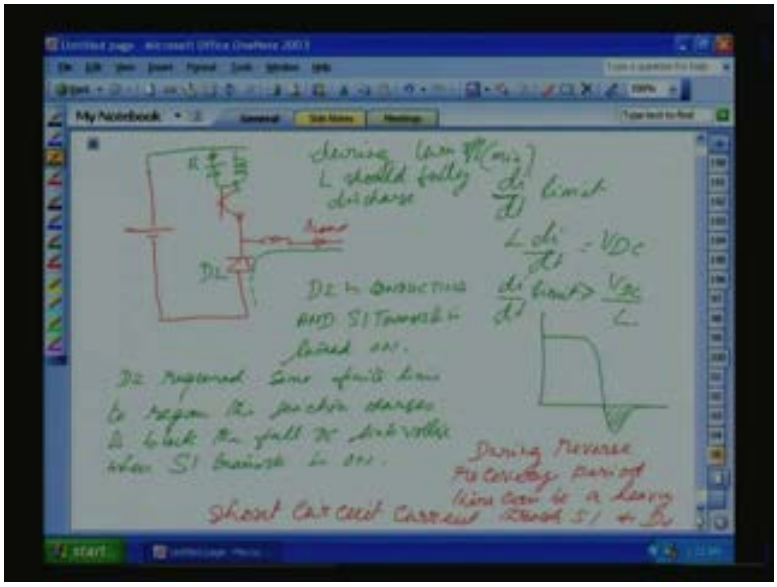

Now, let us take the current is flowing through like this that is D_2 is conducting. D_2 is conducting, now you are turning on S_1. So, the condition is D_2 is conducting and S_1 transistor is turned on. So, D_2 requires some finite time, D_2 requires some finite time to regain the junction charges to block the full DC voltage across D_2; to regain the junction charges to block the full DC link voltage when S_1 transistor is on. That means if you see here, it is not the device, the transistor diode, the diode it will go like this slowly and comes back like this. During this period, this is called the reverse recovery period; the diode will regain its junction blocking capability.

So now, what happens? During this period, transistor is conducting because of this reverse conductor. Now, the conduction is transferred from diode to diode to transistor. Now, the diode is under recovery. So, during this period, during this recovery, diode conduction is in the negative direction and the transistor is also in the direction. So, full DC link you will be short circuited that is during reverse recovery period that is this period, there can be a short circuit current through the transistor S_1 and diode D_2, there can be a heavy short circuit current through S_1 and D_2. So, because of this heavy current, the transistor can get damaged. So, this heavy current that indicates a high di by dt of the transistor has to be limited.

How to limit this one? We will put an inductance here; here we will put an inductance like this. So, this inductance L will limit the di by dt. So, how do you design the inductance? If you see, any devices, any device will have a di by dt limit. So, during this period, di by dt L should support the full DC link voltage. So, L di by dt is equal to V_{DC} or now due to the we are introducing a inductance L, that L should take care that, this di by dt should be less than the di by dt limit. So V_{DC} by L, V_{DC} by L should be, there is a this di by should be less than the di by dt limit of the transistor.

Now, this can have another effect. See, during the turn off process, now the current is flowing through the L and the transistor. Now, when the transistor is turned off, the current through the inductance cannot change instantaneously and due to the leakage part; the moment the switch is turned off, the current through the inductance will not come down to 0 immediately because the leak leakage part. So, during this turn off process, a current through or the stored

energy, through the inductance should dissipate. So, for that we should provide an alternate path that means we should put a diode here.

Now, when the transistor is turned off, the freewheeling will happen through the, even if the stored energy it is here, it will pass through the diode. Now, there is another problem; we want the inductor should dissipate completely same like the capacitor should dissipate completely during the turn on period, we want the inductor energy should completely dissipate through the freewheeling diode during the minimum turn off period that is during the minimum turn off period. So, how to do that one? So, dissipate it faster; instead of diode, we can put one more resistance here.

So, we will put to dissipate, so this RI is provided so that during the turn off period, turn off, L should fully discharge, what dissipates the stored energy is, fully discharge. So, what is the turn off period? For PWM operation, during the turn off minimum operation also, we should see that the L should discharge and ready for limit the di by dt when the next turn on comes. So here, how to decide the L R? L we know how to, some people decide L with di by dt limit or we can also use this diode recovery period.

So, this happens during the diode recovery period we can assume the current flowing through the current is slowly increasing through the transistor and slowly decreasing through the diode. So, instead of di by dt, the recovery period also, we can take it. So, during the TRR period, current is slowly raising from we can assume 0 to the full load; so TRR, di by dt we can take it by I_{load} maximum diode by TRR also we can use it. So, best is the di by dt limit. So, we ensure that the di by dt limit of the transistor is never exceeded.

Now, during turn off, so the turn on problem, we have solved; now the turn off problem happens.

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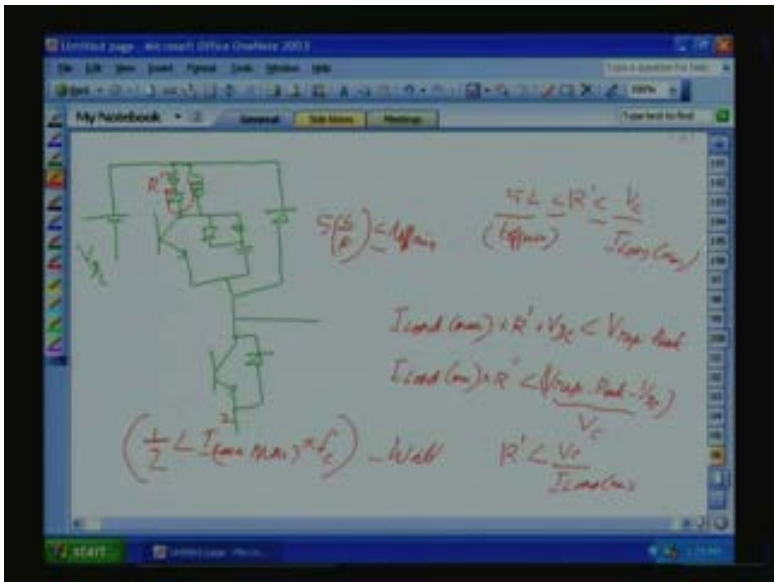

So, let us say we will draw the device like this; so turn on problem we have solved with this one, then we have the diode here, here you have the inductance, then resistance and another

diode here. Now, the DC link is here, V_{DC}, the freewheeling diode D_1 is here, here comes the S_2 and D_2, this should also have this is the load. Now, if you see here, this R dash, I would mark this one as R dash. So, we have introduced the R dash such that the L should dissipate completely within the minimum turn $_{off}$ minimum. So, let us take design approximately, 5 into L by R dash, time constant should be much less than the t_{off} minimum, the t_{off} minimum of the PWM minimum, this we can decide.

So, what this shows? This shows R dash, this shows this shows R dash should be less than or equal to 5 L divide by t_{off} minimum. Now, it can create another problem also, R. See, during the discharge here, transistor is turned off; during the discharge to this way, this transistor has to block the V_{DC} plus because of discharge this, this current plus this one. So this voltage, V_{DC} plus this voltage should never exceed the repetitive peak of the transistor that means let us take L is discharging with the full load.

Previously when this was on, L was taking the full load current. Now, when it is switched off, assuming this L is discharged through this way, transistor is assumed, we can assume transistor has quickly turned off; so worst case, design. So, I_{load} maximum into R dash plus V_{DC} should be less than the V repetitive peak of the transistor that means I_{load} maximum into R dash should be less than V repetitive peak of the transistor minus V_{DC}.

Let us us take as, this I will take as some V_C, this shows R dash should be less than V_C by I_{load} maximum. So, if you say, this condition for R dash has to be within these two values; V_C by I_{load} maximum. Here also, we have to find out the wattage of R. How to find out the wattage of R?

See, the full energy is stored in the inductor has to be dissipated in the resistance R. So, for the full energy stored let us take the full load current, half I_{load} maximum, half L I squared is the energy has to be dissipated. So, the wattage is equal to into the f_c; so this is the wattage of the transistor.

So, for discrete components if we can take care of the somewhere circuit design like this; we can protect the device for high PWM application. But now a days we get devices with high dv by dt and high di by dt but when we take discrete components to design for a switch application, if you can provide this snubber circuits; many of the old text books we can see many design details are available for snubber circuit design or many of the manufactures device detail, they will give lecture note, they will give design notes, there we can see this. So, this is one approach for designing.

So, what we want to say here? The turn on process, we do not want the high di by dt, the device should not or the turn on should be immediate to take care of the high frequency PWM; at the same time, we do not want the high di by dt. So, we will put the inductance. The moment inductance, we should also during turn off we should have the alternate path to dissipate it so that the minimum turn off period the induction should be fully discharged. So, we put a resistance R dash.

Now, due to the R dash, there be a voltage, blocking voltage across the device during the turn off process V_{DC} plus I_{load} maximum into R dash so that we have to choose R dash for the I_{load} maximum, we should never exceed that. So, turn on process, we have taken care of the device by this R dash and L snubber. Now, during turn off process, we do not want or as current slowly decreases through the transistor, we do not want during the turn off, we do not

want the full V_{DC} come immediately across the transistor. So, it will have lot off power losses. So, we put a snubber capacitor C such that the voltage will slowly rise to V_{DC}.

So, we will ensure that during the minimum turn off period, within the minimum turn off period, the voltage across the device will not rise to V_{DC} by providing a capacitor C and this will also create another problem during turn on, capacitor will quickly discharge. So, it can go the more than the repetitive peak load current, maximum load current of the device to limit that one, we put a transistor we put a resistor and the resistor means, so this can affect again the charging path. So, we put a diode parallel to that one, so it will take care of that one.

And RC, we will choose such that during the minimum turn on period also, the RC will discharge completely before the minimum turn on and the both R and R dash wattages, we have decided based on the half cv square and half li square and also on the switching frequency. So, if you take care of that one, device protection we can take care of. These are non ideality; these are the effect due to non-ideal devices; the device on minimum turn on and minimum turn off. So, how to protect the device, these you have taken here.