

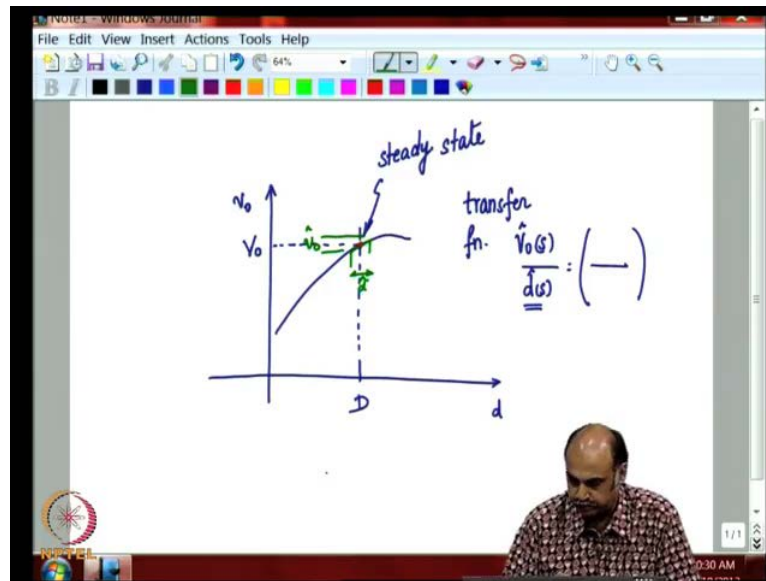
Switched Mode Power Conversion
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Lecture - 34
Controller and Sensing Circuit

Good day to all of you. We continue from where we left off in the last class. We were doing the controller design for dc-dc convertor from the model point of view. You remember that in an earlier class, we had done the controller design based on trial and error approach, and then we used the root locus technique where the small signal model of dc-dc convertor, that is the boost convertor was taken as an example, and then the root locus was plotted and on the root locus which gives basically the loci of the close loop pole location of the entire system along with the controller, a particular pole was chosen. It is responsible for the designer to choose a proper pole location and it is called pole placement, and using that value of gain corresponding to that chosen point on the root locus, the gain was substituted into the system controller and step response was seen and evaluated and then seen how close was to the performance specification. So, this iteration was continued till you reach a satisfactory design. So, this is the root locus process.

What we shall do today is, we use ngspice to simulate the circuit, boost convertor and the controller. We shall plug in the value which we obtain in the last class and see how it performs. During implementation and also simulation, you should keep one thing in mind that we are using the small signal model.

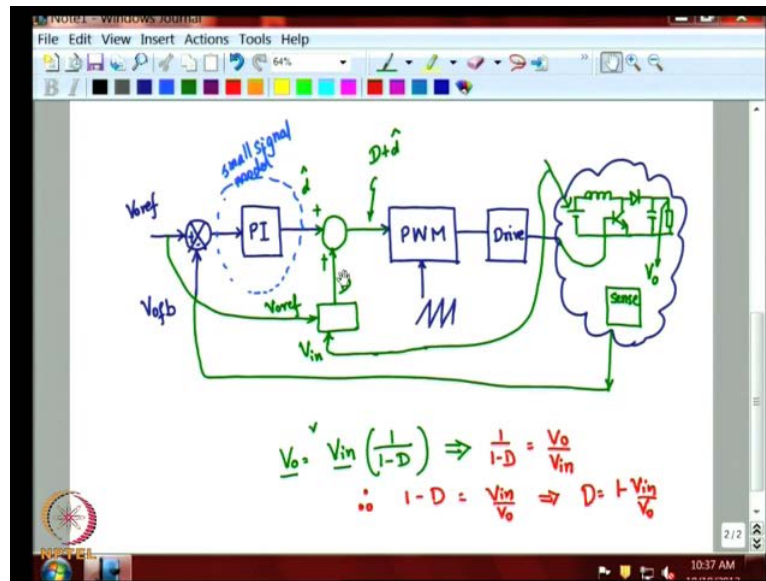
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So, if we consider for example, the boost convertor, in the boost convertor, we had used the transfer function V naught S by d of s and they were all small signal model and you had some set of zeros and poles. Now, what those small signal variables indicate is that if you are having D verses V naught and as the D increases, let us say the V naught increases. At a given operating point D and V naught, uppercase D and uppercase V naught indicating steady state operating point. This is steady state.

So, in the neighbourhood of this steady state operating point, you have small deviation which is your d hat and v naught hat. So, the model actually is representing these small deviations in the neighbourhood of the operating point and therefore, that needs to be considered while implementing the controller design.

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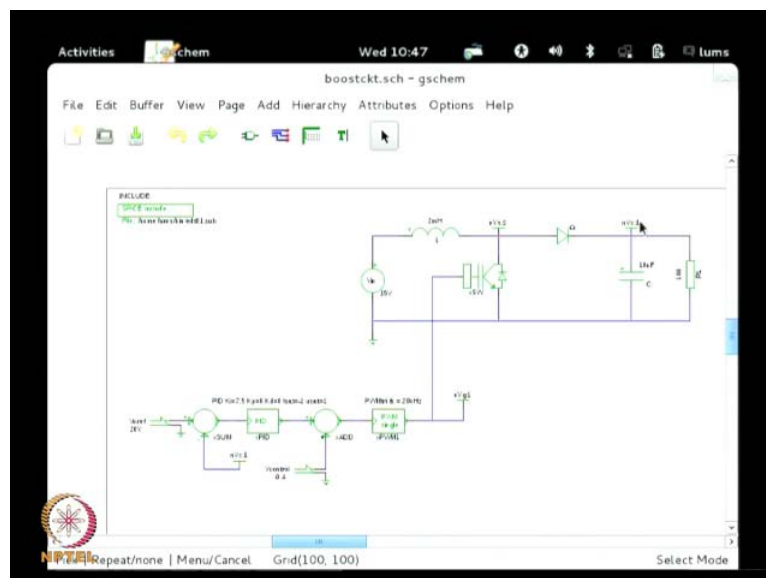
So, we make a slight modification even though this has been mentioned right at the beginning at the time of modelling. I will try to restate this problem and show. See normally our controller even in the trial and error approach, what we had was a comparator followed by a PI controller. Let us say a PI controller, we have V_{naught} reference and we have V_{naught} feedback. Now, the output of the controller goes to the pulse width modulator, PWM which actually has also another input triangle or a saw tool carrier determines the switching frequency and then, you have the driver which actually goes to the plant and the plant can be any convertor. In this case we had chosen a boost convertor like this. Let me indicate it in this fashion. So, the gate of it is actually controlled by this and you have V_{naught} coming in there and this is feedback to this, of course there will be sensing circuitry to do that, to do the feedback portion.

Now, if you look at in the case of a switched mode convertor, what we have used to design in this controller is the small signal model. So, this portion should actually focus or should be the disturbance of the steady state operating point. So, in order to do that we introduce here a feed forward term like this plus and plus. Now, let us say this represents the voltage corresponding to D and this represent the voltage corresponding to D hat. So, what you would get here is the voltage corresponding to D plus D hat. The voltage corresponding to uppercase D or the steady state operating point is obtained from the steady state equation V_{naught} is equal to $V_{in} / (1 - D)$. Therefore, this is known, this is measured which is this point. This is also measured or the reference is known. We

could have what is the value. So, from here, we can have V_{naught} by V_{in} equals 1 by 1 minus D and therefore, D 1 minus V equals V_{in} by V_{naught} and D is 1 minus V_{in} by V_{naught} .

So, what one can do is at this point have a calculator which takes in V_{naught} ref, takes in V_{in} from here. This is V in V_{naught} ref and calculate a voltage equivalent to D . So, this feed forward term ensures that even if this portion is not there, let us say it is 0 . Under steady state, this will go to zero because the steady operating point is given by this term. So, this modification has to be done in all switched mode convertors, where you design the controller based on the small signal model of this because this is supposed to only handle small signal deviations in the neighbourhood of the steady operating point.

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Now, I will try to show the boost convertor in spice. So, this is the gdea, gscan or the g schematic editor, where we normally enter the circuit and this is later on converted into a net list and ngspice is used for performing the simulation as we did in one of the previous classes for the buck convertor. So, let me zoom in on to the circuit.

So, this is the regular boost convertor. All of you are familiar with it by now. You have input dc voltage of 15 volts, you have the boost inductor; there is a power semi-conductor switch, a diode and the capacitor followed by a load resistance. This node point is labelled as NVS and this is labelled as NVC. Now, this portion, this whole boost convertor is the plant. Now, the control input for the plant is the gate drive which is

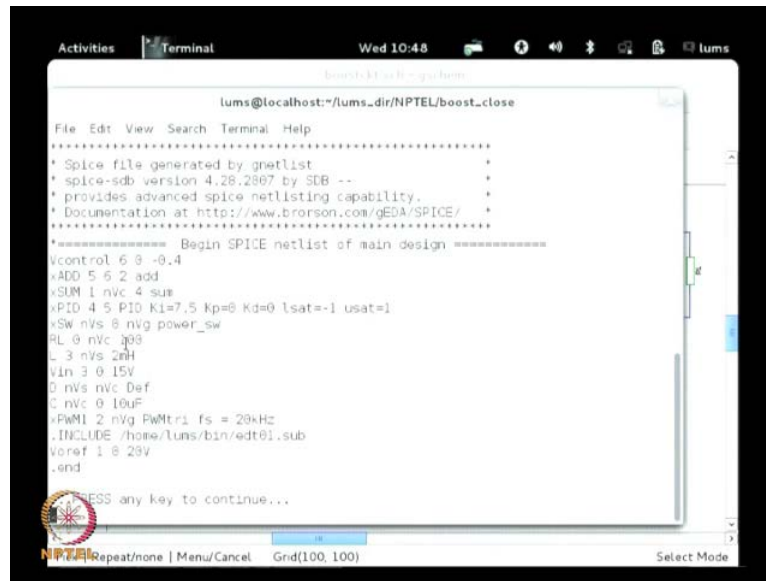
coming from the controller portion. So, if I zoom in the controller, you see that the control input what goes to the gate drive NVG is coming from the output of a PWM generator which is having a 20 kilohertz carrier, and what I was talking about just now is this portion.

See, you have a V_{naught} reference is a 20 volt. You are feeding back in VC from the output node, comparator goes through a PID. This PID value is fixed to what we had found out the gain, what we found out from the root locus plot in the class. Remember that we had kept k_p is equal to 0; k_d is equal to 0 and found out k_i as 7.5. You could include in the control structure 0 and then, later on try it as homework, try to found out the value of k_p for different values and see how the response improves. Let as just try it out what we did in the last class.

Now, the output of the PID. Now, the PID was actually, the PI controller was actually designed using the small signals modules. So, these are small signal deviations in the neighbourhood of the operating point. So, let us say this is the steady operating point I am giving it from a source, constant source. You can actually put another calculation block here, sense the input voltage and the V_{naught} ref here $1 - V_{in} / V_{naught}$ will give you the D, and corresponding voltage at this point will give you the steady state D. These two are added which will give $D + \hat{D}$. The voltage corresponding to that go through PWM and gives the pulse here, pulse output with the duty cycle of $D + \hat{D}$ will be given to the gate of the boost convertor power semi-conductors switch.

So, this is basically the modification that I was suggesting that we need to include, that is we need to have this feed forward term, such that the controllers operating for only this small signal term from in this steady state. In the steady state, this portion we had portion voltage corresponding \hat{D} portion will become 0. So, here as I mentioned earlier in the other, we give actually the file name which contains the sub circuit models of all the components. Now, this particular circuit, let us now try simulate and see what would be the voltage at their output, this 20 voltage reference and we have a 15 volts which we want it to be boosted to 20 volts as we have referred here.

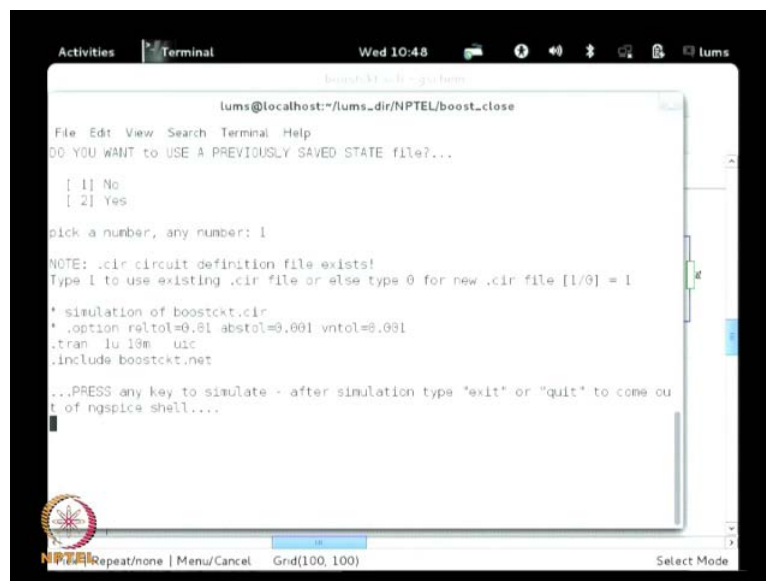
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```
boostckt.cir - gnu-lums
lums@localhost:~/lums_dir/NPTEL/boost_close
File Edit View Search Terminal Help
.....
* Spice file generated by gnetlist
* spice-sdb version 4.28.2867 by SDB --
* provides advanced spice netlisting capability.
* Documentation at http://www.brorson.com/gEDA/SPICE/
.....
===== Begin SPICE netlist of main design =====
Vcontrol 6 0 -0.4
RADD 5 5 2 add
RSUM 1 nVc 4 sum
RPID 4 5 PID Ki=7.5 kp=0 Kd=0 Isat=-1 usat=1
Rsw nVs 8 nVg power_sw
RL 0 nVc 300
L 3 nVs 2mH
Vin 3 0 15V
D 0 nVs nVc Def
C nVc 0 10uF
.PWM1 2 nVg PWMtri fs = 20kHz
.INCLUDE /home/lums/bin/edt01.sub
Voref 1 0 29V
.end

...PRESS any key to continue...
```

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```
boostckt.cir - gnu-lums
lums@localhost:~/lums_dir/NPTEL/boost_close
File Edit View Search Terminal Help
DO YOU WANT TO USE A PREVIOUSLY SAVED STATE file?...
[ 1 ] No
[ 2 ] Yes

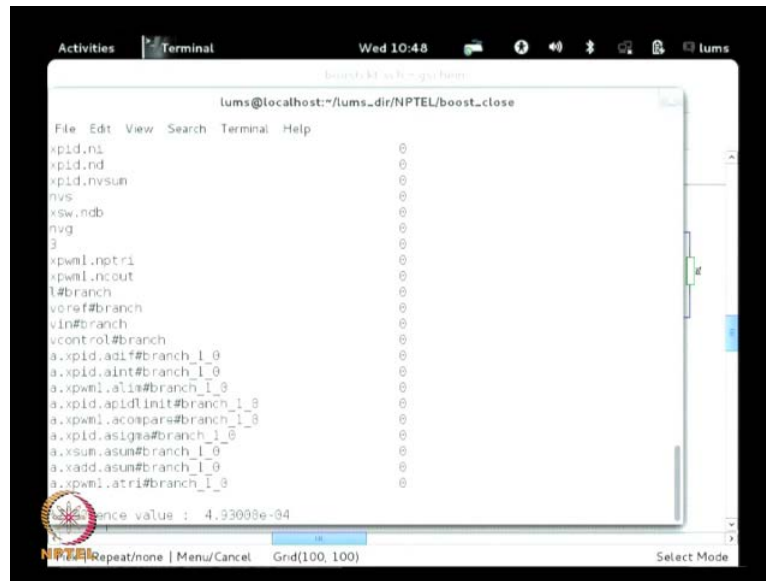
pick a number, any number: 1

NOTE: .cir circuit definition file exists!
Type 1 to use existing .cir file or else type 0 for new .cir file [1/0] = 1

* simulation of boostckt.cir
* .option raltol=0.01 abstol=0.001 vntol=0.001
.tran 1u 10m uic
.include boostckt.net

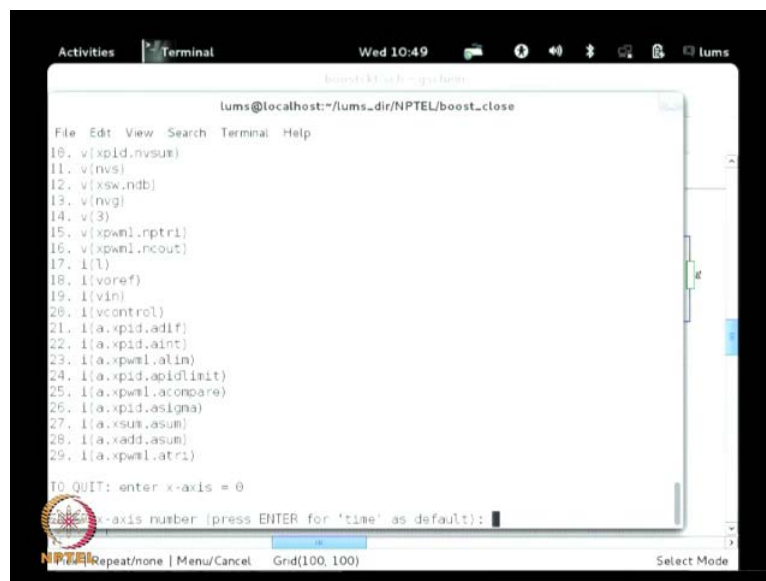
...PRESS any key to simulate - after simulation type "exit" or "quit" to come out of ngspice shell....
```

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```
lums@localhost:~/lums_dir/NPTEL/boost_close
File Edit View Search Terminal Help
xp1d.n1 0
xp1d.nd 0
xp1d.nvsun 0
nvs 0
xsw.ndb 0
nvg 0
3 0
xpwl.rptr1 0
pwl.ncout 0
l#branch 0
voref#branch 0
vin#branch 0
vcontrol#branch 0
a.xpid.adif#branch_1_0 0
a.xpid.aint#branch_1_0 0
a.xpwl.alin#branch_1_0 0
a.xpid.apidlimit#branch_1_0 0
a.xpwl.acompare#branch_1_0 0
a.xpid.assigna#branch_1_0 0
a.xsun.asun#branch_1_0 0
a.xadd.asun#branch_1_0 0
a.xpwl.atri#branch_1_0 0
a.x...
Reference value : 4.93000e-04
```

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```
lums@localhost:~/lums_dir/NPTEL/boost_close
File Edit View Search Terminal Help
[0] v(xpid.nvsun)
[1] v(nvs)
[2] v(xsw.ndb)
[3] v(nvg)
[4] v(3)
[5] v(xpwl.rptr1)
[6] v(xpwl.ncout)
[7] i(l)
[8] i(voref)
[9] i(vin)
[10] i(vcontrol)
[11] i(a.xpid.adif)
[12] i(a.xpid.aint)
[13] i(a.xpwl.alin)
[14] i(a.xpid.apidlimit)
[15] i(a.xpwl.acompare)
[16] i(a.xpid.assigna)
[17] i(a.xsun.asun)
[18] i(a.xadd.asun)
[19] i(a.xpwl.atri)

TO QUIT: enter x-axis = 0
x-axis number (press ENTER for 'time' as default):
```

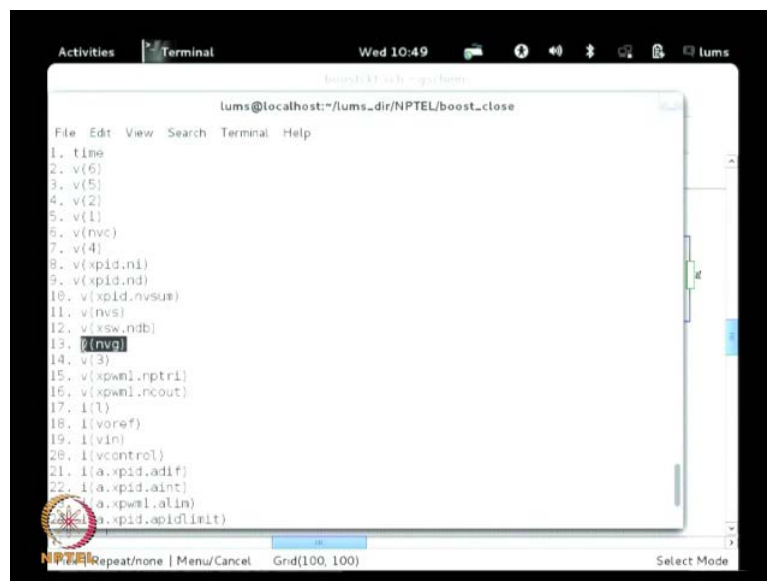
So, going back to the command line let me go to that particular folder. Now, I will run ngspice through a script file written in octave called ngsim boost circuit dot schematic. So, when you run that, the first thing that will be done is the net list will be generated and later, we go into the ngspice simulator engine which does perform the simulation, calculates all the node voltages in the branch current and gives you all the possible variables which can be observed. You see that here NVC, the node which we are labelled as the output, you want to see that.

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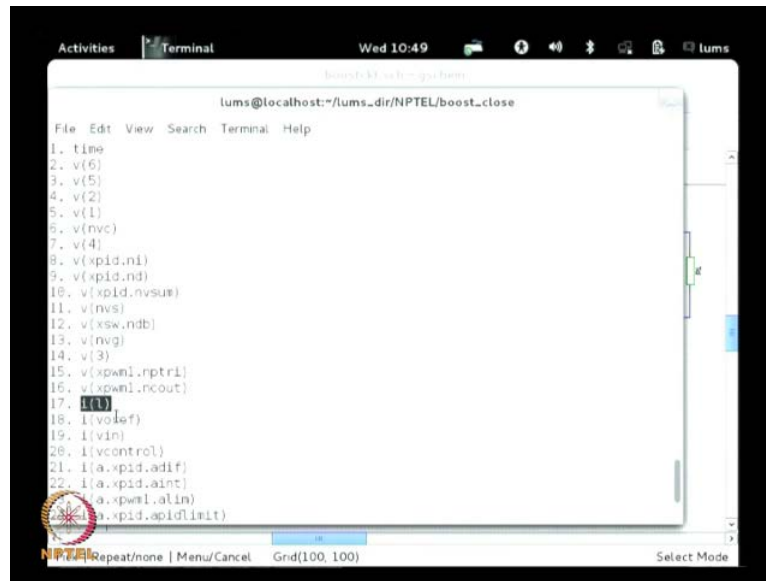
```
lums@localhost:~/lums_dir/NPTEL/boost_close
File Edit View Search Terminal Help
SELECT X-axis and Y-axis
1. time
2. v(6)
3. v(5)
4. v(2)
5. v(1)
6. v(nvc)
7. v(4)
8. v(xpid.n1)
9. v(xpid.nd)
10. v(xpid.nvsur)
11. v(nvs)
12. v(xsw.ndb)
13. v(nvg)
14. v(3)
15. v(xpwn1.rptr1)
16. v(xpwn1.ncout)
17. i(1)
18. i(voref)
19. i(vin)
20. i(vcontrol)
21. i(a.xpid.adif)
```

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```
lums@localhost:~/lums_dir/NPTEL/boost_close
File Edit View Search Terminal Help
1. time
2. v(6)
3. v(5)
4. v(2)
5. v(1)
6. v(nvc)
7. v(4)
8. v(xpid.n1)
9. v(xpid.nd)
10. v(xpid.nvsur)
11. v(nvs)
12. v(xsw.ndb)
13. i(nvg)
14. v(3)
15. v(xpwn1.rptr1)
16. v(xpwn1.ncout)
17. i(1)
18. i(voref)
19. i(vin)
20. i(vcontrol)
21. i(a.xpid.adif)
22. i(a.xpid.aint)
23. a.xpwn1.alin)
24. a.xpid.apdlimit)
```

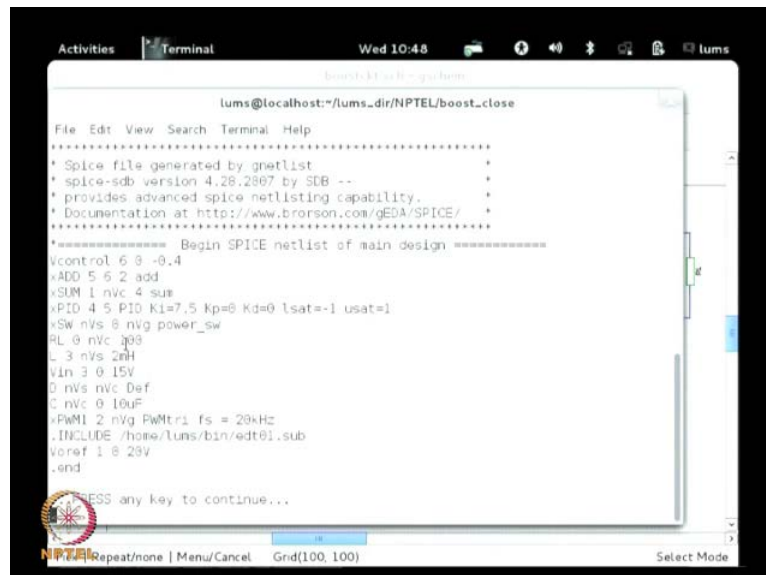

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```
lums@localhost:~/lums_dir/NPEL/boost_close
File Edit View Search Terminal Help
1. time
2. v(6)
3. v(5)
4. v(2)
5. v(1)
6. v(nvc)
7. v(4)
8. v(xpid.ni)
9. v(xpid.nd)
10. v(xpid.nvsut)
11. v(nvs)
12. v(xsw.ndb)
13. v(nvg)
14. v(3)
15. v(xpwm1.rptr1)
16. v(xpwm1.ncout)
17. i(l)
18. i(volef)
19. i(vin)
20. i(vcontrol)
21. i(a.xpid.adif)
22. i(a.xpid.aint)
23. i(a.xpwm1.ain)
24. i(a.xpid.apid1rit)
```

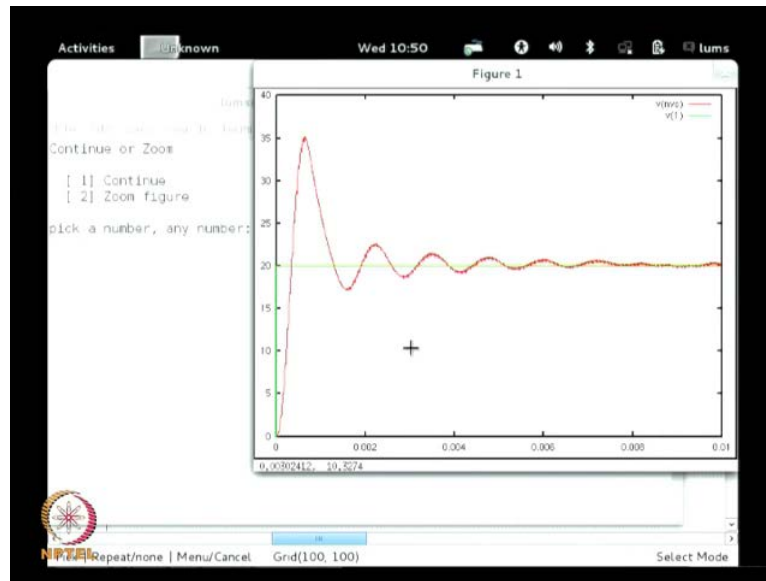
We could see NVG; the one which we want is basically the pulse width modulated wave form, the pulses which are given to the gate. We could see that. We could also see the (()) current through the inductor. So, one by one we could have a look at how these look like, so if you see the voltage of NVC and the voltage V naught ref.

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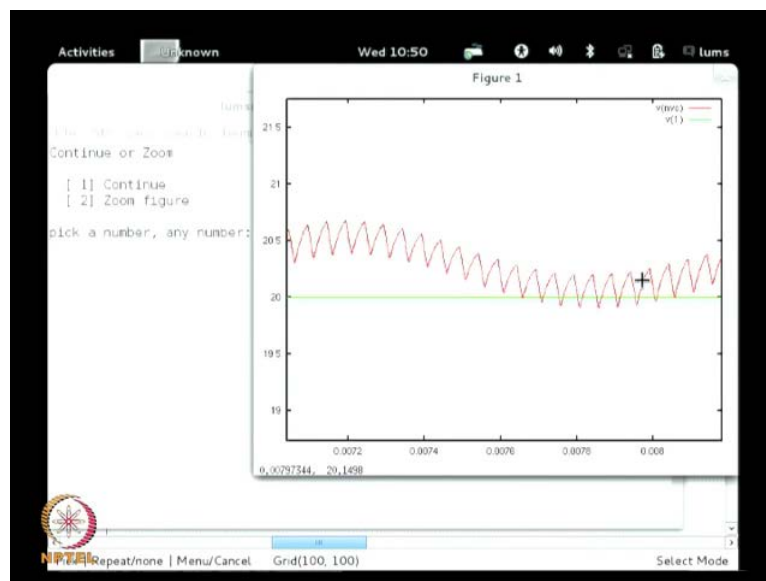


```
lums@localhost:~/lums_dir/NPEL/boost_close
File Edit View Search Terminal Help
*****
* Spice file generated by gnetlist
* spice-sdb version 4.28.2007 by SDB --
* provides advanced spice netlisting capability.
* Documentation at http://www.brorson.com/gEDA/SPICE/
*****
***** Begin SPICE netlist of main design *****
vcontrol 6 0 -0.4
xADD 5 6 2 add
xSUM 1 nvc 4 sum
xPID 4 5 PID Ki=7.5 Kp=0 Kd=0 Isat=-1 usat=1
xSW nVs 6 nVg power_sw
RL 0 nVc 300
L 3 nVs 2mH
Vin 3 0 15V
D nVs nVc Def
C nVc 0 10uF
xPwm1 2 nVg PwMtr1 fs = 20kHz
.INCLUDE /home/lums/bin/edt01.sub
Voref 1 0 23V
.end
PRESS any key to continue...
```

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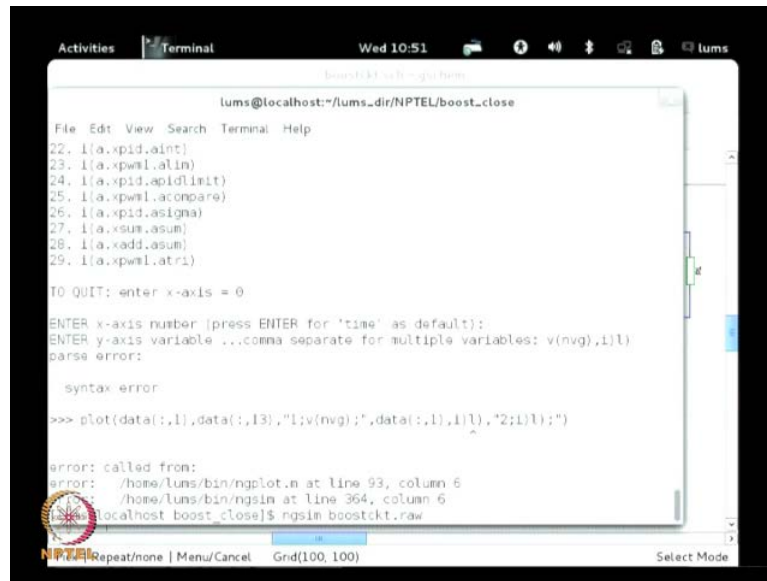


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Now, if you look at the net list here, V naught ref is node 1. So, we could see node 1 also, V of node 1. So, you see that this is the green waveform is node 1 which is actually the reference and the output voltage is trying to get controlled and reaches the stable state. You could zoom in and try to see the nature of the ripple, calculate and study all those characteristics.

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```
lums@localhost:~/lums_dir/NPTEL/boost_close
File Edit View Search Terminal Help
22. i(a.xpid.aint)
23. i(a.xpwl.alin)
24. i(a.xpid.apidlimit)
25. i(a.xpwl.aconpare)
26. i(a.xpid.aigna)
27. i(a.xsus.asum)
28. i(a.xadd.asum)
29. i(a.xpwl.atr1)

TO QUIT: enter x-axis = 0

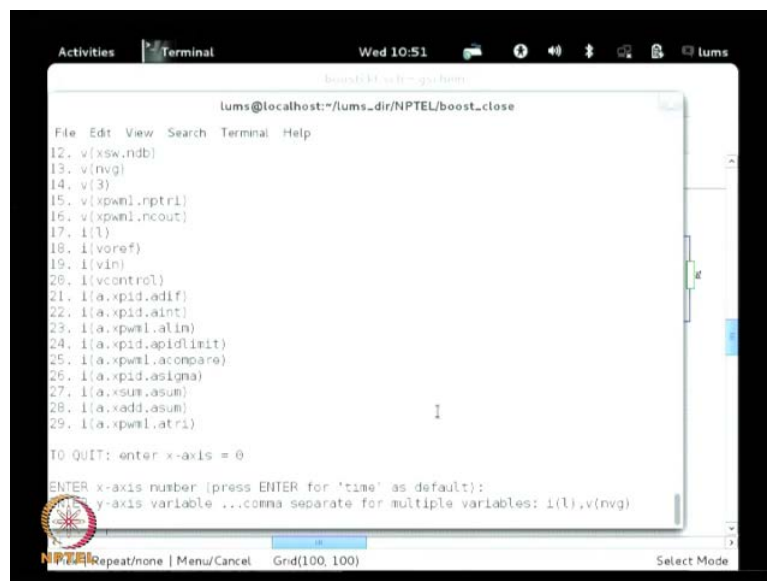
ENTER x-axis number (press ENTER for 'time' as default):
ENTER y-axis variable ...comma separate for multiple variables: v(nvg),i(l)
parse error:

syntax error

>>> plot(data(:,1),data(:,13),"i:v(nvg);",data(:,1),i(l),"2:l(l);")

error: called from:
error: /home/lums/bin/ngplot.m at line 93, column 6
error: /home/lums/bin/ngsin at line 364, column 6
lums@localhost boost_close]$ ngsin boostckt.raw
```

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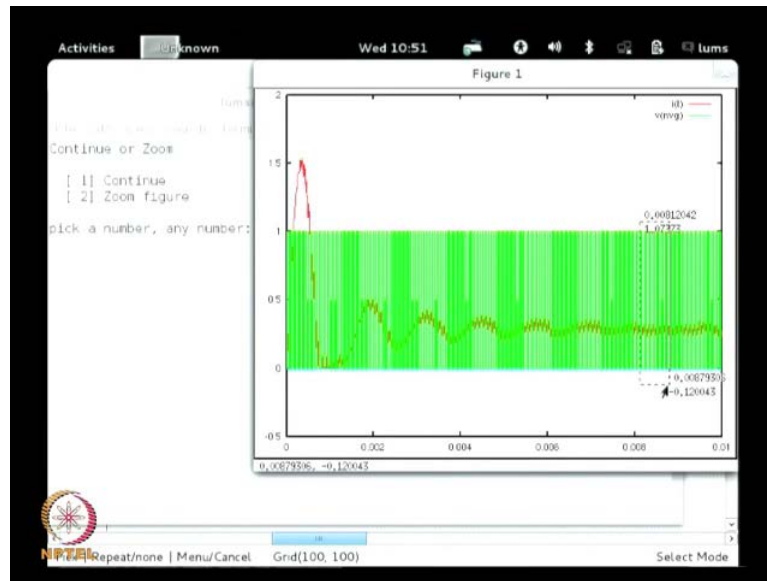
```
lums@localhost:~/lums_dir/NPTEL/boost_close
File Edit View Search Terminal Help
12. v(xsw.ndb)
13. v(nvg)
14. v(3)
15. v(xpwl.rptr1)
16. v(xpwl.ncout)
17. i(l)
18. i(voref)
19. i(vin)
20. i(vcontrol)
21. i(a.xpid.adif)
22. i(a.xpid.aint)
23. i(a.xpwl.alin)
24. i(a.xpid.apidlimit)
25. i(a.xpwl.aconpare)
26. i(a.xpid.aigna)
27. i(a.xsus.asum)
28. i(a.xadd.asum)
29. i(a.xpwl.atr1)

TO QUIT: enter x-axis = 0

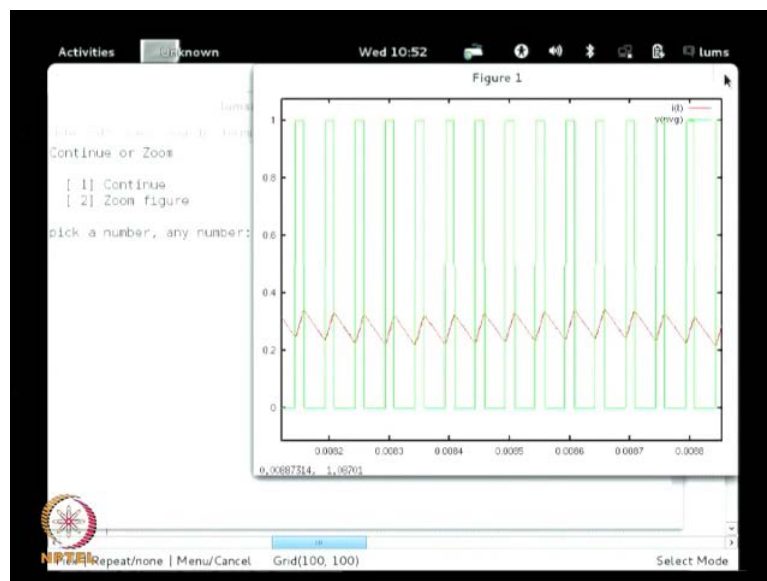
ENTER x-axis number (press ENTER for 'time' as default):
ENTER y-axis variable ...comma separate for multiple variables: i(l),v(nvg)
```

We could also have a quick look at the il waveform and nvg waveform. The inductor current waveform and you see, these two super posts, let us zoom in so that we could, so let me zoom near the steady state portions.

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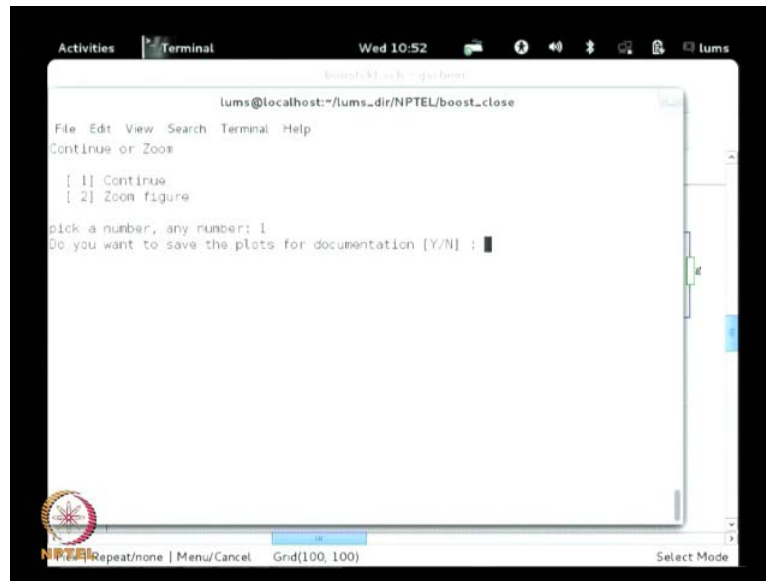


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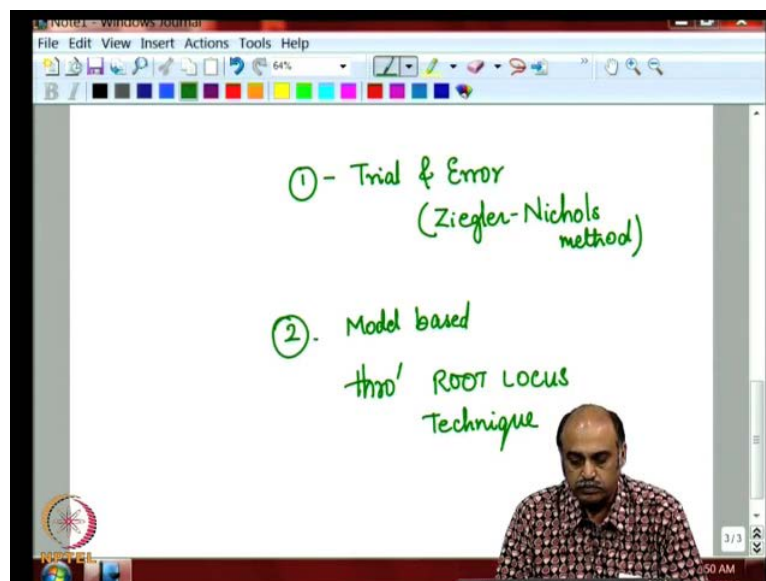


So, this is the red waveform is the inductor current waveform, and the green waveform is actually the pulse width modulated waveform that has been generated to achieve that steady output voltage of 20 volts. So, this pulse width modulated waveform 0 to 1 is actually the gate drive signal which is given to the boost convertor switch and you see this triangular waveform in the current waveform in the inductor as discussed in the analysis of the boost convertor, ok.

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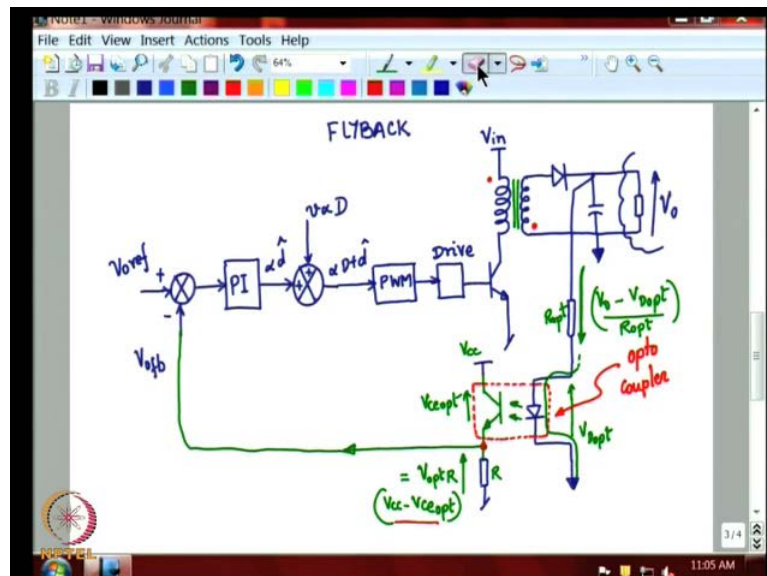
So, we stop here at this point and let me go over back to the white board. So, we have discussed the trial and error approach something similar to Ziegler-Nichols method, and we have seen the other model based through the root locus technique. As I said people have used bode plot technique that also is quite popular using the gain and the phase margin. However, for the switch mode power convertors, where they are made using the three primary convertors, the building blocks like the boost convertor, the buck convertor, the buck boost convertor. The boost convertor in particular has 0 on the right of the s plane, bode plot is not valid and cannot be used for such non-minimum phase

system and all the boost derivatives will not be in a position to be addressed by bode plot method.

The root locus method is much more general approach and it is something similar to the pole placement approach of the state space, or the model control systems and this can be applied even for non minimum phase systems. Therefore, the root locus technique can be used when you know the model of the system well, and when you have the small signal model or even the large signal model and if the system is a black box, apply the trial and error method.

Now, let us go forward and see some of the problems that we would get during implementation. Now, let us take the example of an isolated convertor. Now, isolated convertor or the forward convertor, the half bridge, push pull and the fly back convertor. Let us take the one of the popular topology like the fly back convertor, and see how the feedback is achieved. You remember that we were discussing while feeding back, we just drew a line from the outputs to the feedback point, but actually there is a sense circuit in between and let us have a look at that sense circuit, so that we have a complete schematic.

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So, if we take the fly back convertor, it is of this form. You have the fly back transformer which is also actually an inductor, where I am using this b j t or i j b t. You can actually replace it with mosfet, i j b t or b j t or let say, you have this drive and this comes from

the output of the PWM signal in this fashion. Now, on the secondary side, we have just a diode and capacitance which goes on further to other loads. Let me indicate it as a resistive load in this fashion. It is very important to note that the dot polarities of the transformer are in this fashion for the fly back as you have studied earlier in the class.

So, briefly the operation is very simple when the switch q is on. You have dot as positive at V_{in} , and the non dot end as connected to the ground that is 0. Therefore, this dot end is positive, this dot end would also be positive. In the secondary side reverse places the diode and the diode is off, the secondary side portion is off. Only the capacitance is discharging to the load. So, during this time the current flow through this transformer, this is actually an inductor. It has a near gap inside and starts storing energy in the reluctance within the (()). When this is switched off, the energy which is stored within is now released, starts freewheeling through secondary. There is a reversal of polarity, the non dot end becomes positive, this becomes positive, and this will try to forward bias the diode and pump the energy into the capacitance, and there by replenish the charge that the capacitance lost during the cycle when this diode was off.

So, this is briefly how it operates. This is the fly back convertor and here, we have the comparator, compare and control plus minus, you have V_{naught} reference and V_{naught} feedback, the output of which goes into the controller, PI controller which is plus and plus. So, you give a voltage which is proportional to D here and this voltage is proportional to \hat{D} , and this will be proportional to D plus \hat{D} .

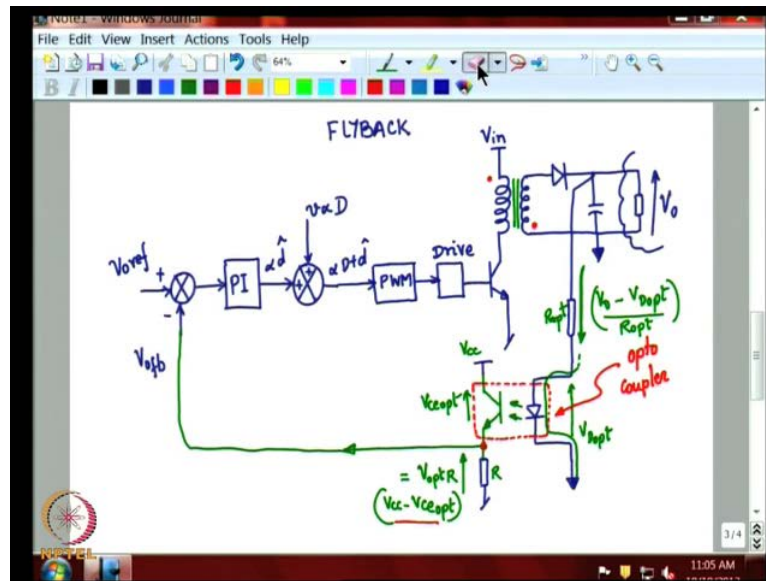
Now, all along we have been trying to say that this of course is V_{naught} . You take V_{naught} and feed it back here, every simple line. However, in practice we cannot just draw a simple line such like that. There are two issues. One is compatibility and another is there is this isolation. This main function of the transformer, one of the main function of the transformer is to achieve a voltage scaling, such that the load voltage becomes compatible with a V_{in} for a given duty cycle, and the other function is input and output galvanic isolation. That is also a very key important parameter to be addressed because most of the time, you like to have isolation of the load with the input side power and also with the control side power. Therefore, we need to interpose in between here something which does maintain that isolation, and also sends across the information.

So, one of the very nice way do that is to use an opto coupler and like this, I will use a different common point symbol. Observe that these two labels or symbols are connected and this is different. These are galvanically separated. They are not connected together. So, it is like saying that we have a thick line wire connecting these two, but in order not mess up the paper, we normally keep this line out and then, put a symbol at this point and the same symbol at this point indicating that these two are wired tightly together. So, the opto coupler is having the diode on the primary side and has b j t on the secondary side and together, it is available as a pack in this form. So, this is the opto coupler.

Now, considering this kind of opto coupler connected in this fashion, we shall introduce one more component here instead of connecting the voltage directly through to the opto coupler, we normally would like to protect it, allow only predefined amount of current to flow through. So, you need to have a resistance and allow only that much amount of opto current for which it is rated and then, let us say we have a resistor here and then, you have some voltage which is connected across that with respect to ground. Now, if you tap at this point and draw the signal from here, this signal we will call at this one V_{opt} across R . This signal will be a measure of the output V_{naught} . Consider the current which flow through like this through this R_{opt} . So, it will be V_{naught} minus. If this is $V_{D_{opt}}$ divided by R_{opt} will be the current that is flowing through in this resistance through the primary into this virtual grounded output which actually comes back here complete the circuit. So, this is how it would be going.

Now, this amount of current comes and flows through. This will bias this transistor, the opt transistor here and it will be at some operating point, and it will have some V_{ce} . So, what appears across here would be if this is V_{cc} minus $V_{ce_{opt}}$, this is $V_{ce_{opt}}$, so the voltage across the emitter resistance r , is this value. So, as the voltage V_{naught} increases, I increases, the transistor is biased more to the saturation, $V_{ce_{opt}}$ decreases and once this decreases, V_{cc} minus $V_{ce_{opt}}$ increases or V_{opt} across R increases. So, this value increases. So, v_{naught} increases, this value increases. V_{naught} decreases, the current through decreases. The transistor is bias more away from the saturation $V_{ce_{opt}}$ increases and V_{opt} decreases because of this.

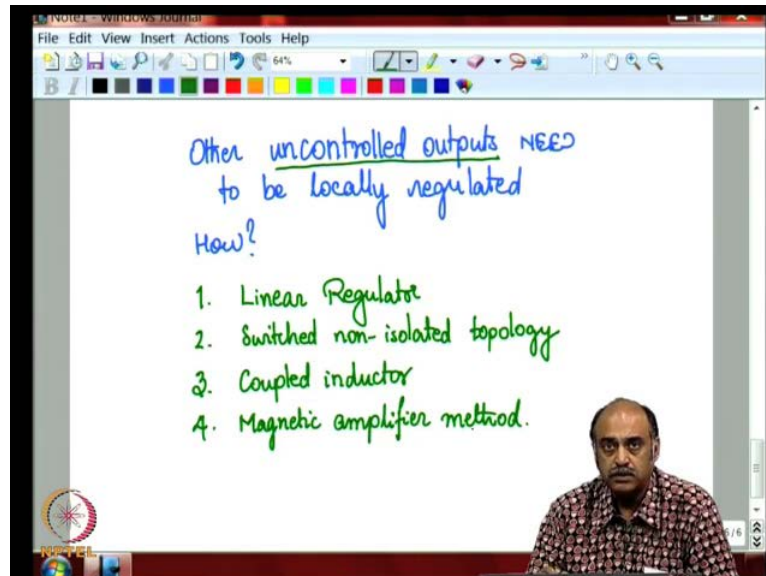
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So, this point tries to have the same proportionality with respect to V_{naught} and also, preserving the galvanic isolation. So, this V_c connected here in more size in circuits, where you need size output regulation, the transfer ratio, the current transfer ratio, the opto coupler, and the voltage across the opto coupler is dependent on a temperature, especially the voltage V_D of is dependent on temperature. As temperature varies, this value varies and therefore, current varies and therefore, the bias point varies. Therefore, the output that is feedback here even if the voltage here, V_{naught} has not vary. Because of the temperature variation, this value would have varied and the controller thinks that the output is varied and tries set two different values. Therefore, in order to compensate of the temperature, normally another component is included.

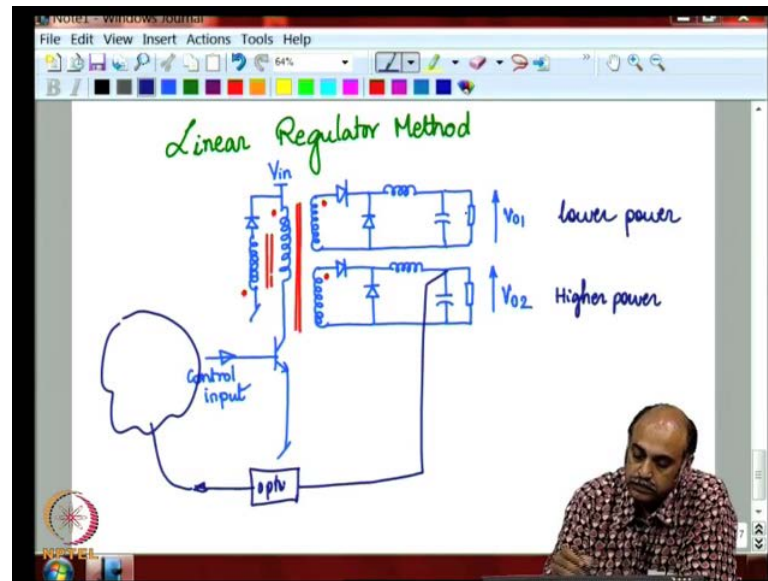
to feed 50 watts max, then this is the output that will be fed back and take that, pass it through the opto circuit and feed that back.

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What happens to $V_{naught 2}$? What happens to the other output or other outputs? There are more than 2. They need to be locally regulated. The other uncontrolled outputs need to be locally regulated. How? There are few methods and one method is linear regulator method using switched non isolated topology. You could use coupled inductor method. There is the magnetic amplifier method. These are some of the more popular ways by which regulation of the uncontrolled outputs are addressed. So, we shall see these possibilities because in a practical power supply, you will always find power supplies having multiple outputs. So, one by one let us take up these methods and see how it is accomplished.

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So, first by the linear regular method. It is very simple. Let me draw this time, I will draw another converter instead of fly back. Let me draw the forward converter with demagnetizing winding. It could be half bridge, full bridge, fly back, any just that to break the monotony, I will try to draw some other converter. This is the topology of the forward converter isolated multiple outputs. It is not very popular though because of too many inductor components. I will just draw two outputs. These are the two outputs. You have the load across them and this is the control input.

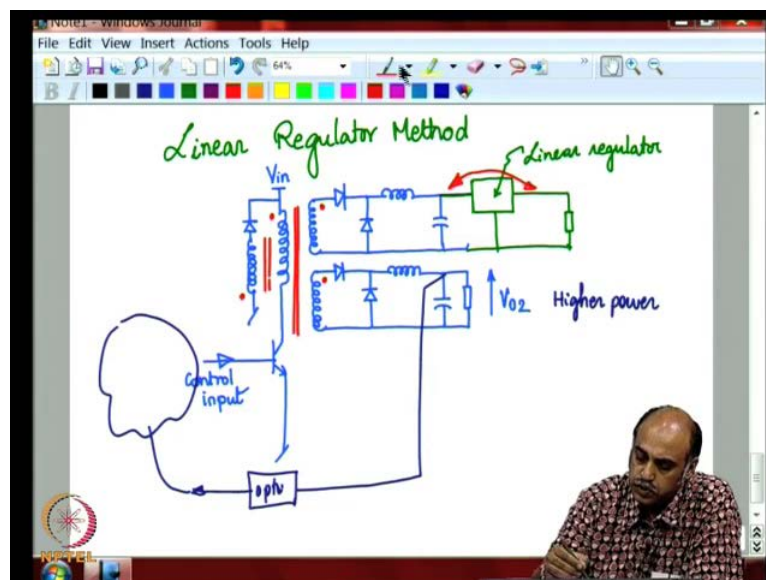
Dot polarities in the forward case, the dot polarities are like that. Refer back to your class and be careful. The dot polarity of this is the opposite. All are on the same core, and this is V_{in} , this is $v_{naught 1}$, $v_{naught 2}$. So, what is the operation? When the switch is on, this primary winding is connected to ground, the dot portion is V_{in} and by the terms ratio times, the dot here is positive, dot here is positive, turns on this diode, the forward biases and the potential occurs across this diode. This diode is reverse biased, charges up the inductor and capacitance in the inductor is building up, the inductor energy is also building up.

Now, because this dot is positive, this diode is reversed biased. Now, this is switched off. The moment this is switched off, there is the reverse law polarity, dot end becomes negative, non dot becomes negative, non dot becomes positive here, non dot is positive. This diode is turned off; the inductor will start freely like this at the same time because

non dot end is positive, this is positive. This will turn on diode and put energy into the supply. So, the magnetizing energy is pushed into the supply. So, this is the operation of forward converter which we already know.

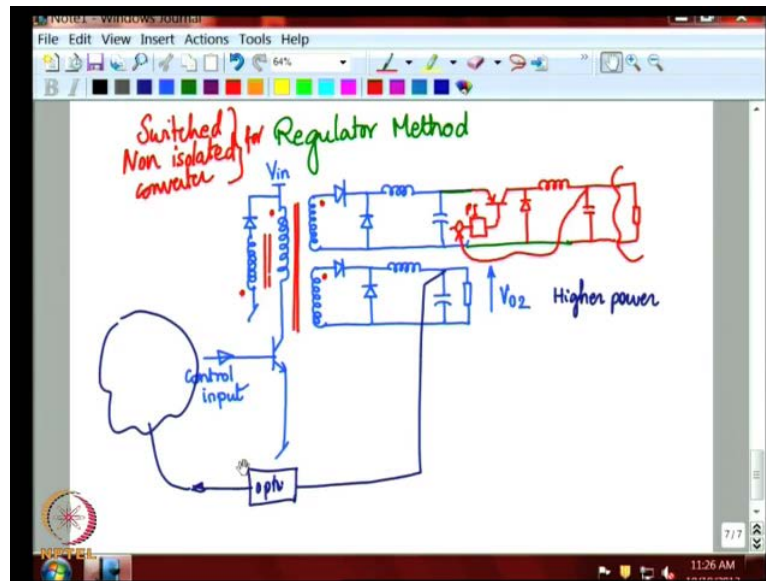
Now, the problem as I was trying to tell is how we control the two outputs. So, depending upon the power; now let us say that this is the higher power, this is the lower power one. So, higher power let as feedback through our regular opto circuit that we discussed to the control version.

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Now, for the lower power let us do a local regulation with a linear regulator. If it is a linear regulator, three pin fixed linear regulator and then, give it to the load. So, this would be a linear regulator, three pin regulator, either a fixed one like this. 1 7 8 series are the variables ones at the 3 1 7, those type of regulator. So, what happen is that the pulse with modulated switching converter here tries to bring the voltage here to a more compatible voltage to the output. It is only different by the amount of regulation and this block. So, this block is this probe here across the linear regulator is maintained to just a minimum, so that the loss is kept minimum and further, this is a low power side. So, this linear regulator does the job of regulating this unregulated portion and thereby providing a good regulated output here. The higher power output portion is automatically getting regulated because that voltage is fed back through the opto given to the controller which gives the proper controller signal to modulate the drive duty cycle here.

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So, on adjusting the duty cycle here, not does this only change, this would also change that the variation here is regulated by this linear regulated. Instead of using a linear regulator, one could use a switched mode regulator point. The regular bulk converter says you could have a buck converter like this, another small inductor, capacitance and the load and you have a small PWM and the local control, and this is feedback here, the voltage. So, this would be a $v_i p w m$, this would be a local regulator based on T 1 4 9 4 or any other pulse with modulator which is using the output voltage here itself power supply to power up all these portions control circuitry. This portion, the control circuitry is powered up by this or powered up by the regulated unregulated voltage of this at this point. Then, the gate drive is supplied to transistor which does the buck operation here and then, appropriately you get a regulator voltage at this point.

So, this is a local regulation and such type of locally regulated converters is basically called switched non isolated converters for regulating the output. So, this is the second method. That means first method linear regulator where this portion was replaced with linear regulator, so that it is the output regulator. Instead of linear regulator, you can use a switched non-isolated topology like the buck, the boost buck depending upon the output that would like to regulate here and use that output voltage for having a local feedback control loop which will adjust the duty cycle of the switch here, and give a regulated output. The other winding, output winding goes through the same way as we have discussed now. Now, there are two other methods, coupled inductor method and the

method of magnetic amplifier which we will have to discuss which we shall do in the next class.

Thank you.