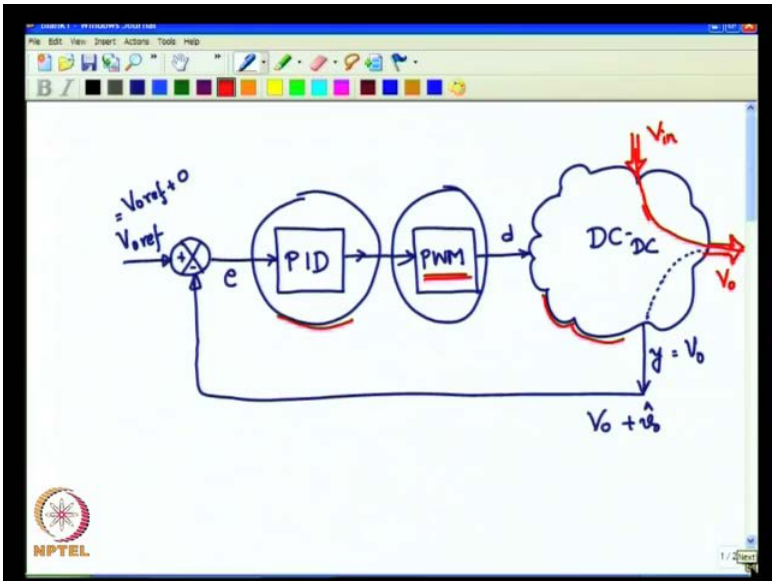
Switched Mode Power Conversion
Prof. L. Umanand
Department of Electronics System Engineering
Indian Institute of Science Bangalore

Lecture - 31
Pulse Width Modulator

Good day to all of you. Till now, we have been discussing on modeling the DC DC converter, and we have been discussing on the controller. We discussed about the PID controller and the block diagram. The various aspects of, how PID controller can be protected from anti anti wind up and such issues.

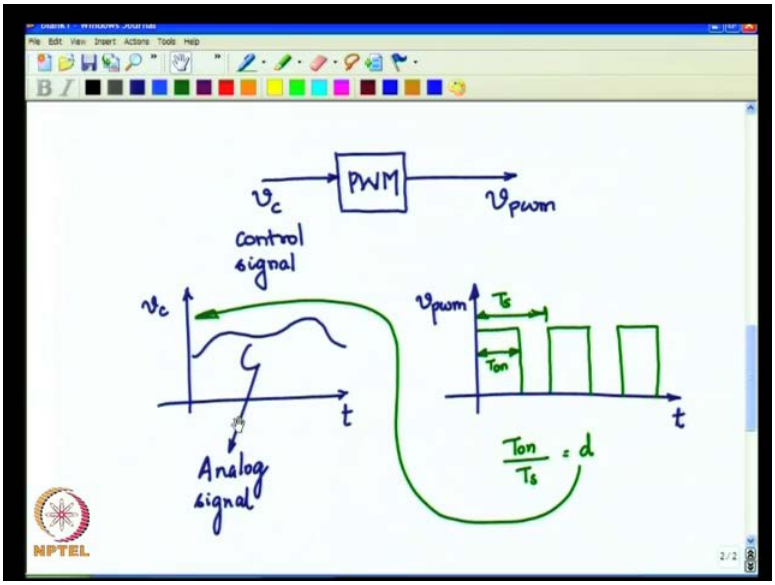
(Refer Slide Time: 01:04)



So, if you look at the block schematic in bird's eye, the bird's eye view of the whole system look something like this; this is the DC DC converter. Now, this has an energy input, power input V in, power output V naught; it has two non-power ports, signal ports. One is control input that is where you feed in variation duty cycle, another signal port is an output in fact, where the signals are sensed for feedback, this sensed signal does not contain or does not pass power, but only an information back to the controller. So, in this case, it senses the output voltage and that is feedback and compared with a reference the error is feed to a PID controller.

Now, output the PID controller, is given to a pulse width modulator and chop the pulse width modulator is to convert the voltage, which is on the input terminals to a signal, which contains the information of the input signal in terms of time. So, the variation here is in terms of duty cycle, so voltage amplitude to duty cycle conversion is performed by this pwm pulse width modulator. So, let us look at, what goes inside the pulse width modulator, before actually performing the whole exercise of control in simulation or or in hardware. So, let us take up the topic, of pulse width modulation and then get back to the topic, of control for the DC DC converter.

(Refer Slide Time: 03:58)

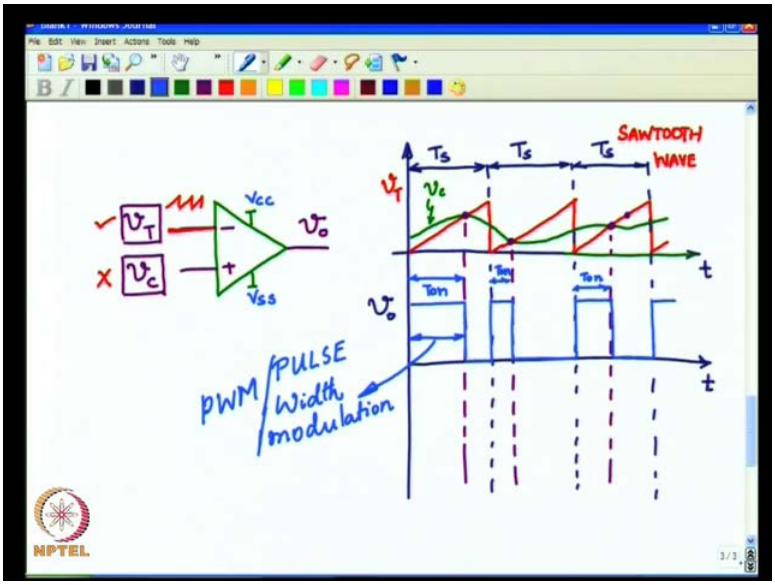


Now if you take the pulse width modulator, the pulse width modulator is black box, so give an input v c a control signal, this is the control signal. Now, this has an nature with respect to time v c is an analog signal, this is an analog signal. Now, the pulse width modulator takes such an input signal and gives an output should call that, as v pwm output of the pulse width modulator. This is somewhat like an digital signal discretize v pwm, this is converted to, this type of signal. Where this width in time with respect to this width t s this is T on.

So, T on by T s, which is equal to the duty cycle, this is need proportional to v here v c to this waveform. So, that is the job of pulse width modulator, an analog signal continuously varying is converted into a discrete signal, which has, which has two levels either a high level or a low level, this is the low level, this is the high level two states.

The time for which it is on the high state time for, which it is off; that is low state that is controlled and is made proportional to this analog sig. So, this is essentially what the pulse width modulator does, and let us see how this can be achieved?

(Refer Slide Time: 07:41)



So, now let us take a very basic simple case consider an op amp, so we have an op amp is at it is assumed that, it has it supply it has three terminals, other than the supply signal terminals, one is minus one is plus and the output terminal. Now, let us say to this minus terminal I give a signal v T and to the plus terminal I give the signal v c. Let us see what, we would get at the output of the op amp. Now, what you get at the output op amp depends upon the natures of these two signals v T and v c.

Now, v c is an input to the modulator, so this is generally not under your control, however v T is under your control. We want to make the output proportional to the output proportional to the input v c proportional in time, that is the duty cycle is made the output duty cycle is made proportional to the input v c. So, let us consider the following case, now let us draw waveform versus time, let me divide the time into few cycles each of period T s. So, let us say, we have these three periods here of course, these periods keep repeating each of time T s.

Now, let us say that v T is of the following form, at it is a linearly rising waveform up to that period n and drops down to 0 and again linearly rising, at the end of the period drops down to 0 and keeps repeating in this fashion, this is nothing but a saw tooth wave

pattern. So, let us say that this v T, which is a saw tooth wave pattern is generated by some means and applied to this terminal here. So, to this terminal the applied something like this, the saw tooth wave at.

Now, v c is an analog signal input signal as mentioned just previously before, where it is coming from the output of the controller the slightly varying analog signal. Let us say it has an amplitude less than the maximum saw tooth amplitude. Now, look at the points of intersection in every period, we have a following points of intersections, of v c with the saw tooth or v T. Let us mark that, now the points of intersections as indicated here by the violet line, violet dotted lines.

Now, let us draw one more axis here, with respect to time and let us plot v naught. So, remember that this green wave shape is nothing but v c, the red wave shape is v naught v T. So, let me mark that in the same colour, as the wave shape v T, now what is v naught? Now, go back to the op amp circuit, now this op amp is acting like a comparator, whenever v c is greater than v T, whenever v plus is greater than v minus v naught will go and clamp to positive maximum of power supply.

Whenever v c is less than v minus v pus is less than v minus, the output of the op amp will clamp to the negative of the power supply. So, if we say that the positive of the power supply is v cc and the negative of the power supply the lower level is minus vss. So, you have two states, state one the higher state v cc, lower state vss. So, let us see what happens, now at the left of the intersection point, this is the intersection point in this period to the left of the intersection point, you see v c is greater than v T. So, v c v plus is greater than v minus and then therefore, the output will be clapped to v cc the positive maximum.

So, during this period, you will see that it is clapped to the positive maximum this is v cc. During the period to the right of the intersection point, you see v c is lower than v T v minus is greater than v plus and then v naught will be clapped to the lower portion of the, lower state of the power supply, which is let us say it is 0, it could be anything other than 0 also anyhow for the sake of this graph we will put it as 0.

So, you have then again in the next cycle, you see that here v c is higher than the red that is v T and therefore, the output v high here. So, this will jump up and to the right of the intersection of that period, you see that v c is lower than v T, v plus is lower than v

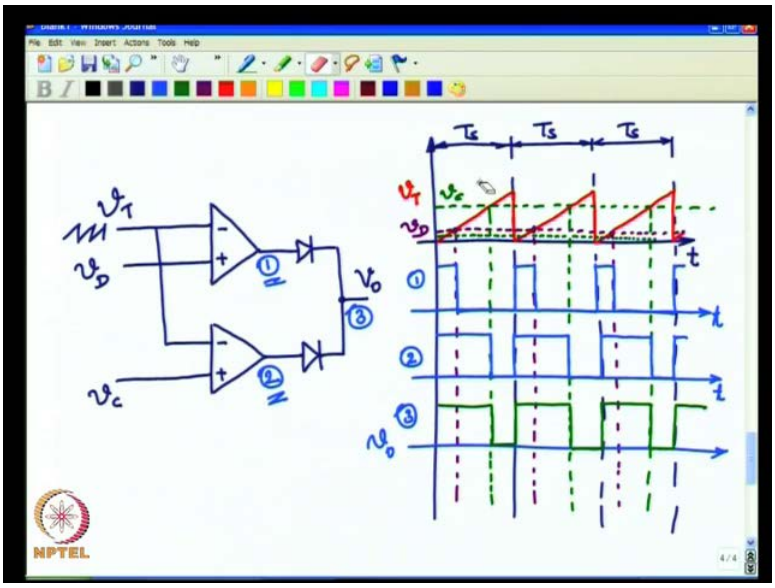
minus therefore, v naught clamps to a lower value v c c v s s. So, on every cycle the situation is same to the left of the intersection point, you will see that v c is greater than v T. Therefore you will find the output getting clamped to the positive maximum of the power supply and towards the later part of the cycle, it will the output will clapped to the lower part.

However what is interesting here, is the intersection point itself, so if you look at the intersection point. Now, this intersection point can swing anywhere from here to here. So, if you see here, let us say, let us say for example, I make the following modification, let us consider the v c, which is having intersection at different points as shown, we retain the ramps, we retain the saw tooth pattern only, we change the v c. Let us say v c has large amplitude in the cycle, a small amplitude in the cycle. So, on like that where the intersection points are now, in this fashion and you see that it becomes evident at, when the intersection is at higher value of the ram observe that, the duty cycle is large. When the value of v c is low, the duty cycle has dynamically changed to a low value.

So, the point of intersection is actually the key in pulse width modulator, which actually dynamically controls the on state, this is the on time and this is the on time the next cycle, this is the on time third cycle so on. So, you see that the on time is large in, this case v c is larger on time is small here, likewise v c is lower so on on time as increase again with the increase in v c. So, as v c is varying the amplitude of v c is mapped to the on time, is mapped to the on time of the output and this results in what is called as the pulse width modulation. So, what is actually being accomplished is modulating the pulse width, this width modulation.

As the amplitude is kept flat part and reasonably constant, what you achieve the wave shape is a pulse and therefore, it is called as pulse width modulation in acrony acronym form it is PWM. So, this is the basic concept of a pulse width modulator, which is employed in most switch mode converters dc dc converters power converters. Now, let us go a bit mode deeper into this pulse width modulator towards, what you would see practically.

(Refer Slide Time: 24:07)



Now, taking from where we left of let us say, we had that op amp and let me now include one more op amp and minus plus minus plus. I am assuming that there is power supply and to the minus let us give the saw tooth v T of the saw tooth shape. Let us give to one of the pluses v c and to another plus v D, let as call it v D. What do we do with the output, let as or them diode or them, so this is called diode oring and the diode ored output is called v naught.

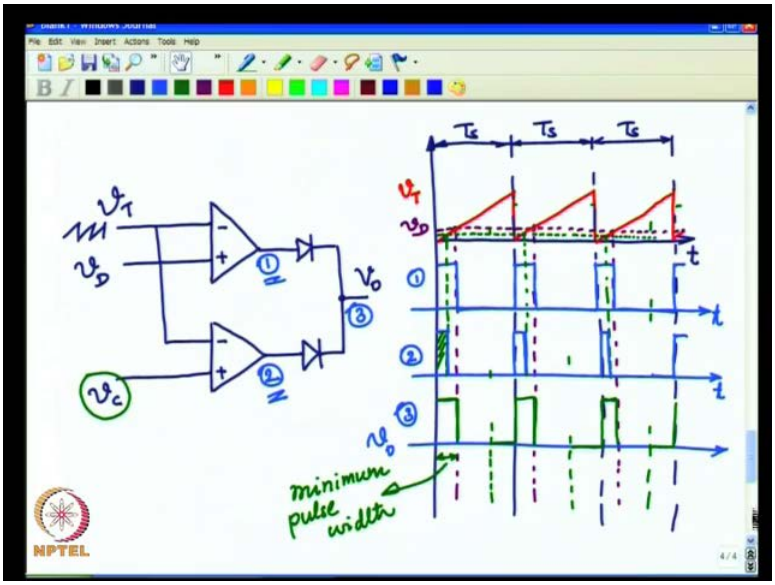
Now, what do we get out of this, let us quickly plot the wave shapes and see what we get now, look at this across is a three time periods, switching periods like before and we have v T. They are saw tooth linearly rising dropping down to 0 at the end of cycle linearly rising once again and so on this is a v T. Now, let me draw two lines and am going to mark them as dotted now, this violet coloured line the low is mark it as v D and the green coloured line am going to mark it as v c.

So, you see that v D has a point of intersection, with the same triangle ramp and v c also has a point of intersection every period, with the same ramp v T because, v T is given as a common minus input to the two op amps. So, now that we have drawn all the lines markers ,let as take one axis another axis t and try to plot v naught. Now, for this v c what is v naught, now v naught and if we take v c here, is greater than v D and therefore, even when during the time v D is low.

Let let me make small modification here, let us have some more clarity. Let me plot first this as 1, 2 and 3. Now, let us plot one the output of op amp at one, you see that it has a wave shape something like this now, this is how the wave shape looks would look at the output of one. Now, let us plot, what it would like at 2 here, it is with respect to this input v c. So, as you see we are taking the intersection corresponding to hop that v c and then what is v naught 3. v naught is nothing but oring of this wave shape and this wave shape, which is nothing but this wave shape in this case.

So, v naught is nothing but this itself, this itself is your v naught. However the issue would cop up, when what happens when v c has gone below vd look at this am carefully drawing, this v c has gone below v D, which means let us take out some of these confusions.

(Refer Slide Time: 31:55)

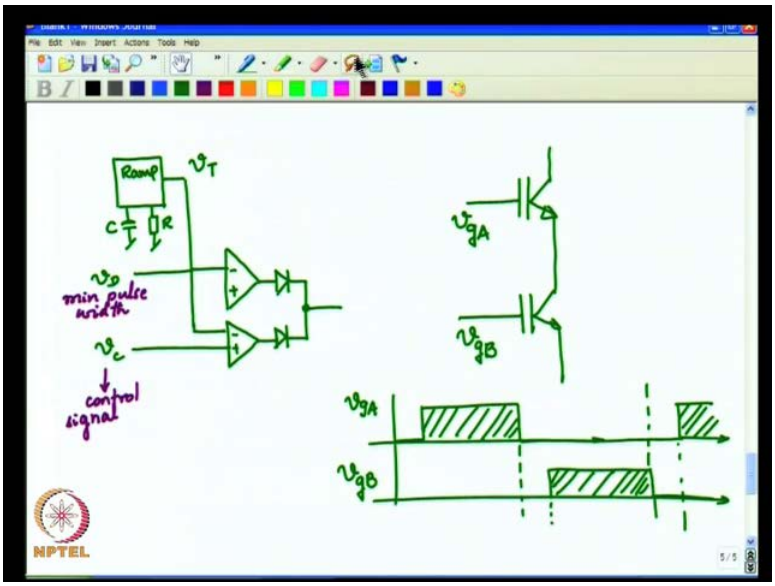


We will redraw then first what would happen to the output. So, am going to redraw some of these, notice that the v c intersection is smaller across at a lower part of the ramp and output of 2, is limited to small pulse like this. What is 3 now, 3 is nothing but oring of 1, 2 and 3 becomes same as one. So, this may vanish but, still v naught will remain at this value, so what do you take away what we see here, is minimum pulse width. In most of the switch mode power converters, the switches are nothing but power semiconductor devices.

Now, the power semiconductor devices cannot switch at very, very low pulse widths, there should be minimum pulse width given to the power switches of the switch mode converters, otherwise there will pulse skipping and other undesirable effects. Therefore, in most of the pulse width modulators a minimum pulse width is decided and fixed. So, even when the input signal, even when the input signal goes to a very low value, which results in very small pulse width, the v D portion of the op amp, which is oared together.

Here, will ensure that the output pulse width does not go below, what is decided by v D. So, that is an important part of the pulse width modulator to fix the minimum pulse width of that, can be applied to the power semiconductors switches. So, next let us see, what we try to achieve, so this is one aspect let us go further from there.

(Refer Slide Time: 36:05)



Try to put in the entire, we saw that, we have two op amps with diode oring and these two op amps resulted, at in kind of the pulse width modulated output. Now, let us say we have another black box and out of the black box given is v T the saw tooth way. In most of the cases a saw tooth wave is generated by means, of timings that are set by two components a capacitance and a resistance the R and C. The R C time constant of, which determine the period of the saw tooth then we shall call this as v D.

Let us say we have v c, v c is the control signal coming from the output of pid, v D is called dead time control or just say minimum pulse width, minimum pulse width control. So far the moment we will call this as, min pulse width. So, now the output of this, we

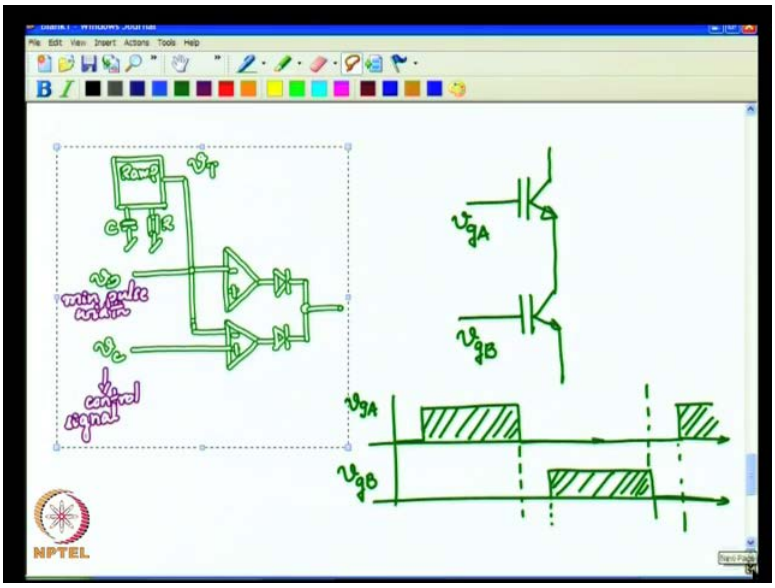
know is the pulse width modulator circuit. But there are many circuits, like the push pull, like the full bridge, lithe half bridge, where you need to give pulses, pwm pulses to the two switches, to two switches, which are complementary. Then not 180 degrees exactly 180 degrees complement. They are not in fact supplementary, they are actually complementary as you would see we would like to give a pulse something like this.

Now, if you are having a full bridge circuit composed of two semiconductor switches; that is HIGPT's. Now, let me call this one as v gate A v gate B, now we would like v gate A to the of this fashion, we would like v gate B to be something like this. So, see that v gate B is not an inversion of v gate A, v gate B is complementary to v gate A occurring at a time, when we v gate A is fully off, but there is also a gap. A common time, when both are off is necessary because all these power semiconductor devices are practical devices, they need finite time to switch on and switch off.

So, when of when one of the transistor is on and other is off, we need to give some specific time, this is called the dead time. During which time, you are allowing the on transistor to turn off and allowing the off transistor to turn on without having an overlap are therefore, I should through, current should through. So, in order to have such safety we need to provide some time, where both do not get gate drive, do not gated gate drive pulse.

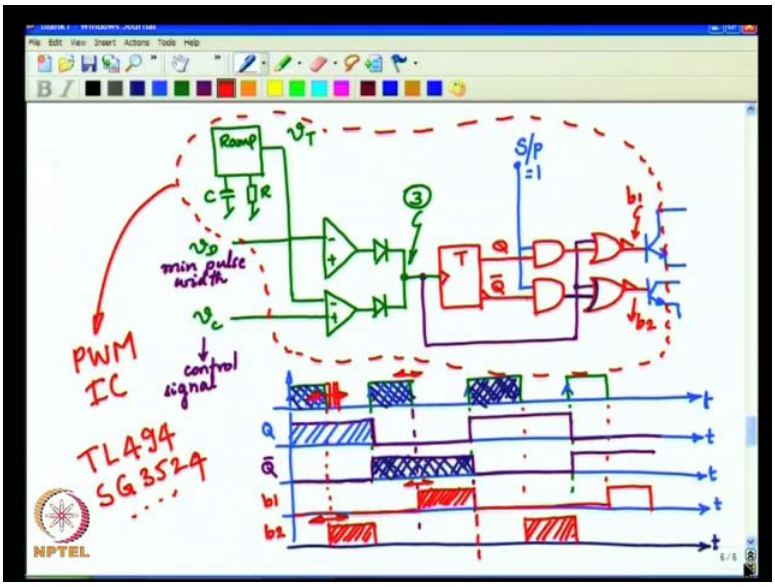
This is a type of output that is needed by most of the power semiconductor devices drive signal therefore, let us see, how the raw pulse width modulated wave shape is modified to something of this time? So, if it is for single ended output just only this one any one of them can be utilized, if it is for double ended switching both complementary pairs, you need to use both of these signals.

(Refer Slide Time: 43:03)



So, so continuing from, where we left of let me take this portion alone and paste it here, now to this circuit let us add a flip flop.

(Refer Slide Time: 43:40)



Now, let me put a toggle flip flop, this is a t flip flop you have Q and you have Q bar. Now, the output of these two go to two and gates and output of those two and, gates go to two nor gates as shown like this. Now, look at what is going to be done from here, the input you draw a line and give it to the other inputs of these nor gates. The other input of the hand gate is brought out and we will call it as a steering control or we just call it as S

bar P, series or parallel. Let us see what it means or it could be single ended or push pull mode for dual drive complementary drive.

So, when it means S, an S is S bar P is 0, this and gates are disabled and nothing from the toggle flip flop is going to affect here. So, this is 0 and what you get directly from the output is state to go this or gates and you would get exactly similar waveforms here, x except they are inverted. When this is equal to one that is, when you have the push pull mode or complementary mode. Now, let us see, what happens to the various waveform and the output of this in general is given to two bipolar transistors and they are brought out.

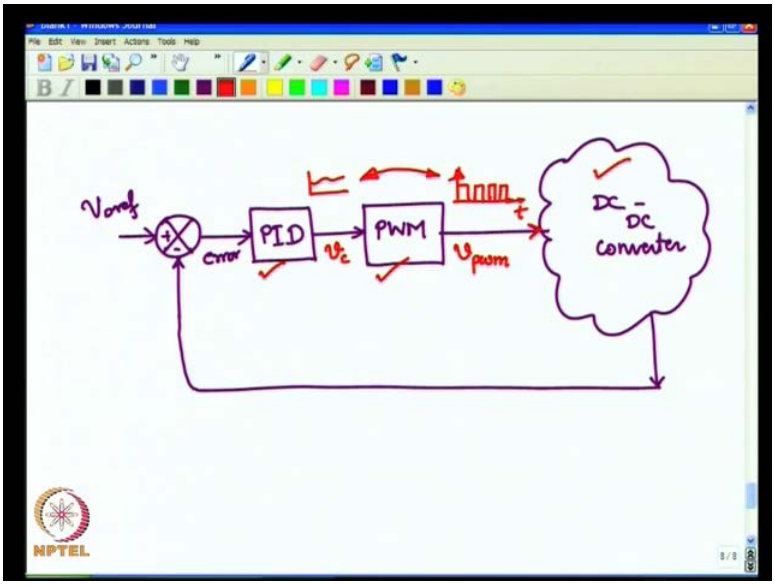
Now, let us start, let us start with the waveform at 3 we know that waveform, this is 3 if you go back we had named it as 3. So, we will again call it as 3 starts from there and what you had at that point is pulse width modulated waveform something like this. Now, what is obtained at Q, Q this is toggle flip flop at every positive edge at every positive edge the toggle flip flop is triggered and you would get the change of sate. So, let us say we get it change of state at this positive edge, you have another change of state at this positive edge, you have another change of state.

So, on and likewise Q bar, Q bar is nothing but any inversion of Q, this is exactly 180 degree inversion of Q no dead time here, as such as comes in this fashion. Then let us see what is the, now because S bar P is 1this and gates are enabled the Q and Q bar signal go directly cleared to this point the or point. The signal this signal is oared with this and inverted, so oring of this and this signal would mean, like that and like that oring and inversion an inversion would mean, a direct inversion of this.

Therefore, am going to write am going to remove this and write the nor signal, which is like this. This is at base 1 likewise base 2 is the complementary output this I will call it as base 1. Now, here this is oring of this signal oring of this signal, you see here, with Q bar what comes at Q bar here. So, Q bar is now oring of this and this and take this inversion would give waveforms like this. So, on notice that b 2 and b 1 are complementary there is no overlapping zone and we have the dead time. So, as this is varied this pulse width varies, as this pulse width varies you will see a variation in pulse width here, likewise a variation in the pulse width here for the b 1 b 1 waveform.

So, as this varies, this will vary, so this will give the pulse width modulated complementary signal. So, in fact most of your pulse width modulators have this kind of basic structure, which would give you to possibility of complementary signals possibility of having the staying steering line. When it is made 0 the output is the point 3 output is directly brought to the output an internal ram an internal power supply. So, there are many pulse width modulators available, these are available as pulse width modulator IC's. One very common pulse width modulator IC with this structure, which we use is T L 4 9 four S G 3 5 2 4 and many more.

(Refer Slide Time: 55:03)



So, the pulse width modulator in short can be put as a v c as the input and the output which is the PWM. Notice that there are two possibilities, because most of the output of pulse width modulator have an output stage and both the emitter and collector are brought out. So, if you connect an external circuit in this fashion or if you connect an external circuit in this fashion, there if you take v pwm from here or if you take v pwm from here, both will definitely give PWM output pulse width modulated output.

However there is an 180 degree inversion, between this PWM output and this PWM output because here, you are taking it from emitter here, you are taking it from collector which results in 180 degree output. So, very, very careful and count the number of phase shift that you have within the loop in order to have, an over over phase shift proper for closed loop negative feedback keeping that in mind. Now, this has to be brought into

focus for our overall closed loop picture that we had, which is the controller the PI or PID followed by PWM the modulator, which is connected to the DC DC converter the output feedback is fed across to this, we have v naught reference error output of the PID is called v c and the output of PWM is v pwm. What you have here, the waveforms analog signal and what you would have here, is pulse width modulator kind of discrete switching signals. This information is fed to the DC DC converter, basically the control signal information is, fed into DC DC converter has a switching pulse width modulated signal.

So, this of course, is our complete control block diagram. So, we have seen the various aspects of the block diagram, we have seen how to model the DC DC converter, we have how to model the PID controller and we have also add a discussion on, what the PWM modulator is and how it look inside. Now, in the following classes, we will try to look at this whole control system block diagram as a whole. See how we can design this and also how we can read this and simulate this, to get better inside into the whole system.

Thank you.