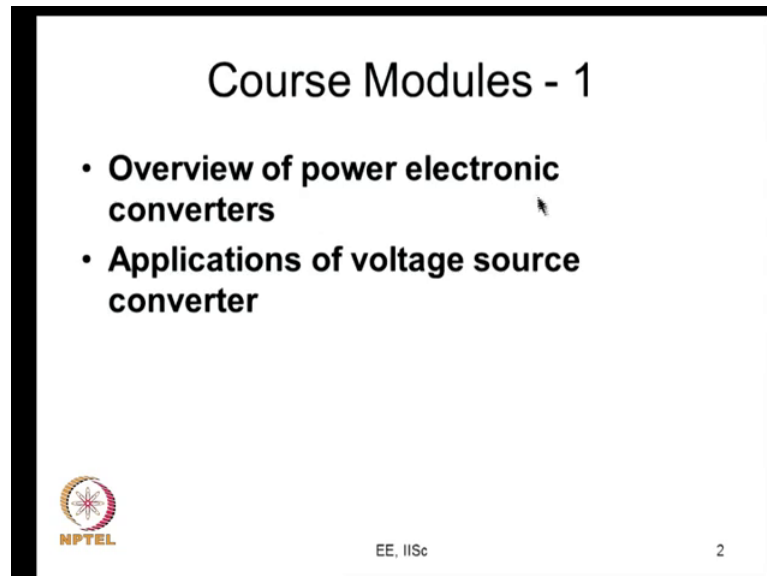


Pulse width Modulation for Power Electronic Converters
Prof. G. Narayanan
Department of Electrical Engineering
Indian Institute of Science, Bangalore

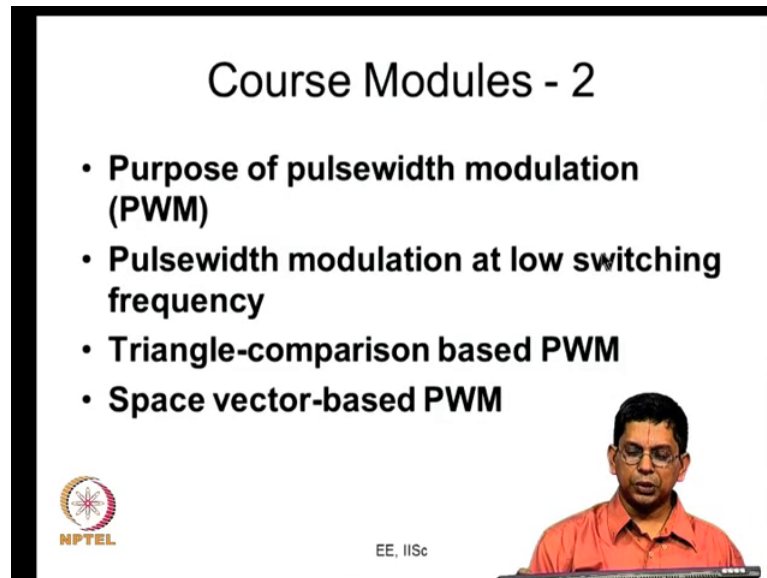
Lecture - 39
PWM for three-level neutral-point-clamped inverter – II

(Refer Slide Time: 00:37)



Welcome back to this lecture series on pulse width modulation for power electronic converters. We are looking at the last module of this lecture series and which is actually on pulse width modulation for multilevel converters basically three-level converters. So, we had this various course modules which we had covered earlier, this would be the first set of course, modules like a module one and module two which essentially covers certain basics of power electronics looked at dc-dc converters, dc, ac voltage source and current source inverters. And also you know looked at multilevel converters including neutral point clamped and flying cap capacitors and so on, and particularly neutral point clamped converters we were looking at. Then we were looking at applications of voltage source converters like motor drives and static reactive compensator active front-end converter and so on grid connected applications and the motor drive applications. So, this is on the first set of modules.

(Refer Slide Time: 01:22)



The slide is titled "Course Modules - 2" and contains a bulleted list of topics. In the bottom right corner, there is a small video inset of a man in an orange shirt speaking. The NPTEL logo is in the bottom left, and "EE, IISc" is in the bottom center.

Course Modules - 2

- **Purpose of pulsewidth modulation (PWM)**
- **Pulsewidth modulation at low switching frequency**
- **Triangle-comparison based PWM**
- **Space vector-based PWM**

NPTEL

EE, IISc

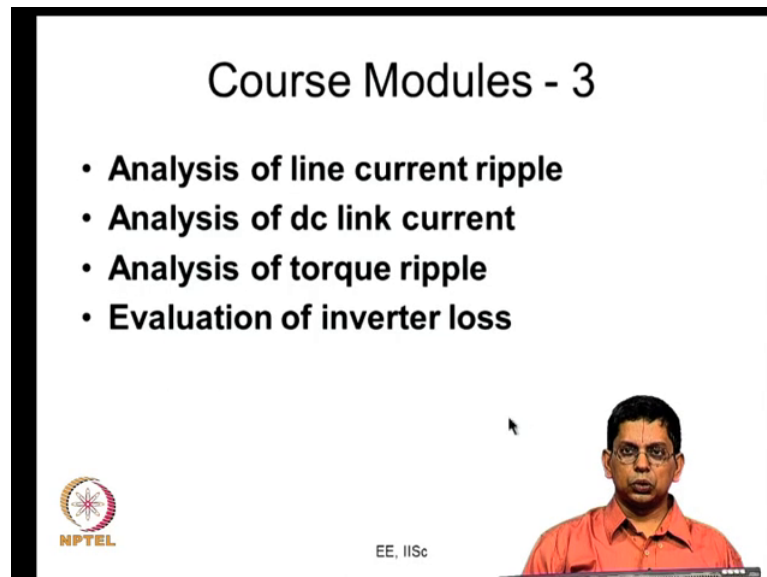
And subsequently we are looking at PWM generation in this second set of modules, we looked at certain basics of this PWM methods such as you know Fourier series waveform symmetries and the effect of waveform symmetries on the harmonic components. And then how you would generate PWM waveforms at low frequencies where you know you switch the inverter at only is there let say five times or seven times or nine times the fundamental frequency. And then how you do it when you are switching at a fairly higher frequency that is your fundamental frequency maybe several tens of times say 30 times or 40 times the fundamental frequency.

So, for example, if you have a motor drive and the maximum speed the maximum fundamental frequency is 50 hertz if you switching it at like 3 kilo hertz or 4 kilo hertz, the switching frequency is much higher than the carrier I mean modulation frequency. And in such cases you use this kind of triangle comparison space vector based PWM methods normally you know where you compare them with three phase modulating signals against a common triangular carrier.

Here you use the space vector approach instead of the three phase modulating signals, you have one revolving voltage space vector. You sample that every sub cycle and that gives you the voltage command and you try to realise that by applying the various vectors of the inverter for appropriate durations of time. And these two are equivalent to a large extent you know you can have continuous PWM methods or bus-clamping

PWM methods implemented through either of the approach, but there are certain advance bus-clamping PWM methods which are space vector method just we have observed on numerous occasions before. Thus we regard space vector based PWM to be more general than the triangle comparison PWM.

(Refer Slide Time: 03:05)



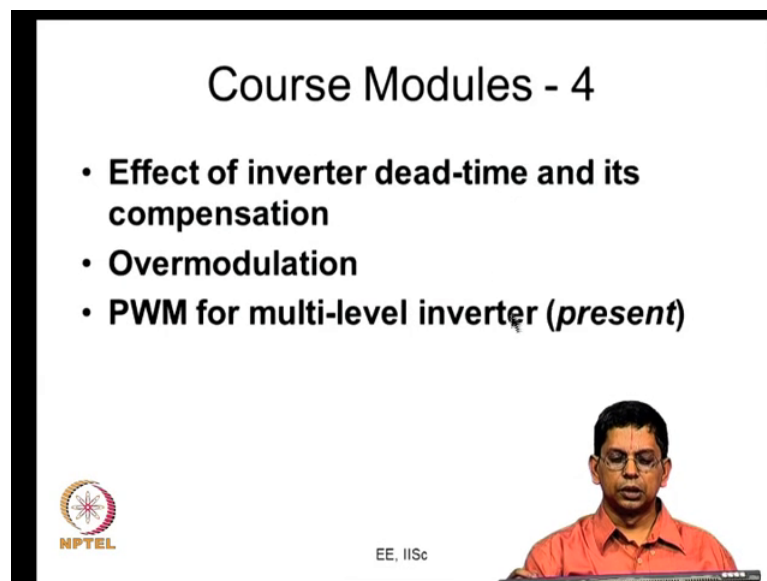
So, now this is all done in the context of two-level inverters. So, like the entire PWM generation in the context of two-level inverters, again there is this analysis in the context of two-level inverters. Here considering high switching frequency case, we try to see how to evaluate the current ripple the RMS, current ripple there and then how to look at the dc link current is something that we looked at and how to look at the torque ripple this is for low switching frequency high switching frequency cases. So, the principles are pretty similar. And here again evaluating inverter loss these were certain things we saw in the third set of modules. These are all again in the context of two-level inverters, but all these are extendable to three-level inverter also. This line current ripple is basically we do what we do is we integrate the error voltage or voltage ripple that is something that you can do in the three-level inverter also.

Now, you know except that the error voltage vector will be shorter here. So, the error voltage will be lower and because there are more number of vectors available your error was lower, and therefore, the line current ripple will be lower in a three-level inverter. And similarly like dc link current that the way you evaluated by multiplying the load

current and switching function of device, here also we can evaluate it in a similar fashion.

So, again torque ripple also in the current ripple part if you look at the q axis component alone you know which is orthogonal to the fundamental flux, then you would get a measure for of torque ripple. So, the basic principle are essentially the same. And the inverter losses it is a little different here, because you may have two devices conducting concurrently and your switching loss would be involved V_{dc} by 2. But you know the same ideas are still valid the switching loss you know you need to come up with the e on and e off of the devices and then you can certainly calculate them now. So, again these are all on the context of two-level inverters mostly they could actually be extended to three-level inverters.

(Refer Slide Time: 04:53)



Course Modules - 4

- **Effect of inverter dead-time and its compensation**
- **Overmodulation**
- **PWM for multi-level inverter (*present*)**

NPTEL

EE, IISc

The slide features a black border and a white background. At the bottom right, there is a small inset image of a man with glasses wearing an orange shirt, likely the speaker. The NPTEL logo is in the bottom left corner, and the text 'EE, IISc' is centered at the bottom.

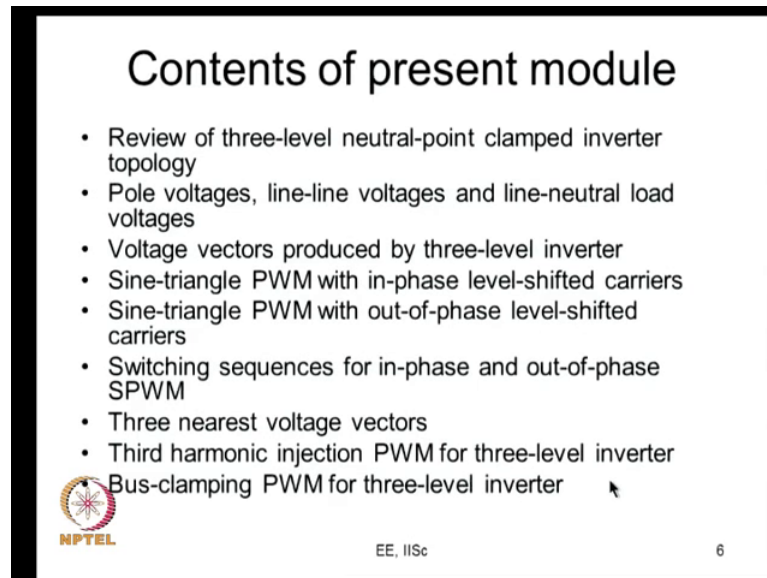
Then here we looked at certain advanced issues, for example, inverter dead time. So, because of the switching transition taking a considerable time, we introduce this dead time that is we are not switching the two devices in a leg exactly complimentary, we delay the incoming device after the outgoing device is been turned off the incoming devices turned on after some time delay t_d . So, that has its effect on the fundamental voltage and all that. So, this is their certain amount of nonlinearity gets introduced here. The reference voltage is no longer proportional to the I mean output is no longer proportional to the reference; of course, the ideal output is proportional to the reference

there is small error voltage that gets added up. And in this module, we try to see how much is that error and that is the error in the fundamental voltage and we also try to estimate the harmonics etcetera. We actually found that the error can be approximated the average error in a average door carrier cycles you could look at this effect of dead time as like a square wave for continuous PWM methods are some kind of quasi square waves so the discontinuous PWM methods.

So, what you can actually do to compensate for that is to add the inverse of this square to the modulating signal so that is a way to compensate for that. So, this is a certain kind of nonlinearity coming up there that is your modulating at a particular modulation index you are producing an output and that output is slightly different from what you want plus there are also low frequency distortion getting introducing that. Your modulation frequency maybe 40 hertz or 50 hertz let say 50 hertz is this also introduces low frequency distortions like you know 250 hertz or 350 hertz in the inverter output, so that is something about dead time. And over modulation is where you want to go from linear modulation all the way till six step mode to increase the dc bus utilization from 90.7 percent of six step voltage to 100 percent of six step voltage. So, we looked at this from the triangle comparison and space vector point of views.


Well all these are also extendable these ideas are extendable to three-level inverter, what we would essentially be doing in this few lectures is to look at these. We look at these like this particular is the triangle comparison and the space vector PWM we would like to see how exactly we can extend that. In the last lecture we looked at extending sine triangle PWM particularly to the three-level inverter. And we would look more about it now. And today we will also discuss how do we do it from the you know in the space vector based approach produced PWM. And probably the next lecture we would focus on some aspects of this analysis how you would analyse the line current ripple and as a consequence how could you could possibly design some hybrid PWM techniques as we did in this particular module for two-level inverters now.

(Refer Slide Time: 07:35)



Contents of present module

- Review of three-level neutral-point clamped inverter topology
- Pole voltages, line-line voltages and line-neutral load voltages
- Voltage vectors produced by three-level inverter
- Sine-triangle PWM with in-phase level-shifted carriers
- Sine-triangle PWM with out-of-phase level-shifted carriers
- Switching sequences for in-phase and out-of-phase SPWM
- Three nearest voltage vectors
- Third harmonic injection PWM for three-level inverter
- Bus-clamping PWM for three-level inverter

 NPTEL

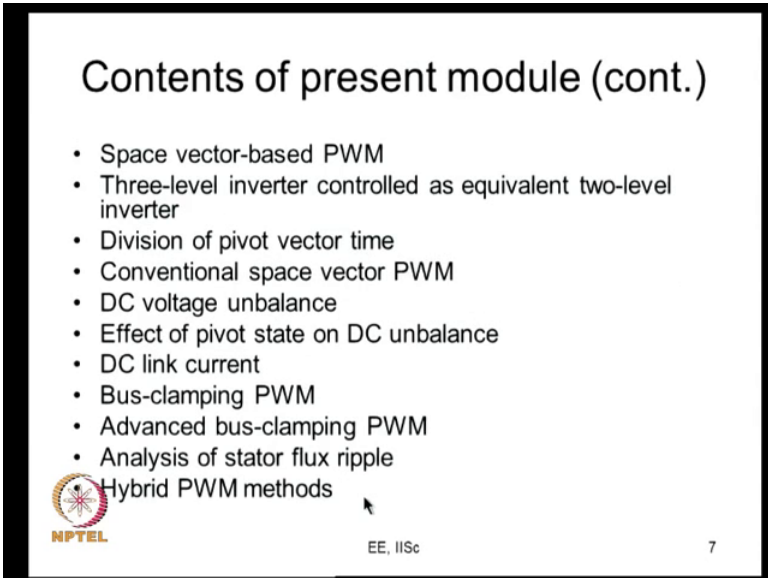
EE, IISc 6

So, let us get going with this present module. So, in the present module which would comprise of three lectures, this being second lecture. We would look at mean we would be reviewing the topology neutral point clamped inverter topology. Actually we did it in the last lecture and we also looked at the definitions of pole voltages, line to line voltages, line to neutral voltages and the mathematical equations relating them. And we looked at the inverter states there are about three multiple 3 to the power 3 - 27 inverter states produced by the three-level inverter and they produce 19 distinct voltage vectors. So, we looked at those and then we looked at sine triangle PWM with you know two-level-shifted carriers who could be in phase or there could be you know with some phase difference or out of phase etcetera.

And we ended up the last lecture just beginning to discuss about the switching sequences for in phase and out of phase PWM. In fact, I had asked you to look at this as a home exercise just try to find out how you know consider some particular switching cycle and see what kind of switching sequence you would get with in phase and out of phase are they different in what sense it is different. Anyway we will do it today. And we would look at this three nearest voltage vectors for any given reference vector. So, in most of the PWM methods, what we do is like in two-level inverter you have a reference vector we applied two active vectors one on the clockwise side, one on the anti clockwise side and one null vector. Here we have more options available.


What we do is we choose the so called three nearest voltage vectors, and we synthesise the average vector by time averaging. And what happens is when you use sine triangle PWM with in phase it automatically chooses the three nearest voltage vectors that something we will see today. And you know it is not this sine triangle sine triangle PWM sine three phase sinusoid, you can compare with two-level-shifted in phase carriers. Then you know instead of sine wave you can also add common mode. For example, you can third harmonic to the sine and you can have the those three phase modulating waveform with common mode added compared against these level-shifted carriers and you can do this. And instead of three or third harmonic injection you can also go for bus-clamping PWM which we did in the context of two-level inverter now we can do it in the context of three-level inverter. So, these are certain things you would focus on today.

(Refer Slide Time: 09:52)



Contents of present module (cont.)

- Space vector-based PWM
- Three-level inverter controlled as equivalent two-level inverter
- Division of pivot vector time
- Conventional space vector PWM
- DC voltage unbalance
- Effect of pivot state on DC unbalance
- DC link current
- Bus-clamping PWM
- Advanced bus-clamping PWM
- Analysis of stator flux ripple
- Hybrid PWM methods

 EE, IISc 7

And we would possibly try and look at how do we do space vector based PWM, and how you know does some difficulties that we might have in doing space vector based PWM, it is really an extension of what we did in the two-level case. But here three-level case the number of vectors are more and you know the choice of vectors is higher and so you have certain issues coming up you will see how they can be addressed. And one way to address them would be to look at a three-level inverter as an equivalent two-level inverter in every extent of the fundamental cycle. If you have fundamental cycle divided into six parts I mean six portions you call each of them as a hextant a sector. So, in each

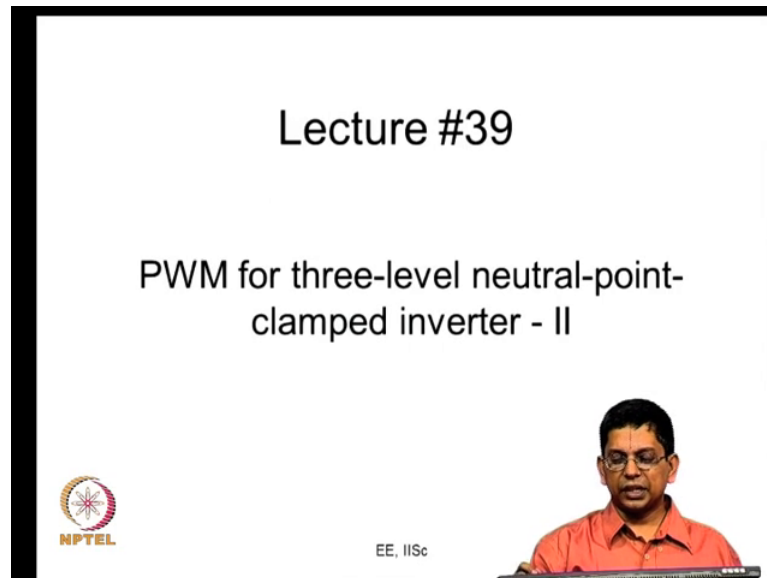
hextant you can see that the three-level inverter can be viewed as an equivalent two-level inverter.

And then you would see further issues on what exactly comes out of that and you know pivot vector which is said to be defined how do you do this conventional space vector PWM. And there is one other issue that you would have is dc voltage unbalance we may not have a very long discussion on that, but we will briefly see why there is a dc voltage unbalance in the context of three-level inverter and how that could possibly be handled all right.

So, again dc link current we would quickly look at how we can extend our knowledge of you know calculation of dc link current for two-level to three-level case. So, we will look at this bus-clamping PWM and all that from now the space vector point of view. And importantly we would look at this advanced bus-clamping PWM. What we did for two-level, we will try and see how that can be done for three-level inverter. And we will get started with you know have some very preliminary discussions on how we can analyse the line current ripple using this idea stator flux ripple, and how we keep possible for us to implement some I mean to design some hybrid PWM method. So, this would be the content of this module.

And as I mentioned today you know the focus today would be on the switching sequences and this other third harmonic injection bus-clamping etcetera after somewhere here on how you could possibly control a three-level inverter as an equivalent two-level inverter. And the remaining portions would be more or less dealt within the next lecture now.

(Refer Slide Time: 11:57)



Lecture #39

PWM for three-level neutral-point-clamped inverter - II

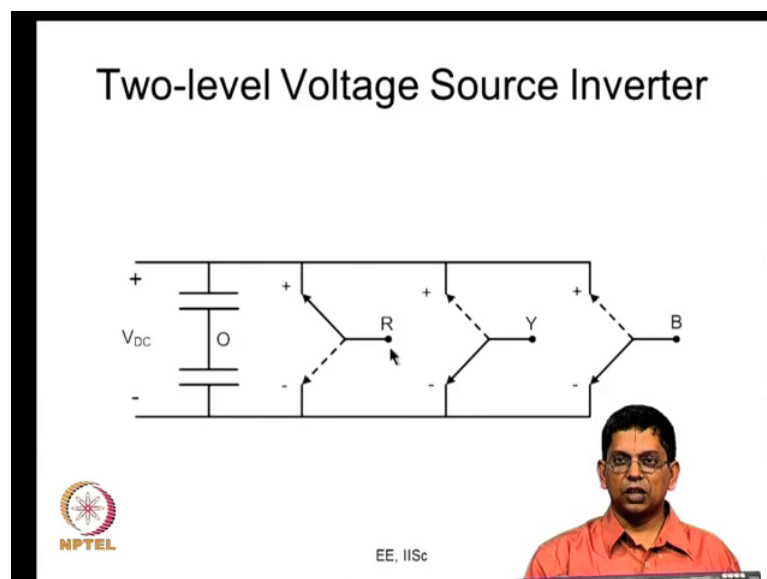
NPTEL

EE, IISc

The slide features a black border and a white background. At the top center, the text 'Lecture #39' is displayed in a large, black, sans-serif font. Below it, the title 'PWM for three-level neutral-point-clamped inverter - II' is centered in a smaller, black, sans-serif font. In the bottom left corner, there is a circular logo for NPTEL (National Programme on Technology Enhanced Learning) with the text 'NPTEL' underneath. In the bottom center, the text 'EE, IISc' is visible. On the right side, there is a small inset image of a man with glasses and a red shirt, who appears to be the speaker for this lecture.

So, this is the second lecture in this module is the lecture 38 of the forty lecture series, second lecture in the thirteenth module we would call this PWM for three-level neutral point clamped inverter two.

(Refer Slide Time: 12:09)



Two-level Voltage Source Inverter

V_{DC}

R Y B

NPTEL

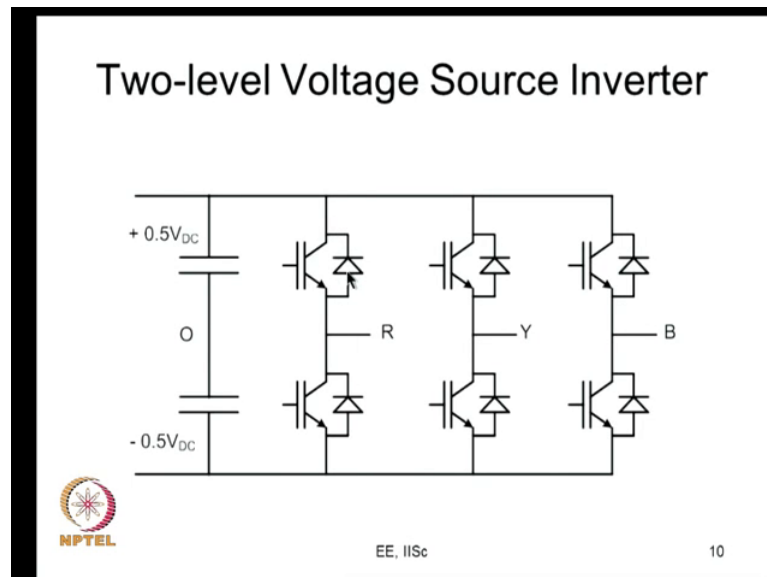
EE, IISc

The slide features a black border and a white background. At the top center, the title 'Two-level Voltage Source Inverter' is displayed in a large, black, sans-serif font. Below the title is a circuit diagram of a two-level voltage source inverter. It shows a DC source V_{DC} on the left, represented by two cells in series with '+' and '-' terminals. The positive terminal is connected to the top of three half-bridge legs. The negative terminal is connected to the bottom of the same three legs. Each leg consists of two MOSFETs in a half-bridge configuration. The output terminals are labeled R, Y, and B. The output lines are shown as solid lines for R and Y, and dashed lines for B. In the bottom left corner, there is a circular logo for NPTEL with the text 'NPTEL' underneath. In the bottom center, the text 'EE, IISc' is visible. On the right side, there is a small inset image of the same man with glasses and a red shirt as in the previous slide.

So, voltage source inverter. So, you have three phase load the load is presumed to be inductive. So, you see that these are all poles. So, they are you know the load terminals are connected to the poles of the switch, so that the inductive circuit would not get opened out and then the throws you have the dc voltage connected across the throws. So,

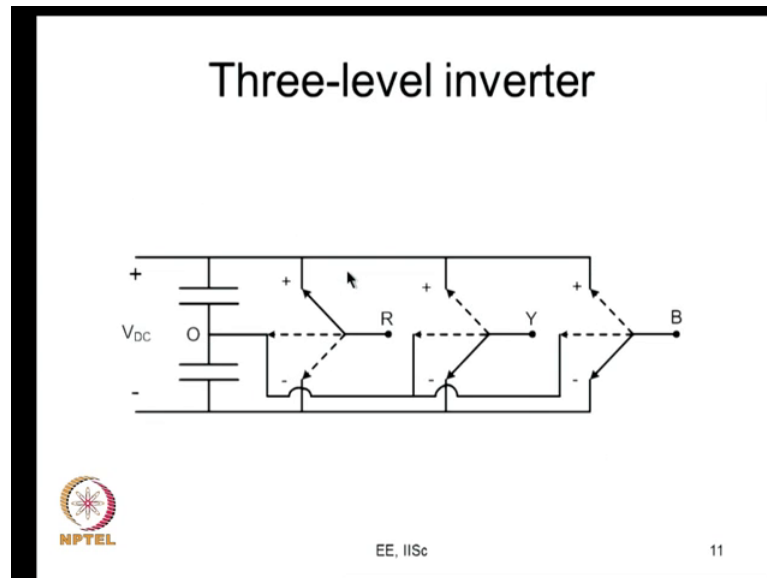
you have that and you know you switch and this is how you really connect that you have a capability of connecting the pole either two plus V_{dc} by 2 or minus V_{dc} by 2 to the top or bottom here. So, it is possible for you to apply alternating voltages here, and you know you do this as on inverter here.

(Refer Slide Time: 12:51)



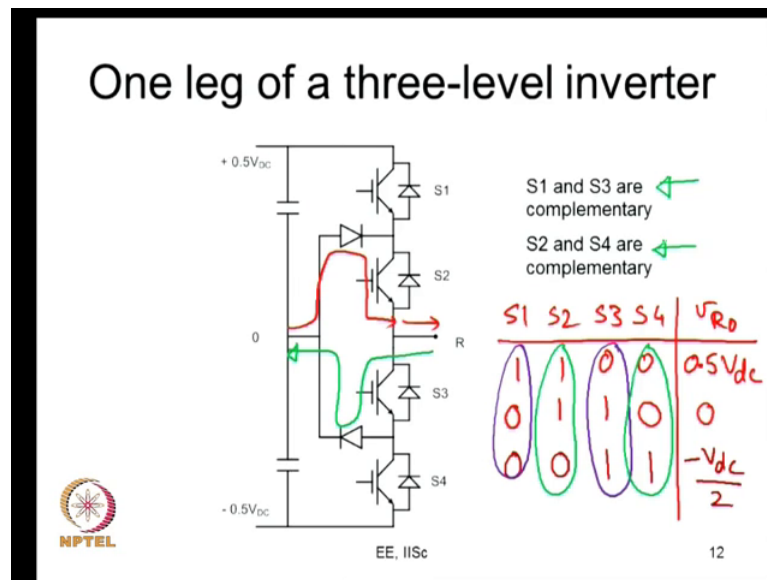
One thing that we realised here was you know this is for dc-ac conversion, where you single pole double through switches. You know three-level so and this is how they are actually electronically realised you have two transistors and you know each transistor has an antiparallel diode, it can conduct in both the directions and it can block voltage with the particular polarity

(Refer Slide Time: 13:02)



So, we realise that we could also use a single pole triple throw switch. In fact, we can have single pole and n number of throws 5 throws, 6 throws etcetera where each throw is connected certain voltage level. So, now, there is an intermediate voltage level plus V_{dc} by 2 minus V_{dc} by 2 in between there is 0, this actually helps us in maintaining better waveform quality as we saw before. So, we can you know for example, the instantaneous voltage earlier could only be plus V_{dc} by 2 and minus V_{dc} by 2, now it could be 0 also. So, earlier the v_{RY} the potential between these two can only be plus V_{dc} or minus V_{dc} or 0, now, it can be plus or minus V_{dc} or plus or minus V_{dc} by 2 or can be 0. So, it gives you better choice and you know if the output waveform has a chance of following the desired sinusoidal output more closely so that is what it leads to.

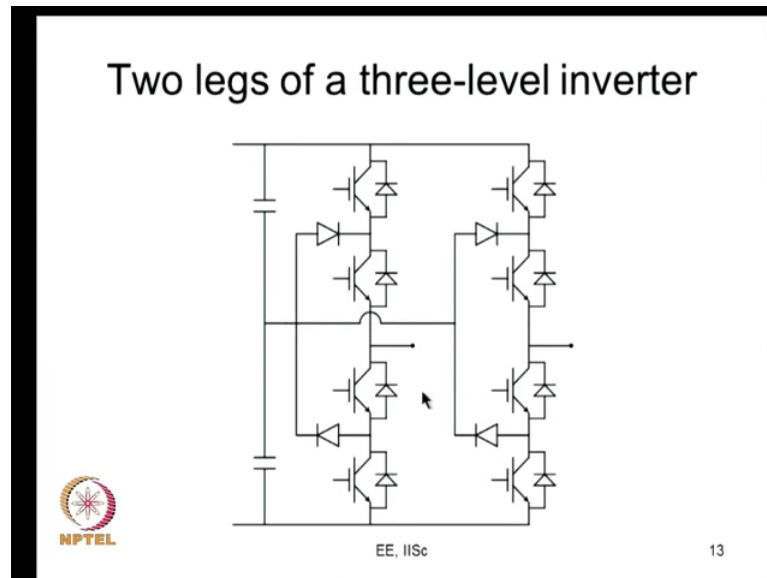
(Refer Slide Time: 13:54)



So, this is how we realise a single pole triple throw switch we discussed this in a lecture hour two earlier in the first module. So, this pole to the top throw these two switches are on we found that it is going to be that. I also did this in the last class I am not sure if that is required now in any case. If I have my S 1, S 2, S 3, S 4 and this is v_{RO} , if I have my S 1 and S 2 on, S 3 and S 4 are off then I will have v_{RO} will be equal to $0.5 V_{dc}$. On the other hand, if I have S 1 is off the outermost device is off, here also S 4 is off, S 2 and S 3 are on then I will have 0.

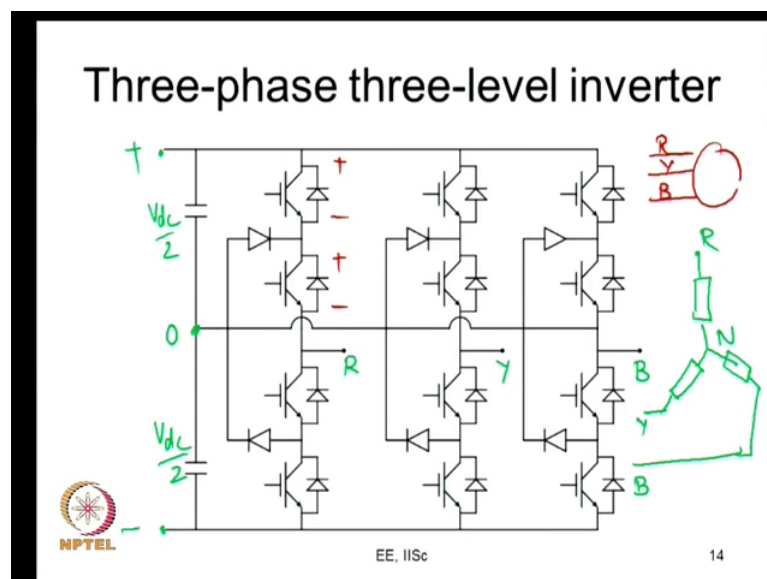
So, in this case as I mentioned to you the current is in this direction, the current would flow like this. On the other hand, if the current is in a different direction then it would flow like this. So, if the S 3 and S 4 are off, S 1 and S 2 are on, then you are going to get minus V_{dc} by 2, these are the three different pole voltages. And you can very easily understand or quickly realise that this and this are complementary. The same way you can see this I am sorry let me change that this and this are complementary that is what we have said here S 1 and S 3 are complementary and S 2 and S 4 are complementary. So, you need two independent signals, earlier we needed only one signal in the case of two-level inverter here we needed two in a two signals here.

(Refer Slide Time: 15:56)



And this is where I have just showing two legs connected this is you can probably consider it as a single phase three-level inverter where you know you can connect a single phase load here just I have shown two legs here.

(Refer Slide Time: 16:10)



Now, here I have shown all the three legs. So, this is what is really your three phase three-level inverter, which is what we are considering now. So, this is the load terminal R this is the load terminal Y this is the load terminal B and this is the dc midpoint o this is the dc positive this is negative you have a voltage of V_{dc} by 2 here you have a voltage

of V_{dc} by 2. So, we presume the load is something like this load is R Y B and the load has a certain neutral which is not electrically connected anywhere this is what we understand now. So, this is you know apart from the idea of single pole triple throw switch it can give you there are more number of voltages are possible at the pole and therefore, waveform quality is better.

Now, when you really want to block this voltage V_{dc} , now you have two different devices available to block this. So, in some sense, this is like this series connected IGBTs, but in the case of series connected IGBTs you know the voltage sharing we will have to be ensured, there could be parasitic, there could be other things spread in the characteristics of this devices which may you know may not lead to equal sharing of voltage. This may be little more this may be little less etcetera, but here it has there is one advantage which also like as I have pointed to before now.

For example, let us say this voltage that is these two are off, I mean these two are off, so they are blocking some voltage. And you know let us say this voltage is greater than $0.5 V_{dc}$ if it becomes greater than $0.5 V_{dc}$ what will happen this will dip below 0 then this will come into conduction. So, this clamping diode make sure that when they are sharing the voltage across this is really no more than V_{dc} by 2. So, it partly solves the problem of voltage sharing and that is one of the advantages that we have here. And now so you can handle for example, you know by through two devices the voltage blocking capability. So, if you have two devices you know your voltage rating of some rating v . So, it is as good as having our device of voltage rating $2v$. So, you can actually realise higher inverter with higher dc bus voltage. So, one area where they are actually applied this three-level inverter are so called medium voltage drives that is when you have motor drives.

Now let us say this three phase load I have just shown it like a passive load it actually be an induction motor. So, you know it could really be an induction motor connected like this R, Y and B. So, here you would normally have motors there is some voltage rating. So, in India the motor rating the voltage ratings of motors are typically like 400, 415 or 440 volts 50 hertz that is what you have a maybe you know in some other places you will have 110 volts 60 hertz or 208 volts 60 hertz and some you know depends on the standards in different places. So, this the voltage rating is typically 100 of volts.

Now, let us say it is about 440 volts; you will need a dc bus voltage the dc bus voltage may be like 700 volts. So, many a times in the Indian condition you will need you know for this 400 volts systems you may need something like 600 volt to 750 volt not really more than 800 volt and you handle them using a voltage source inverter with the device I mean two-level inverters device rating maybe 1200 volt. Now, you may have these motors which are rated a few kilo volts. So, if it is rated hundreds of volts you call them as low voltage motor if it is rated in kilovolts like 1.1 kv, 2.2 k v etcetera you call them as medium voltage motor drives.

So, for such medium voltage motor drives this becomes a very good option because you may you have lot of 1200 volt devices available 1700 volt devices may be available. Of course, there are devices of higher ratings available maybe up to 3.3 k v which are called high voltage IGBTs and all that, but they become rare or you know or they may be more expensive compared to the voltage ratings of this now. So, this allows you for example, to use to 1.2 k v devices. So, you can use 1.2 k v device 1200 volt devices now like. So, with a 1200 volt devices, you get you know the advantage as though you are using 2400 volt devices are being available to you. So, you know your dc bus voltage need not be 800 volts your dc bus voltage could be 1500 or 1600 volts. So, that is possible with three-level inverter that is one of the reasons why it I mean it is actually one of the major applications of three-level inverter this is the medium voltage motor drive.

(Refer Slide Time: 21:06)


Instantaneous pole voltages, line-line voltages and line-neutral load voltages

$$v_{RO} = 0, \pm \frac{V_{dc}}{2}; v_{YO} = 0, \pm \frac{V_{dc}}{2}; v_{BO} = 0, \pm \frac{V_{dc}}{2}$$

$$v_{RY} = v_{RO} - v_{YO}; v_{RN} = (v_{RY} - v_{BR}) / 3$$

$$v_{RY} = \pm V_{dc}, \pm \frac{V_{dc}}{2}, 0$$

$$v_{RN} = \pm \frac{2V_{dc}}{3}, \pm \frac{V_{dc}}{2}, \pm \frac{V_{dc}}{3}, \pm \frac{V_{dc}}{6}, 0$$


EE, IISc
15

So, here what we have is. So, you can also use it in the low voltage conditions. So, that is what I was mentioning yesterday when I was saying this it has the advantage of medium voltage drives because you know it uses two devices to block certain dc bus voltage and when it is switching you can see that each switch each switch handles a voltage of V_{dc} by 2 only as against V_{dc} . So, sometime in the low voltage applications also like for example, you know certain grid connected applications it becomes advantages because this switching loss tends to be a little lower than the two-level inverter.

So, some studies have been made in the literature where you also find you may find some papers and comparison of two-level inverters, and three-level inverters and so. One of the thing it shows up is you know in the low voltage applications also three-level inverters are applicable their advantage is compared to two-level inverters particularly when the switching frequencies are high. Because they are able to reduce the switching losses and give certain advantages in terms of the overall losses that is one of the advantages. Because they produce better wave form quality the filtering requirements is slow that is another advantage all right.

So, even we look at this let us look at the equations pertaining to that this is the instantaneous voltage as I mentioned it can be plus or minus V_{dc} by 2 only for two-level inverter now it can be 0 also. So, v_{YO} v_{BO} , so v_{RO} is v_{RO} minus v_{RY} is v_{RO} minus v_{YO} as in the case of two-level inverter. Again v_{RN} is one-third of v_{RY} minus v_{BR} as in the case of two-level inverter here we assume a balanced three phase load. So, because of this additional 0, your v_{RY} is you know you also have this plus minus V_{dc} by 2 possible. In the case of two-level inverter, your possible values of v_{RY} are plus minus V_{dc} and 0, here it is plus minus V_{dc} by 2 also possible then you have v_{RN} .

So, what happens is plus or minus $2 V_{dc}$ by 3, this is what is possible with two-level inverter and also plus or minus V_{dc} by 3 or and 0, these are possible with two-level inverter now you have this V_{dc} by 2 also and plus or minus V_{dc} by 6. So, these are certain additional voltage levels that become possible because of your additional connection your you know the third point that is the available your ability to connect the load terminal to the dc midpoint using this options now.

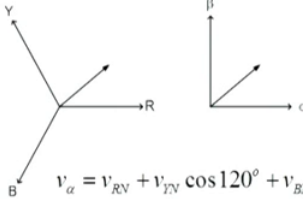
So, the other thing as I mentioned yesterday is for example, if you want two V_{dc} by three there is only one possibility or let us say V_{dc} there is only one possibility v_{RO} has

to be plus V_{dc} by 2 v_{YO} has to be minus V_{dc} by 2. But if you are looking at plus V_{dc} by 2 v_{RY} is equal to plus V_{dc} by 2. There are two possibilities one is v_{RO} can be plus V_{dc} by 2 v_{RY} can be 0 or v_{RO} can be 0 and v_{YO} can be minus V_{dc} by 2. So, this have two possibilities here. Here you will have multiple possibilities to come up with that. So, for getting v_{RY} equal to 0, both v_{RO} and v_{YO} could be equal to plus V_{dc} by 2 or both v_{RO} and v_{YO} could be equal to 0 or both v_{RO} and v_{YO} could be equal to minus V_{dc} by 2.

So, when you come to the lower you know lower and lower voltage levels you see that that can be realised through many switching states through a number of more number of switching states and this possibility are the ones that give you many ways of designing PWM methods and so on and so forth.

(Refer Slide Time: 24:29)


Space vector transformation of three-phase voltages



$$v_\alpha = v_{RN} + v_{YN} \cos 120^\circ + v_{BN} \cos 240^\circ = \frac{3}{2} v_{RN}$$

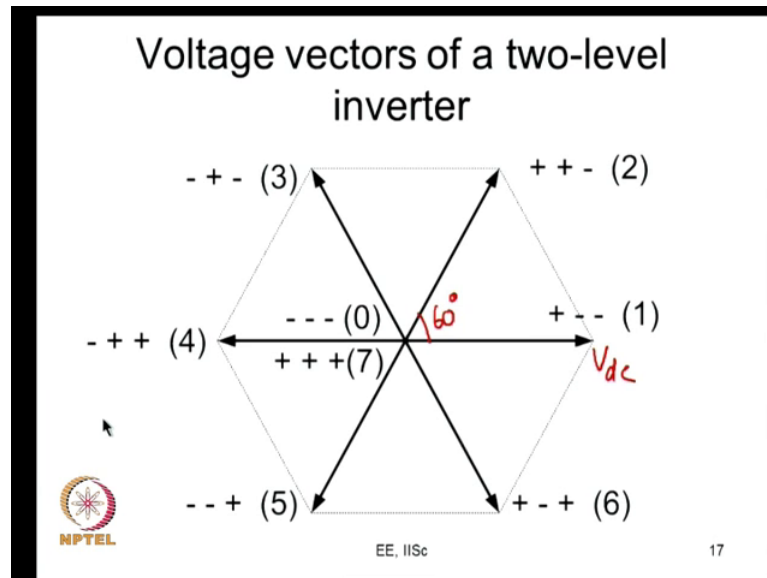
$$v_\beta = v_{YN} \cos 30^\circ + v_{BN} \cos 150^\circ = \frac{\sqrt{3}}{2} (v_{YN} - v_{BN})$$

$$v_{RN} + v_{YN} + v_{BN} = 0 \quad (\text{Balanced star connected load})$$


EE, IISc
16

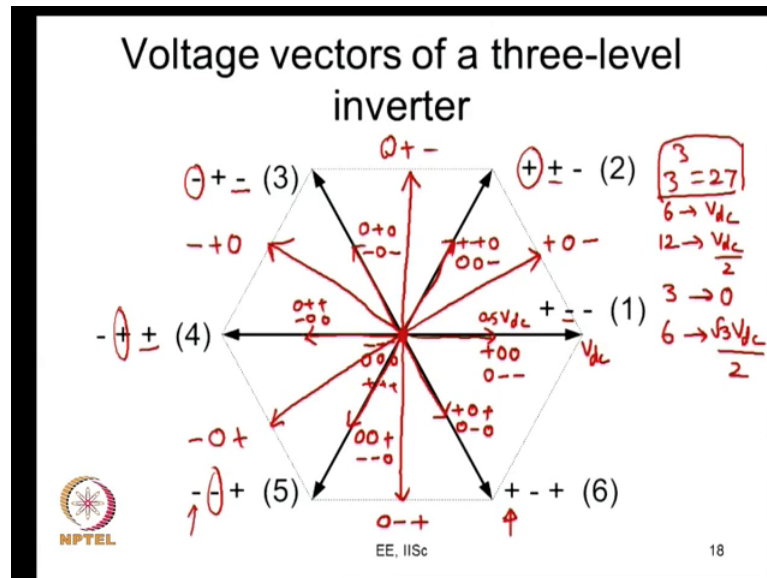
So, this three phase pole voltages I mean three phases line to neutral voltages v_{RN} v_{YN} and v_{BN} they satisfy the condition $v_{RN} + v_{YN} + v_{BN} = 0$. So, they are not three independent quantities they can be represented in terms of two independent are orthogonal quantities which are called v_α and v_β . And you can arrive at v_α and v_β from these by saying v_R v_α is $v_{RN} \cos 0 + v_{YN} \cos 120 + v_{BN} \cos 240$ and that would be equal to $\frac{3}{2} v_{RN}$. Then you can say v_β is equal to $v_{RN} \sin 0 + v_{YN} \sin 120 + v_{BN} \sin 240$ and that turns out to be $\frac{\sqrt{3}}{2} (v_{YN} - v_{BN})$ this is the three phase to two phase transmission.

(Refer Slide Time: 25:14)



So, when you do this you would get that for a two-level inverter. So, these are the you know the two-level inverter has eight inverter states there are each leg the top can be on or button can be on there are three legs. So, two to the power three eight inverter states we designate them as 0, 1, 2, 3, 4, 5, 6. So, now, 0 and seven res correspond to what are called 0 states minus minus minus meaning all the top bottom devices are on here all the top devices are on in both cases the load is shorted and therefore, the output voltages are 0 the voltage vector is 0 in all the other cases there is some transfer power between the active between the dc side of the ac side. So, you have it like this. So, you have these were your six active vectors all of them are of length V_{dc} that is given our conventions the length is V_{dc} and this angle is 60 degrees. So, the way we arrived at this voltage vectors for two-level inverter this same wave we can arrive at the voltage vectors for three-level inverter.

(Refer Slide Time: 26:16)



As we discussed yesterday and which we can quickly again do today. So, we have accounted for there are 3 to the power 3 is equal to 27 inverter states out of 27 inverter states we have accounted for six inverter states. These lead to voltage vectors of length V_{dc} these vectors are identical to what is there then you will have three vectors I mean three inverter states minus minus minus, 0 0 0, and plus plus plus all these lead to a null vector. So, instead of two at two 0 states in two-level inverter you have three 0 states now all the three you know pairs of top switches are on or bottom switches are on or the three pairs of middle switches are on. So, these are three things now

So, let us take the other combinations. Let us say you take plus 0 0, now plus 0 0 is very similar to plus minus minus, you can see lot of similarity here. Whereas, in plus minus minus, plus minus minus, your voltages are you know line to line voltages are V_{dc} 0, and minus V_{dc} would be the line to line voltages here it is V_{dc} by 2 0 and minus V_{dc} by 2 are the line to line voltages. So, it is similar except V_{dc} getting reduced to V_{dc} by 2 the line to line voltages getting reduced to V_{dc} by 2 rather than V_{dc} . And therefore, what happens this produces voltage vector of magnitude $0.5 V_{dc}$.

Now, if you take the other state for example, 0 minus minus, this also produces the same set of output voltages the line to line voltages has plus 0 0. So, you can see that these two states produce a vector of magnitude $0.5 V_{dc}$ and they are aligned with this vector plus minus minus corresponding plus minus minus the same way you can look at the inverter

states plus plus 0 or 0 0 minus. So, they all produce three phase voltages or line to line voltages, similar to this vector here you know the line to line voltages could be plus V_{dc} one will be plus V_{dc} and minus V_{dc} . Here the line to line voltages will be plus V_{dc} by 2 minus V_{dc} by 2 and 0 that would be the difference. Now, the same way you can find out you can see that there are other two vectors which are 0 plus 0 and minus 0 minus.

Similarly, you will have two of the states producing a vector equivalent to $0.5 V_{dc}$ in this direction they are 0 plus plus minus 0 0 again this is something similar you have 0 0 plus and minus minus 0 leading to vectors of 0.5 here you have plus 0 plus 0 minus 0 these would be the vectors now. So, now, how many vectors have been accounted for you have accounted for another 12 more states? So, these twelve more states lead to six distinct active vectors of length $0.5 V_{dc}$.

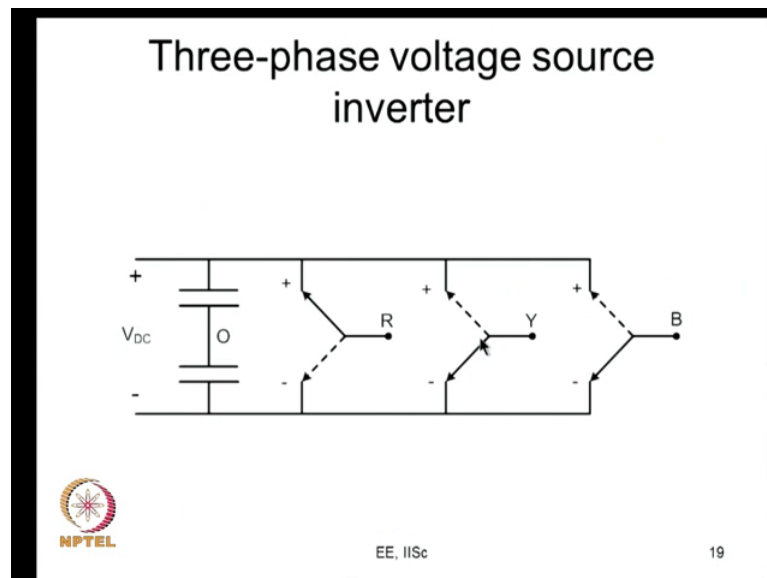
So, let us just say. So, this twelve inverter states lead to vectors of length V_{dc} by 2 and three of them lead to 0. So, you have now accounted for 21 out of this three power three is equal to 27 states 21 have been accounted for there are six other states which are combinations of plus 0 and minus in which one phase one pole voltage will be v_{RO} , V_{dc} by 2. Another one will be zero, and the third one will be minus V_{dc} by 2 such combinations are the ones that are missing. So, those things as we quickly discussed I mean as we discussed yesterday you can see that if this is you here you see it is minus to plus there is a transition.

So, you consider plus 0 minus. And if you look at this, this will be actually be producing a vector which is like this. And similarly you see that this is minus and this is plus here. So, you look at 0 plus minus that would actually producing a vector like this and here you see minus minus minus is the transition minus plus minus to. So, the transition here is here. So, in between you have minus plus 0 look at minus plus 0 would be like this would produce a vector like that and here what switches it is plus and here it is minus it is the Y phase that is switching. So, you consider minus 0 plus and that will be producing a vector like this. And here once again you have minus minus plus switching to plus minus plus. So, in between you have 0 minus plus and that produces a vector like this. So, you see that you have six more vectors and these vectors you know these actives these active state produce active vectors of lengths $\sqrt{3} V_{dc}$ by 2. So, thus you can see that there are totally 21 plus 6 - 27 states have been accounted for.

So, these states which produce you know vectors of length V_{dc} there are unique states. So, this six unique states produce six unique active vectors of you know length V_{dc} . And if you look at the output line to line output voltages their line to line output voltage be plus V_{dc} 0 and minus V_{dc} , there are six other states which produce you know six vectors of length $0.866 V_{dc}$. If you look at there a line to line voltages it will be plus V_{dc} minus V_{dc} by 2 minus V_{dc} by 2 or minus V_{dc} plus V_{dc} by 2 plus V_{dc} by 2 would be there line to line voltages. So, those are this inverter states now.

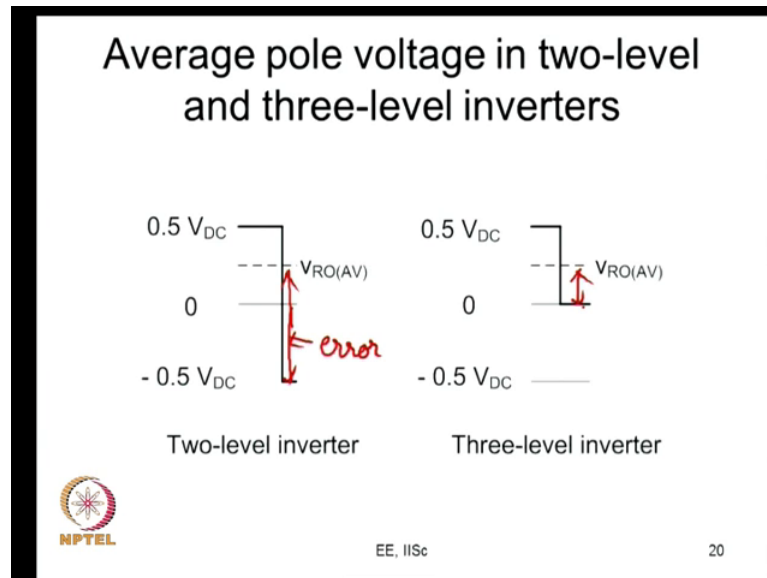
So, these twelve vectors you know their tips are sitting on this these six vectors form a hexagon and the remaining six vectors touch the midpoints of these sides of the hexagon. So, these twelve vectors tip the lie on this hexagon, and there are the other twelve states produce six vectors which lie inside in a in a hexagon. So, this is just for us to get a clearer picture. So, it is the same idea you know you have the pole voltages and additional possibility that instead of plus V_{dc} by 2 minus V_{dc} by 2. It can be 0 also otherwise you know it is a same way we would evaluate v_{RY} v_{RN} and v_{α} v_{β} and so on and this is how we come up the voltage vectors of a three-level inverter.

(Refer Slide Time: 32:42)



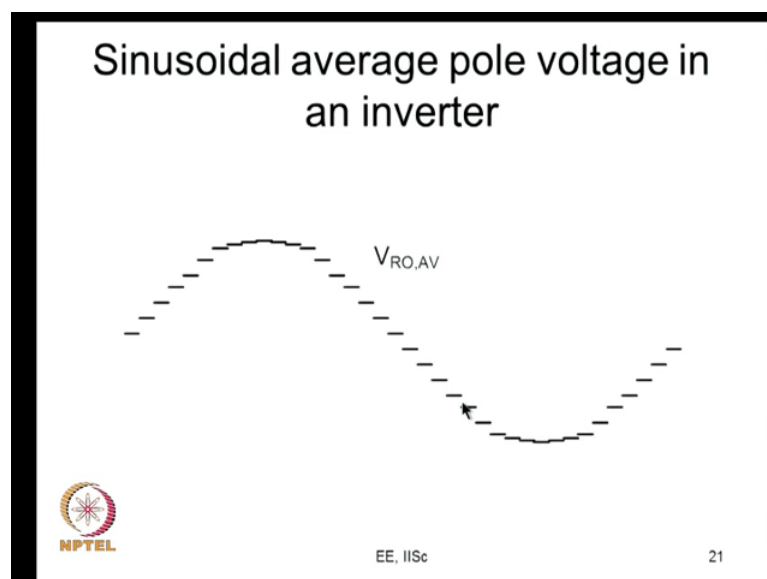
So, this is now if you look at a three phase voltage source inverter you have v_R , v_Y and v_B .

(Refer Slide Time: 32:48)



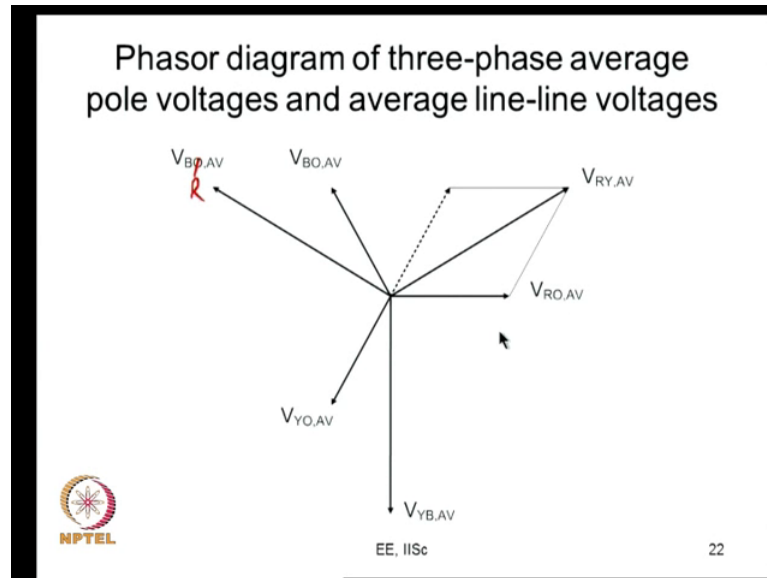
Now, you want an average output voltage in a particular sub cycle this is a small duration of time. So, in a in a two-level inverter you need this average you are going to apply $0.5 V_{dc}$ for some time and minus $0.5 V_{dc}$ for remaining time and realise that whereas, here you are going to apply $0.5 V_{dc}$ and 0 to realise the same average voltage. So, as I mentioned yesterday here you see that the error is very high this is your error between the desired output voltage. And the actual output voltage, but here you see that the instantaneous error is lower. And therefore, this leads to this indicates lower harmonic content in the voltage and that would also result in lower harmonic content in the current.

(Refer Slide Time: 33:33)



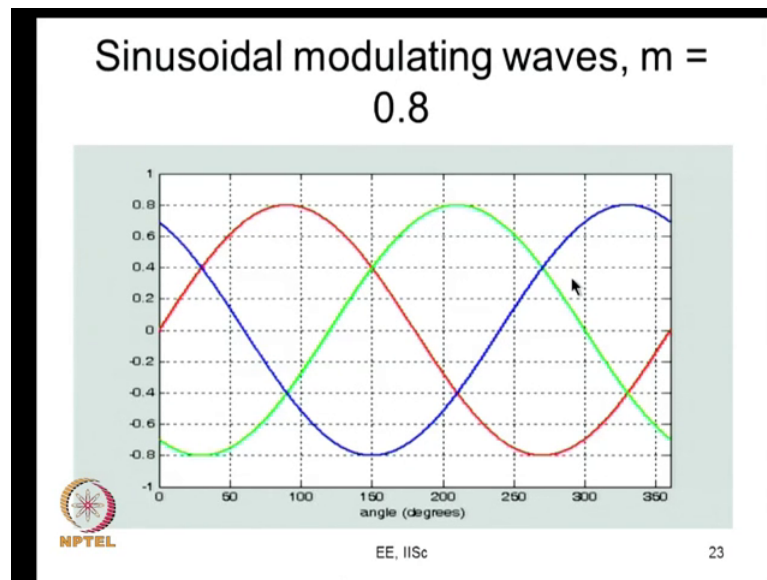
So, in both the cases whether two-level or three-level you want the R o average to vary like a sinusoid when you are doing sine triangle PWM. So, you can vary this sinusoidally.

(Refer Slide Time: 33:44)



And if you can vary v_{RO} sinusoidally v_{YO} and v_{BO} sinusoidally you vary the sinusoidally, then v_{RO} minus v_{YO} average would be v_{RY} average which will be sinusoidal. Again v_{YO} minus v_{BO} average will be v_{YB} average again v_{BO} average minus v_{RO} average will be v_{BR} average. So, you can get balanced sinusoidal voltages in the line to line if you produce balanced three phase average pole voltages.

(Refer Slide Time: 34:19)



So, this is what we do using sine triangle PWM we use modulating signals which are balanced three phase sinusoids and compare them with a triangular carrier. So, this is true for both two-level as well as three-level inverter.

(Refer Slide Time: 34:30)

Average voltages in a three-phase inverter with sinusoidal modulation

$$m_R = V_m \sin(\omega t); m_Y = V_m \sin(\omega t - 120^\circ); m_B = V_m \sin(\omega t - 240^\circ)$$

$$v_{RO(AV)} = \frac{m_R V_{dc}}{V_p} \frac{1}{2}; v_{YO(AV)} = \frac{m_Y V_{dc}}{V_p} \frac{1}{2}; v_{BO(AV)} = \frac{m_B V_{dc}}{V_p} \frac{1}{2}$$

$$v_{RY(AV)} = v_{RO(AV)} - v_{YO(AV)}$$

$$v_{RN(AV)} = (v_{RY(AV)} - v_{BR(AV)}) / 3$$

$$v_{RN(AV)} = \frac{V_m \sin(\omega t) V_{dc}}{V_p} \frac{1}{2} = v_{RO(AV)}$$

But the way we need to switch the number the carriers there will be different now. So, if you do the sinusoidal modulation these are the three phase modulating signals the average pole voltages would be replica of the modulating signals there will be the scaled versions of that. So, this is really the you know what you can regard as the normalized

modulating signal multiplied by V dc by 2 that would be your average pole voltage. So, you will have three phase average pole voltages which will be sinusoidal. And then you subtract the two it to get one line to line voltage similarly you get your v YB average and v B R average. And you also get your v RN average which will this is forms this you know which is given by this equation. Similarly, you will have v YN average as v YB average minus v RY average v BN average would be v B R average minus v YB average upon three you know divided by 3. And you will see for sinusoidal modulation v RN average is equal to v RO average.

(Refer Slide Time: 35:22)

Average voltages in a three-phase inverter with common-mode injection


$$m_R = V_m \sin(\omega t); m_Y = V_m \sin(\omega t - 120^\circ); m_B = V_m \sin(\omega t - 240^\circ)$$

$$m_R^* = m_R + m_{CM}; m_Y^* = m_Y + m_{CM}; m_B^* = m_B + m_{CM};$$

$$v_{RO(AV)} = \frac{m_R^* V_{dc}}{V_p} \frac{1}{2}; v_{YO(AV)} = \frac{m_Y^* V_{dc}}{V_p} \frac{1}{2}; v_{BO(AV)} = \frac{m_B^* V_{dc}}{V_p} \frac{1}{2}$$

$$v_{RY(AV)} = v_{RO(AV)} - v_{YO(AV)}$$

$$v_{RN(AV)} = (v_{RY(AV)} - v_{BR(AV)}) / 3$$


$$v_{RN(AV)} = \frac{V_m \sin(\omega t) V_{dc}}{V_p} \frac{1}{2} \neq v_{RO(AV)}$$


EE, IISc 25

And as we saw yesterday we can also add common mode signals to m R m, Y m B and get m R star, m Y star m B star which contains sinusoid plus some triplen frequency components. In that case v RO average would be the wave shape would be similar to that of m R star, v Y o average wave shape will be similar to m Y star and so on. So, the common mode existence m R star and v RO average, but in v RY average is the common mode will go away. Because when you are doing v RO average minus v Y o average the common mode content here is same as the common mode content here, and therefore, they get cancelled out, and v RN average will also have no common mode component. So, your v RN average will be v RO average minus the common mode component. So, that is what you will get you will get this is a sinusoidal voltage now.

(Refer Slide Time: 36:07)

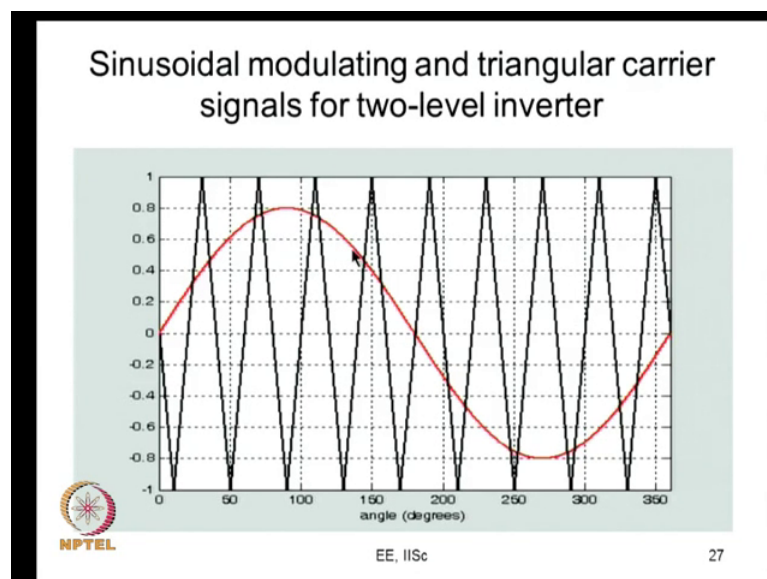
Two-phase average voltages

$$v_{\alpha,AV} = \frac{3}{2}v_{RN,AV}$$
$$v_{\beta,AV} = \frac{\sqrt{3}}{2}(v_{YN,AV} - v_{BN,AV})$$
$$v_{RN,AV} + v_{YN,AV} + v_{BN,AV} = 0$$


EE, IISc 26

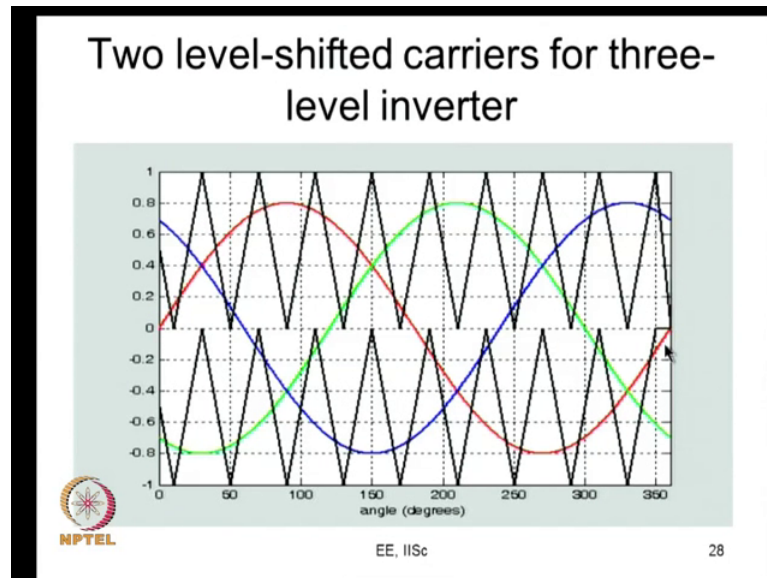
So, your three-phase v RN average, v YN average and v B n average can be transformed into v alpha average and v beta average because when the three sum up to 0 you know you need only two quantities to represent them. So, this is space vector transmission.

(Refer Slide Time: 36:20)



The difference comes in the two-level and three-level cases that you compare it with the single carrier now. I have not shown the Y phase and the B phase sinusoids here, I have shown only the R phase all of them compared with the single carrier now.

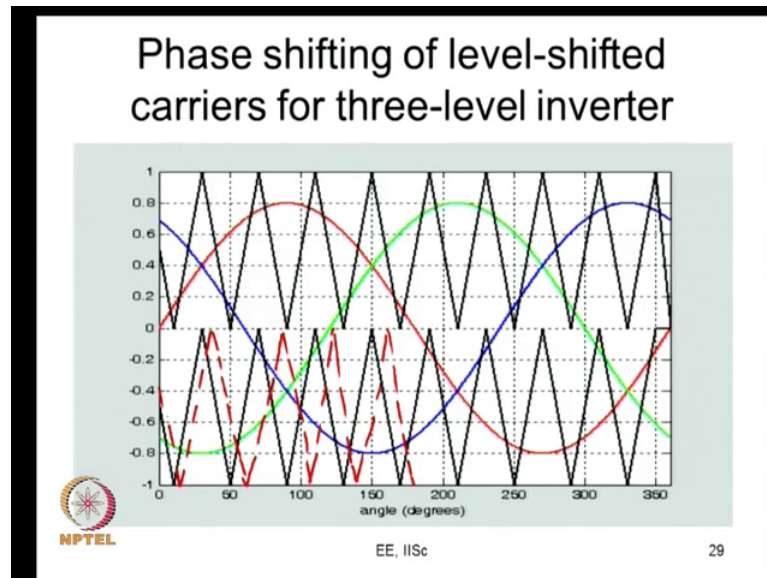
(Refer Slide Time: 36:33)



In the case of a three-level, you need to do it differently you do not have one pair of complementary switches you have two pairs of complementary switches. So, you have two-level-shifted carriers. So, you know there is one top which runs between 0 and 1, there is a bottom one which runs between minus 1 and 0. So, the R, Y, B are all compared here. So, how do you do this what could be the switching logic for example, if considered R phase here, it is greater than both the carriers then v_{RO} is plus 0.5 V dc which means s 1 and s 2 are both high.

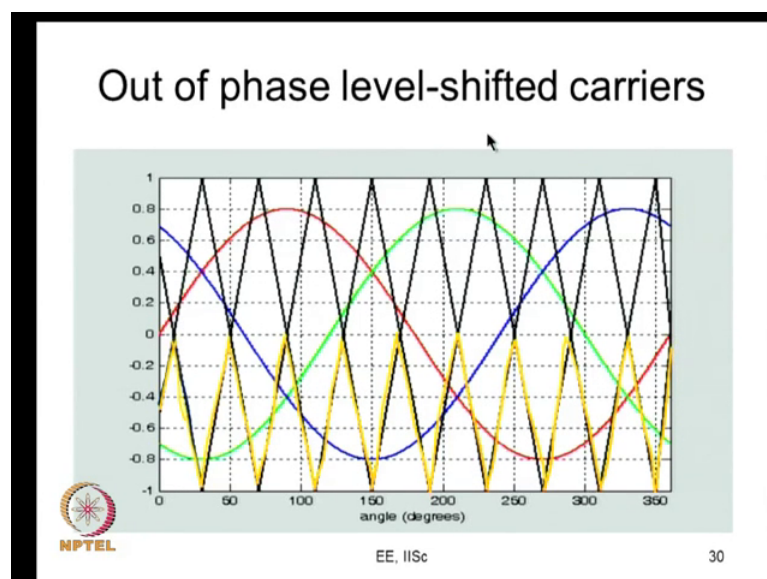
And you take a situation here where m R is lower than both the carriers. So, in that case S 3 and S 4 are high. So, v_{RO} will be minus V dc by 2. And you take anywhere in between where like for example, here, so you know m R is less than one carrier, but greater than the other carrier in that case v_{RO} is equal to 0. So, s 2 and s 3 will be on the middle two switches will be on in the R phase, so that would be your switching logic and you can go about doing this. And this will result in sinusoidal output waveforms as you wanted here like you will get sinusoidal outputs as you want here, and thus will give you sinusoidal line to line voltages average voltages will all be sinusoidal.

(Refer Slide Time: 37:51)



Now, you can also do a phase shifting as I mentioned in the last lecture. So, whether there is any advantage or not is something that you have to see, but it is possible to do that. Now, let me do this phase shifting like this that is what I mean is the top carrier let it be wherever it is, the bottom carrier the same carrier in just shifting it by a certain small angle at this frequency. So, this is the phase shifting. So, what I can do now is I can compare this with two-level-shifted carriers, but they have phase shifted like here. So, generally this will not affect the fundamental voltage provided you have assumed a very high carrier frequency, but this will affect the harmonic voltages now.

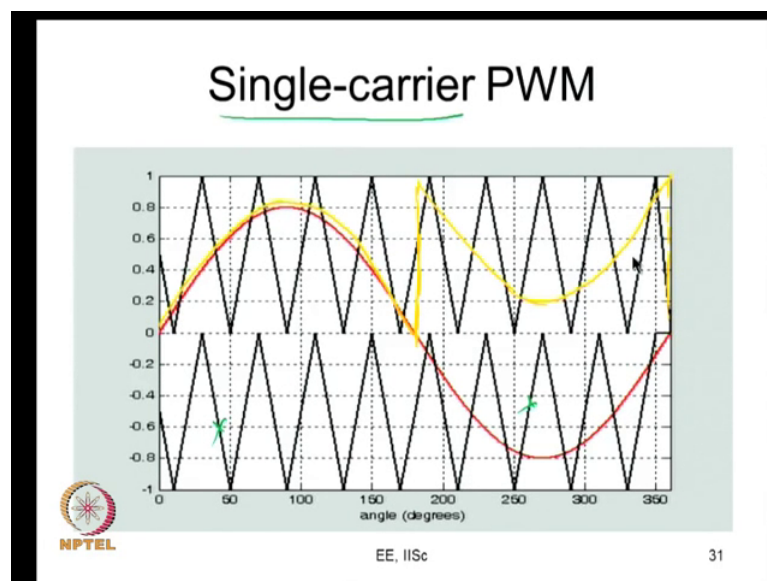
(Refer Slide Time: 38:43)



So, very specific case which is sometimes considered also is the out of phase level-shifted carriers actually what you have here is that let me use a different colour for clarity. So, the top is one carrier, this is another carrier, this colour is also not very clear here. So, should I use orange? So, you can see that this is another carrier, the black is one carrier, this is another carrier. So, because I have used the same colour the carriers may not be very clear to you, therefore, I am changing that.

So, here again you can use the same logic. So, for example, you can say here m_R will be plus V_{dc} by 2, v_{RO} will be plus V_{dc} by 2. And it is between the two carriers then the phase would be 0 the pole voltage; and if it is lower than that then the pole voltage can be minus V_{dc} by 2. So, you will see that you know the harmonic differences are very very pronounced and some studies have also been carried out earlier which shows that the out of phase level-shifted carriers will lead to a much worse harmonic distortion than the single phase carriers now.

(Refer Slide Time: 40:01)



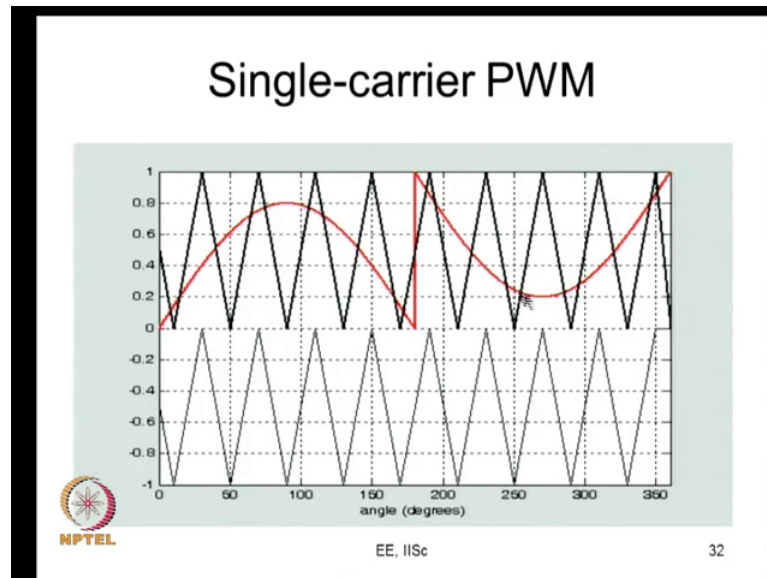
You can actually look at it by looking at the switching sequences which we will do it in some two slides from now so something that I told you at the end of the last lecture. So, before we go into that, let us take the same you know in phase carrier because this is what is preferred from a harmonic performance point of view this is very good. But the trouble here is when you two carriers you know you have to produce two carriers, one is positive, one is negative and you know this signal is bipolar, so normally it is very easy

to handle if the signals are all unipolar in many microcontrollers and microprocessors. So, you can avoid. So, you can see for example, if you look at only the R phase, you see that this part of the carrier they do have no role at all, there is no intersection, again here there is no intersection at all.

So, let me do one very simple thing. What is that let me shift this up, let me shift this up I am showing this in kind of orange colour. So, what I am going to do is I am going to shift this up. So, this orange one is the negative R phase shifted. So, I have the same waveform here from the positive half cycle. And for the negative half cycle let me phase shift like this. So, what do I have here what is the difference between this and that, this is same as I marked; in the negative half cycle this is equal to $1 + m R$ that is what has been done. Now, you compare. So, the comparison between this and the triangle is same as the comparison between this and triangle there is actually no difference really at all you know you should bear in mind that these are very high frequency carriers.

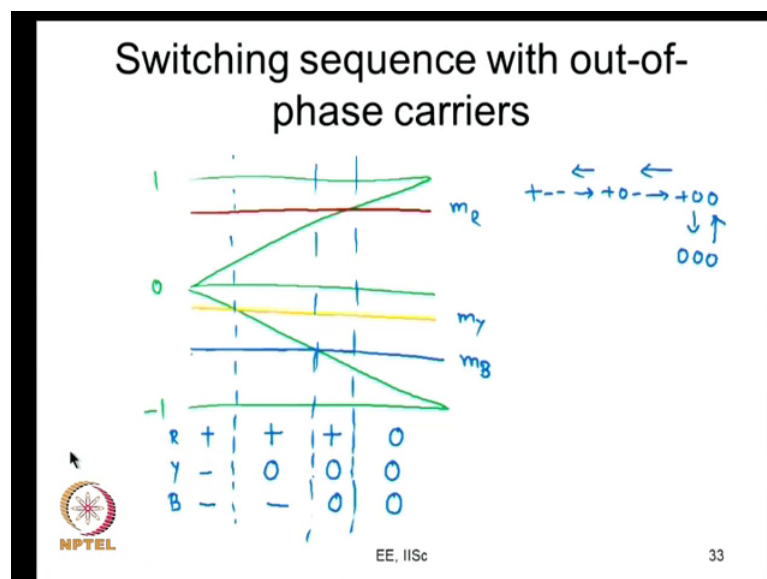
Now, I have shown very few only about nine carrier cycles or so, because it is easy for me to draw that way it is very more difficult for me to draw out of 150 cycles or it may also get very cluttered now. So, we are just shifting this part. So, now, what do you need you may not need the lower one at all you may not need, you may not need the lower carrier at all you will not need the lower carrier at all. So, you do what is case the single carrier PWM like we have one sine wave and two carriers there are also methods where you use two sine waves and one carrier that is also been discussed in the literature. And now this is some modification of your in phase carrier PWM, so that you can use just a single carrier by phase shifting or things all.

(Refer Slide Time: 42:30)



So, this is what I shown plotted here see you this is something you do in your PWM generator, and you do your comparisons based on that so that is easy way of implementing. So, this is only this is very identical to what you do with two-level-shifted carriers which are in phase and that is what we will be considering for the rest of the discussions in today's lecture and the next lecture. So, what we are actually considering is this three phase sine waves compared with two-level-shifted carriers and this is equivalent to that, so that is the PWM waveform you are going to consider.

(Refer Slide Time: 43:03)



So, now let us go and start looking at what we first assumed. You know said that out of phase carrier lead to higher harmonic distortion whatever. So, for that we need to prove, so for that we need to look at the switching sequence. So, how can we possibly do that. Now, let us say we take some levels this is we call this as 1, 0 and minus 1. So, we are going to consider out of phase carriers right. So, let us say this is the top carrier and let us say this is the bottom carrier. So, now, what I am going to look at is I am going to consider three phase signals so R lets say the R phase signal is here. Now, I need to consider Y phase signal. So, let me use orange here for the time being. So, let say the Y phase signal is here. And I need to use B phase, so it is like here. So, the three would actually add up to 0, you can actually call them as m_R , m_Y and m_B , whereas the other two are carrier So, this they should add up to 0 if you are considering is sinusoidal PWM.

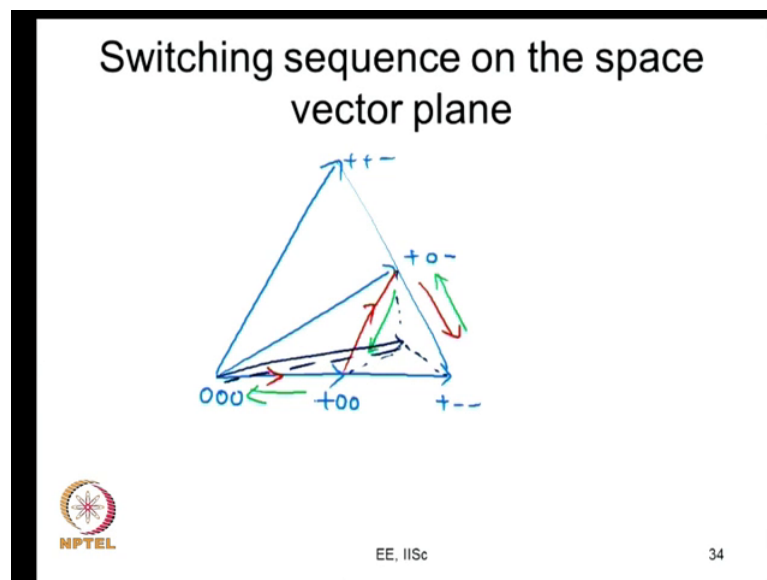
So, now, what happens here you have first certain time interval you have one the happening here. Prior to this interval what happens this is R phase, so you see that the R phase is excuse me R phase modulating signal is greater than both of R phase modulating signal is greater than both the carrier signals, so that is plus it is equal to plus V_{dc} by 2. And that is the case up to this point up to this point R phase pole voltage is plus V_{dc} by 2, beyond this point it is 0. If you take Y phase, Y phase here is minus V_{dc} by 2 and from here onwards Y phase is 0. If you take B phase, it is minus V_{dc} by 2 up to here and from here onwards, it is 0. So, if I write down the sequences this is one switching instant, this is another switching instant, this is yet another switching instant

So, R phase is positive let me write down for the states R, Y, B positive, Y phase is 0 and B phase is also no Y phase is negative, Y phase carrier is lower than both the I mean Y phase is modulating signal is lower than both the carriers and therefore, it is minus. And if you look at the B phase also, it is minus. Then in the next interval R phase is positive because the R phase modulating signal is greater than both of them. Here again the R phase is positive because its modulating signal is greater than both the carriers, here it becomes 0. If I look at Y phase minus at this instant Y phase is switching and then after that it is 0. So, it is the Y phase, v_{YO} is 0, here also v_{YO} is 0, here also it is 0.

And how about B phase initially it is minus. So, in this interval also, it is minus; in this interval it is 0; and in this interval, it is 0 this is what you get. So, your inverter state sequence starts from plus minus minus and next it goes to plus 0 minus and from there it goes to plus 0 0 and there it goes to 0 0 0. And you will see that in the next sub cycle if

you consider the next half carrier cycle the same thing will happen in the opposite direction from 0 0 0, it will go to plus 0 0. From there it will go to plus 0 minus and from there it will go to plus minus minus, this will keep happening then for half a sector or so on. So, this is the nature of variation in the inverter states.

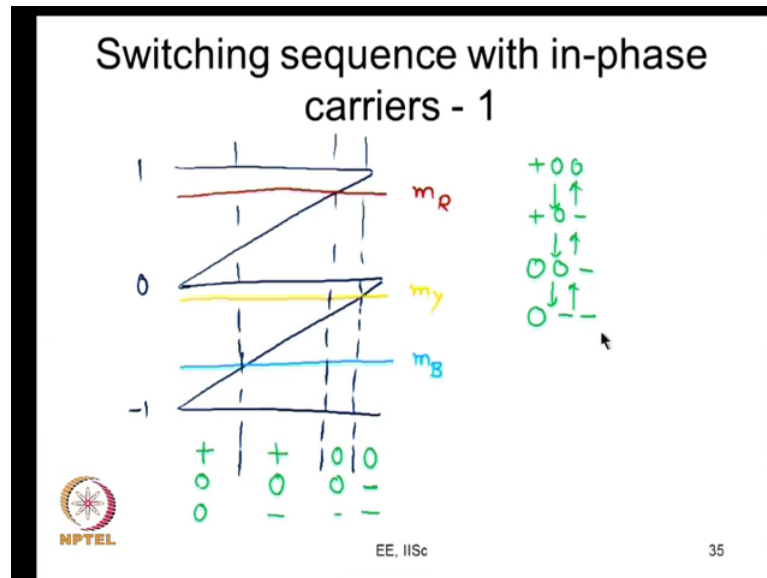
(Refer Slide Time: 47:07)



Now, let us look at how it varies for the other one that is let us look at this in this space vector plane. So, we have 0 0 0 is here we have then plus 0 0, which is here and we have plus 0 minus and plus minus minus plus minus minus is here and plus 0 minus is here this is plus plus minus, plus 0 minus. So, the nature of state transition here is you start from here then here then you go here, this is one. And in the next sub cycle also you will come back in the opposite direction. So, this would be a your sequence this how you are going to change now.

So, let us say where will the average vector be the average vector can be anywhere here the average vector can be anywhere within this, so that will be bound by these steps. So, the average vector can fall anywhere within this one. Now, let me say the voltages are such that the average vector is here, let me choose some other colour. So, the average vector is here. So, now, what happens you look at the error this error is small this error is small this error is small; however, this error is quite large. So, you have a large error coming up here, so that is one reason why the harmonic distortion is quite high.

(Refer Slide Time: 48:52)

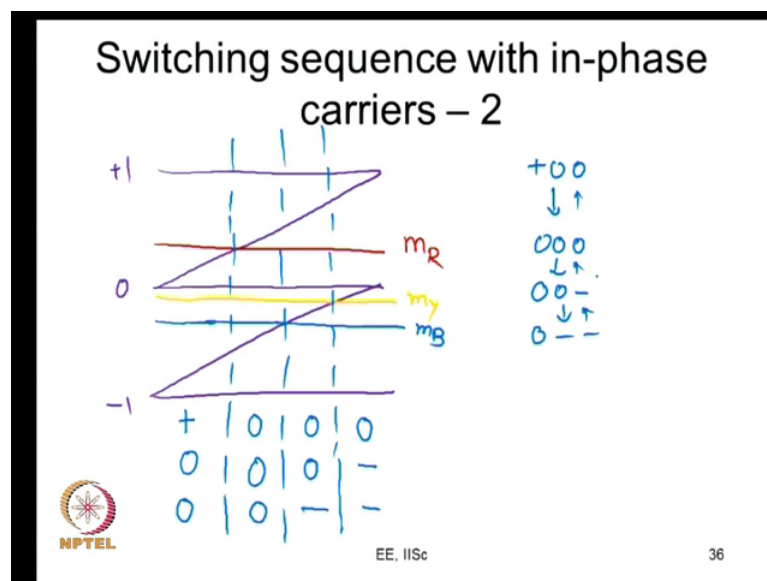


The same way if you will try to do it for this switching sequences for in phase carriers you have 1 0 and minus 1. So, let us say the carriers are in phase. So, the top carrier is rising. So, let us say the bottom carrier is also rising then let us say we go in for red colour. And let us say this is m_R , the R phase modulating signal in this half carrier cycle then let me say I will go to Y phase this is the Y phase modulating signal in this carrier half carrier rather. Then this B phase let me say this is the B phase modulating carrier here. So, now, you have like this what are you going to do from here we are going to look at the various switching transitions when are the switching transitions going to occur. So, you have one switching instant here then you may have another switching instant occurring here and you have third switching instant occurring here.

So, what are the various in this interval if first interval I considered R phase is modulating signal is greater than both the carrier, and therefore, this will be positive. And here also the R phase would be positive, and here it is 0, and this is again would be 0. And then if you look at Y phase in this case Y phase is being compared with the bottom carrier it can actually be 0 or 1, initially Y phase is 0, here also it is 0, here also it is 0, and here it becomes minus. Then if you look at B phase initially it is 0 then here it switches and it goes to minus and it is minus and it is minus. So, how does the inverter state change from plus 0 0, it goes to plus 0 minus and it goes to 0 0 minus, it is 0 minus minus. So, this is how it goes from here in one direction and if you look at the next sub cycle it will probably go in the opposite direction.

So, you can see that all these are neighbouring vectors, you can see everything is away only by one switching here only B phase is switched here only R and then. So, there is one switching for state transition something automatically ensured by most of these methods. Any well-designed method will actually ensure that. If you are doing it in that space vector method and you will construct your sequence assuming you know enforcing this particular condition you will not unnecessarily switch let us say two phases or three phases together for a particular state transition. So, now, this is plus 0 0, plus 0 minus, 0 0 minus and 0 minus minus.

(Refer Slide Time: 51:56)

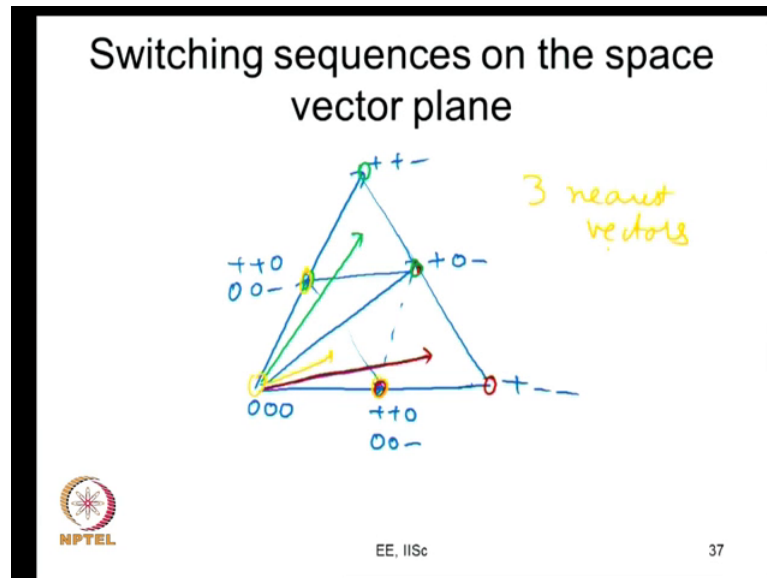


Now, let us say I look at a similar one. Now, this is plus 1 0 minus 1 these are the two carriers. And let me look at the low modulation index. So, low modulation index meaning I may have my m_R like this; this is my m_R . Let say I am having my m_Y , m_Y is like here; and let me have my m_B m_B is like here. So, there are number of switching transitions where are the switching transitions this is one and this is another switching transition and this is yet another switching transition.

So, if you look at the R phase, the R phase is initially positive and then its switches to 0, here it is all 0 0 0. Then if you look at Y phase it is initially 0 continues to be 0 0 and becomes minus. If you look at B phase, it is 0 0 and it is minus and minus here. So, this is how they are transitioning, so that is it starts from plus 0 0 and goes to 0 0 0 and goes to 0 0 minus and then 0 minus minus. The same thing will happen in the opposite

direction in the other side. So, it starts with plus 0 0 goes to 0 0 0, you look at what happens usually plus 0 0, it went to plus 0 minus, 0 0 minus and 0 0 thing. So, you see that it is different. Why is it different, because the modulation indices are different so, but in both the cases there is one similarity, these vectors as also these vectors they are all neighbouring vectors.

(Refer Slide Time: 54:09)



Let us go on the space vector plane. Let me draw that here what happens in, so if I say plus 0 0, 0 0 0, 0 0 minus and 0 minus minus. Every time whatever I may do what you will find is you will find depending on you know case by case for many cases that you may consider this would be the three vectors applied or these would be the three vectors applied or these would be the three vectors applied and these would be the three vectors applied that will depend upon the average voltage vector. You have the three phase modulating signals you can transform it into the space vector domain. And in this space vector domain, if you see that your reference vector is here sorry if you see that your reference vector is here, you will see that these vector should have been used. On the other hand, if your reference vector is here, you will see that these three vectors get applied.


The same way if you let us say your reference vector is here you will see that these vectors get applied and they go around this. So, these are what you would call as the three nearest vectors. And in phase sine triangle PWM make sure that the three nearest

vectors get applied and therefore you have a very good this thing I mean harmonic distortion.

(Refer Slide Time: 56:10)

References – analysis of sinusoidal PWM techniques for three-level inverter

- D. Banerjee, Rajesh Ghosh, V.T. Ranganathan and G. Narayanan, "Comparison of various sine-triangle PWM techniques for three level voltage source inverters in space vector domain," National Power Electronics Conference, NPEC 2005, Kharagpur, India, Dec 2005.
- Soumitra Das and G. Narayanan, "Space vector based analysis and comparison of sinusoidal pulsewidth modulation schemes for a three-level inverter," National Power Electronics Conference, NPEC-2011, Bengal Engg Science Univ, Dec 2011.
- Soumitra Das, "Study on pulsewidth modulation techniques for a neutral-point-clamped voltage source inverter," PhD Thesis, Dept. of Electrical Engg, Indian Institute of Science, Bangalore, July 2012.




EE, IISc 38

You can find something work in this particularly comparison of in phase and the out of phase carrier in the first paper which has published presented in the National Power Electronic Conference. And this is the I mean a later a study it is a follow up on the previous work is the other one which us presented in again the National Power Electronics Conference in 2011. And this PhD thesis by Soumitra Das contains a chapter which is really this comparison of this various methods now.

(Refer Slide Time: 56:40)

Addition of common-mode to three-phase sinusoidal signals

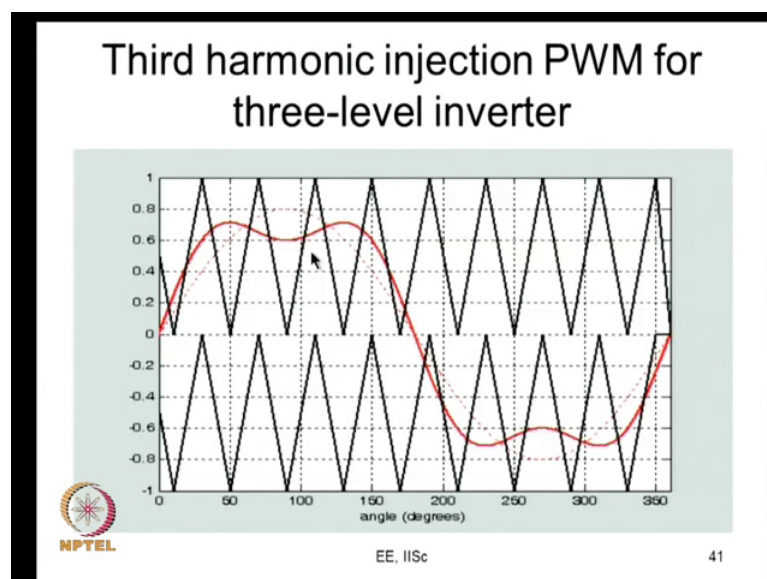
- Third harmonic component
- Bus-clamping PWM or discontinuous PWM
- Different continuous and discontinuous modulating signals are possible
- “Zero clamping” is also possible
- Comparison of three-phase modulating signals with in-phase triangular carriers



EE, IISc 39

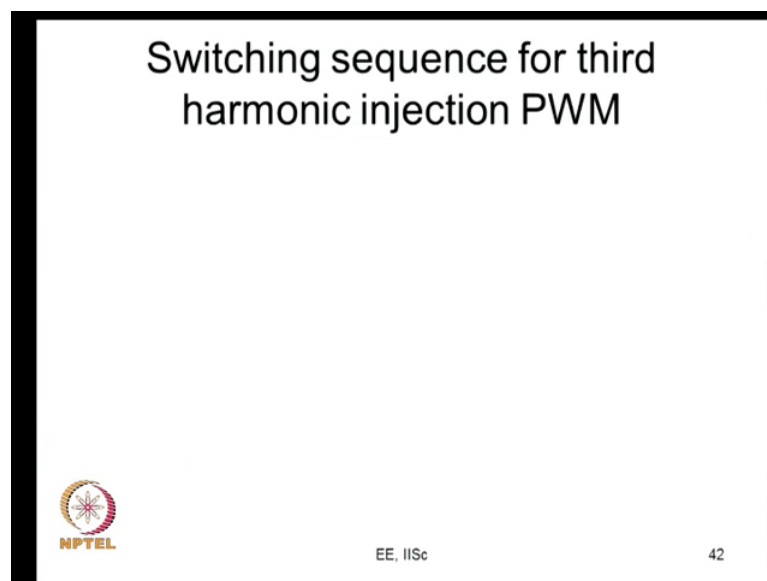
So, what we can actually see is you can also add common mode components to that for example, you can add third harmonic component, you can add certain common mode components which result in bus-clamping so called discontinuous PWM. And different continuous and discontinuous modulating signals are possible with three-level inverter; in two-level inverter, you can clamp a phase only to the positive bus and the 0 bus negative bus, here you can also clamp to the 0 bus that is some interesting possibility you have. And you can compare this three phase modulating signals with in phase triangular carriers.

(Refer Slide Time: 57:09)



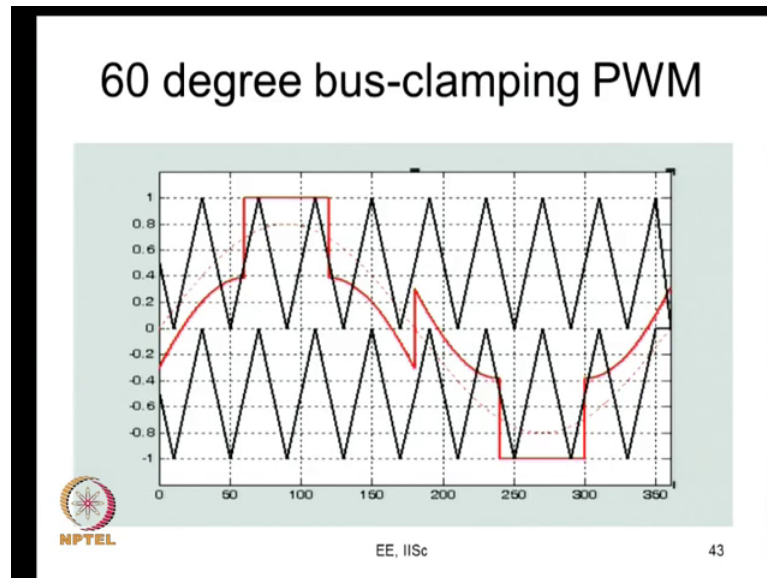
So, this is what we would look at now. For example, if you see this there is a third harmonic injection compare them with two-level-shifted carriers as before you get your PWM. So, what will happen is you know the pivot states the so called pivot state there the time for which they are applied will be the same three nearest vectors will be applied. You will see that one of the vectors get applied twice you may see it to it is always starting from here and ending back here that vector is you know both the 0 states are used that time division will change that is what you will observe now. It is actually interesting to do these studies also.

(Refer Slide Time: 57:41)



And this switching sequence what happens is this is pretty similar if I want to analyse that I is a similar to sine triangle PWM. What we did here in sine triangle PWM you can consider the same way let say like this. You add a small common mode maybe positive common mode or negative common mode and do the comparison. What you will get this plus 0 0, you know this instant may all the three instant may shift to the left or shift to the right. So, the time for which plus 0 0 is applied and 0 minus minus applied they will change, but their sum will remain the same. So, we call this pivot vector this is 0.5 V dc, this is same 0.5 V dc length vector, this is we call pivot vector and these two states are called pivot states like the division of 0 states changing here the division of pivot states will change.

(Refer Slide Time: 58:24)



The same thing you can also do with the you know may 60 degree bus-clamping method you can do an analysis. So, this R phase will be here and the Y phase and the B phase signals will be lower than that you can look at the switching sequence for bus-clamping PWM like we did for sine triangle PWM. You can consider this as an exercise for yourself.

(Refer Slide Time: 58:39)

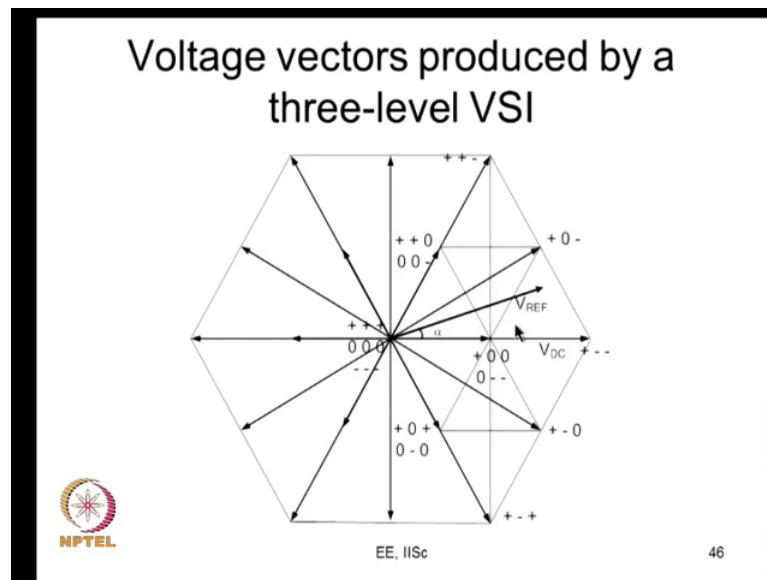
Reference – switching sequences in carrier-based PWM techniques for three-level inverter

- Soumitra Das, “Study on pulsewidth modulation techniques for a neutral-point-clamped voltage source inverter,” PhD Thesis, Dept. of Electrical Engg, Indian Institute of Science, Bangalore, July 2012.

EE, IISc 45

And. So, you can see this various switching sequences for carrier based PWM method they have been analysed in this thesis. So, this is a useful reference for you.

(Refer Slide Time: 58:47)



So, we would actually see this is the complete set of voltage vectors which we discussed before they look like this.

(Refer Slide Time: 58:55)

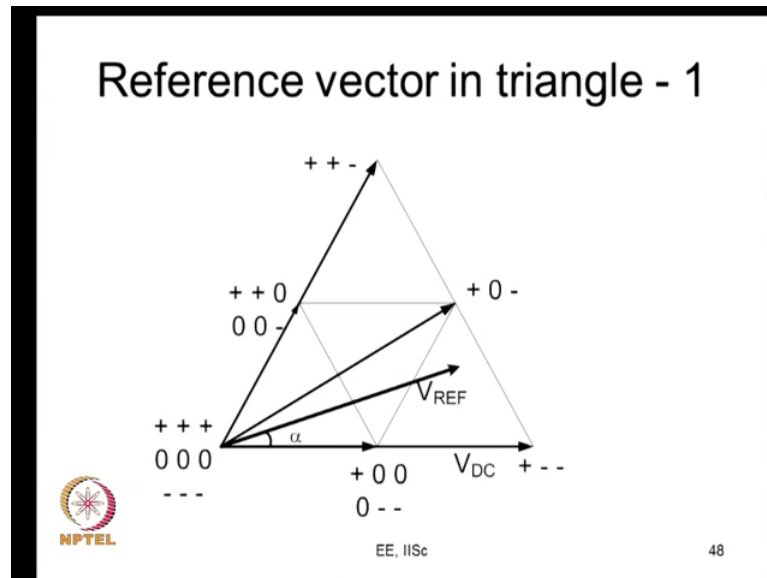
Space vector based PWM for three-level inverter

- Voltage reference provided as a revolving voltage vector, which is sampled once in every subcycle T_s
- Sector within which the sample falls is identified
- Set of voltage vectors (normally the three nearest vector) to be applied is identified
- Dwell times calculated for each vector
- Voltage vectors (inverter states) outputted in the desired sequence

EE, IISc 47

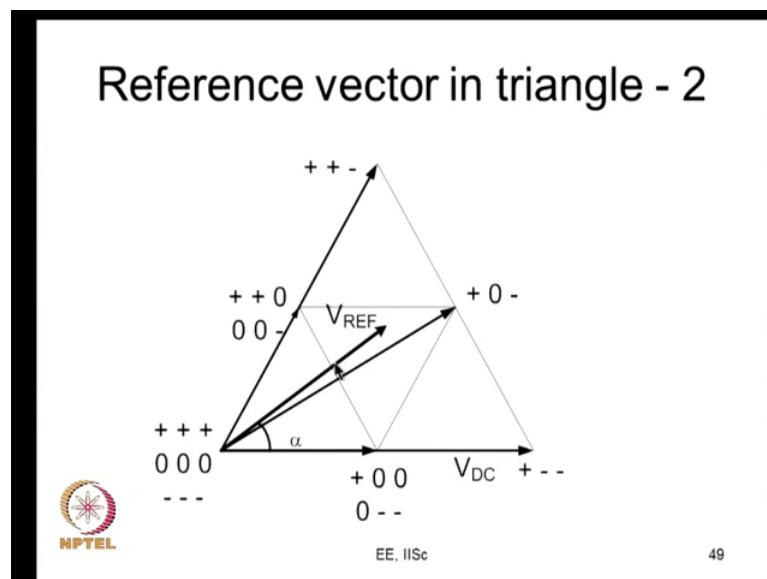
And when you go in for space vector based PWM which is an extension of the space vector based PWM for three-level inverters.

(Refer Slide Time: 59:01)



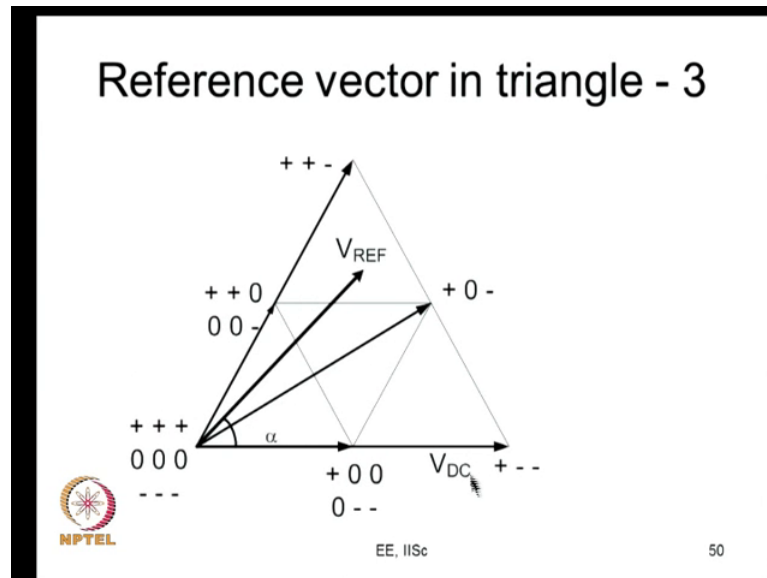
But you have a few issues because in every sector we have multiple triangles.

(Refer Slide Time: 59:05)



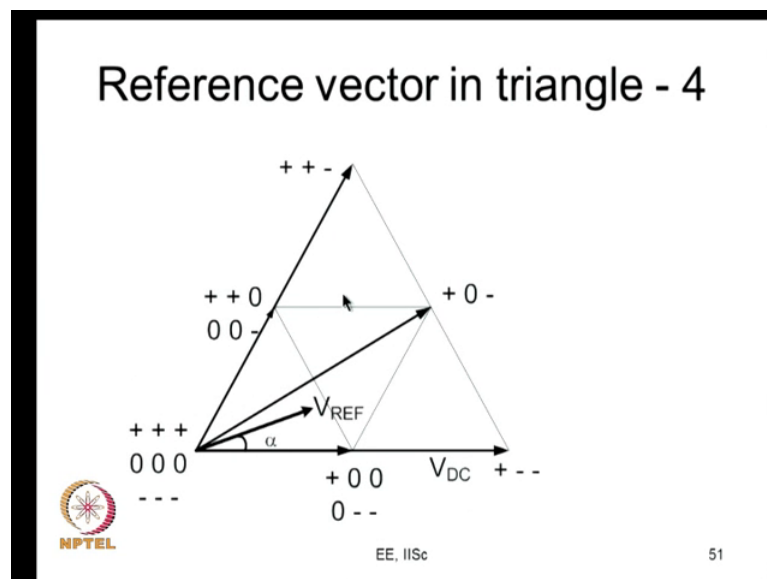
And in each triangle, you will use this one.

(Refer Slide Time: 59:08)



In another triangle, you will use this vector and so on.


(Refer Slide Time: 59:10)



(Refer Slide Time: 59:11)

Steps in PWM calculation for space vector modulation of three-level inverter

- Each sector is divided into four triangles
- Each triangle is formed by tips on three voltage vectors of the inverter
- Tip of reference vector falls inside a triangle
- Vectors whose tips form the given triangle are the three nearest vectors
- Dwell times to be calculated for the three vectors
- Dwell time calculation formulae different for different triangles

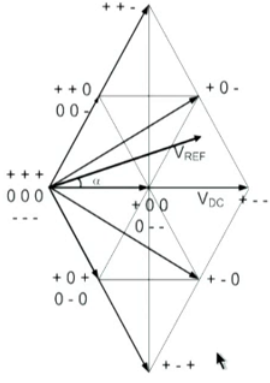


EE, IISc 52

The calculations are all different in different triangle that leads to some difficulties.

(Refer Slide Time: 59:14)

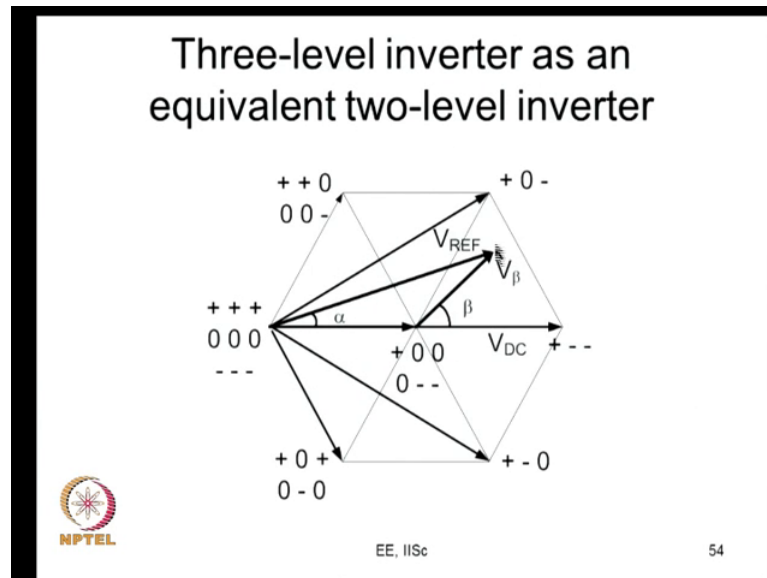
Three-level inverter as an equivalent two-level inverter



EE, IISc 53

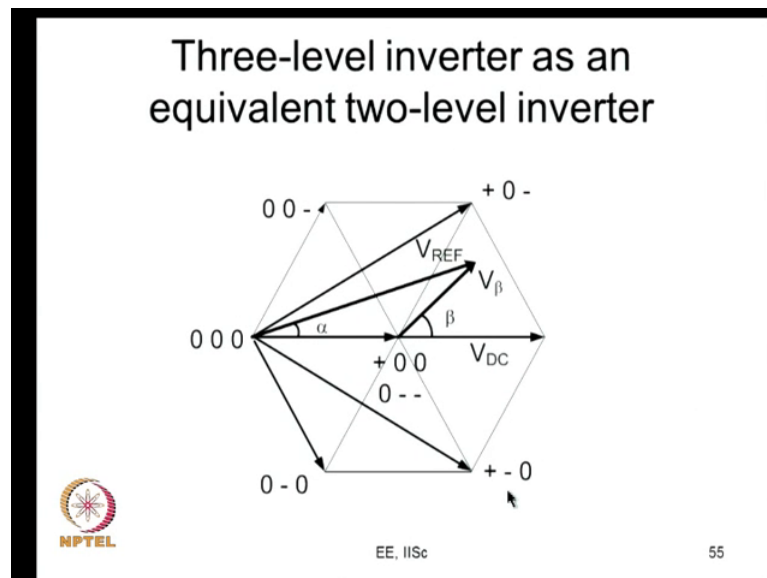
And therefore, you start viewing a three-level inverter as an equivalent two-level inverter.

(Refer Slide Time: 59:20)



So, like only this hexagon and this is something which you would look at in the next class.

(Refer Slide Time: 59:24)




Once you considered it as a two-level inverter.

(Refer Slide Time: 59:28)

PWM calculation for three-level inverter controlled as equivalent two-level inverter

- Identify nearest pivot vector to the reference vector
- Subtract the nearest pivot vector from the reference vector to obtain the equivalent reference vector for the conceptual two-level inverter
- Calculate dwell times as in two-level inverter
- Output voltage vector (inverter state) in the desired sequence




EE, IISc 56

The PWM implementation becomes fairly simple as delineated here; I will discuss this in more detail in the next lecture.

(Refer Slide Time: 59:33)

Reference – Three-level inverter controlled as an equivalent two-level inverter

- Soumitra Das, "Study on pulsewidth modulation techniques for a neutral-point-clamped voltage source inverter," PhD Thesis, Dept. of Electrical Engg, Indian Institute of Science, Bangalore, July 2012.
- T.G. Subhash Joshi, A.S. Haneesh, G. Narayanan and V.T. Ranganathan, "A computationally efficient PWM algorithm for multilevel converters," Proc 1st National Power Electronics Conference (NPEC), pp. 106-111, Mumbai, India, October 2003.



EE, IISc 57

So, these are some useful references in that regard there are couple of references that I have indicated here. So, you could look at those references for this thing, and I will continue this in the next lecture.

Thank you very much.