Pulsewidth Modulation for Power Electronic Converters
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Lecture - 35
Effect of dead -time on inverter output voltage for bus clamping PWM schemes

Welcome to this lecture series on Pulsewidth Modulation for Power Electronic Converters. So, this is actually you know for some of you who may know or might not know like this is very close to particular course called PWM converters and applications, which is start here at the Indian Institute of Science for the Masters and PhD students. So, the students who are specialising in power electronics; you do this as an elective course. So, this lecture series is very closely related to this particular course.

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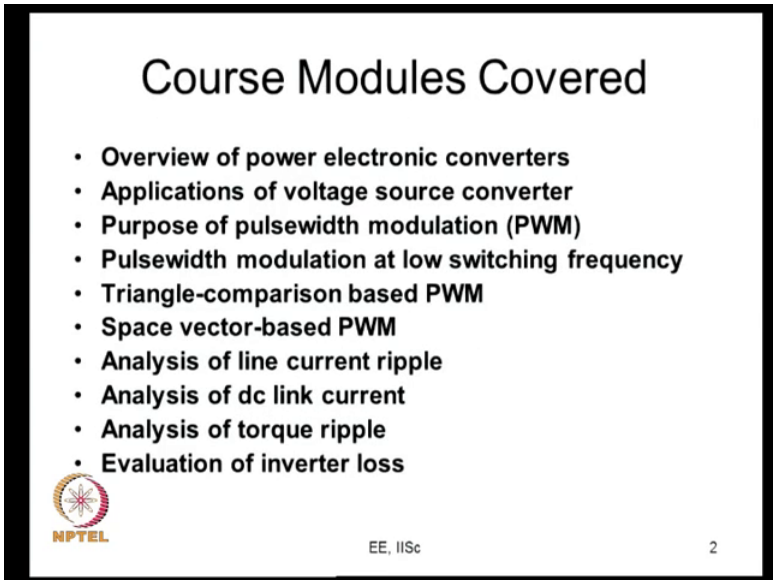

So, what we have is; you want to modulate power converters, you should get a good feel for the power converters. And therefore, as I have done this many times so, we do this kind of; if there is a, we first look at the basics of power converters. That is there are highest power electronic converters are essentially only switches. So, we look at how switches are connected for; let us say DC-DC conversion and DC-AC conversion. So, we looked at it in one of the modules before.

And these power converters what are the primary purposes? Sometimes there is DC available, you want AC; you have an induction mode drive, it needs variable frequency

variable amplitude AC, so that is one application how voltage source inverter. Another application is you can use a voltage source converter for active rectification, which is also another application that you can think of. And you can sometimes use a voltage source converter to supply reactive power to the grid.

So, that is static compensator and you can use these voltage source converters to pump power from renewable energy sources into the grid. Let us say you have some photovoltaic cells and you can use a voltage source converter to power into it. So, they are useful in a variety of applications now and what happens is in all these applications. So, voltage source converter it has three things like one is the DC voltage other one is the modulation and then the AC voltage, so these three are mutually related.

So, the modulation determines the efficiency particularly you are worried about efficiency. So, and the modulation also determines let us say things like waveform quality. When you do a DC-AC conversion, you are not producing sinusoid; you are producing with lot of harmonics, so we are trying to do this. So, this course on modulation what exactly tries to do is; it tries to give a background on generally on power electronic converters for DC-AC conversion and various applications of these. And tries to give certain fundamentals, which will help you understand the PWM methods for motor drive applications and probably and do certain analysis on what you want to do.

For example how much harmonic distortion would be there? Or how much pulse rating torque could be expected? And such things like that. So, certain amount of analysis and also amount of efficiency, so these are the various things what we have really been doing now. So to get some background on that, we had a short module on pulsewidth modulation. So, where we looked at Fourier series, how do you control? And how do you control the fundamental voltage and how one can possibly try to reduce the harmonics and so on.

So, we looked at certain things like that and we looked at things like selective harmonic elimination and optimal offline optimal PWM etcetera in this other module on low switching frequency methods. So, then we started looking at this PWM generation which is more commonly used; like this triangle comparison based PWM and space vector

based PWM where these switching frequencies are typically much higher than the modulation frequencies.

Then we looked at the analysis of the waveform quality. So, particularly of line current ripple; how much current can be expected and things like this now. So, and we also did an analysis of the DC link current and then torque ripple and up to this part, we have ignored all the losses and all that. Though from the line current ripple, you can get the additional copper loss that will be there in this series elements and from the DC link current, it is possible for you to calculate the capacitor RMS current and using the capacitor RMS current and the ESR, it is possible for you to calculate the capacitor loss.

Now, here we are focuses on the switching losses and the conduction losses; the losses in the power semi conductor device. So, these are the various things which we did till now; there are certain other operational issues; that is one is inverter dead time. So, though for largely we have assumed the inverter to be ideal, I mean the devices all to be ideal; the devices are not exactly ideal. Many times you can ignore the non idealities, but sometimes we cannot ignore the non ideality.

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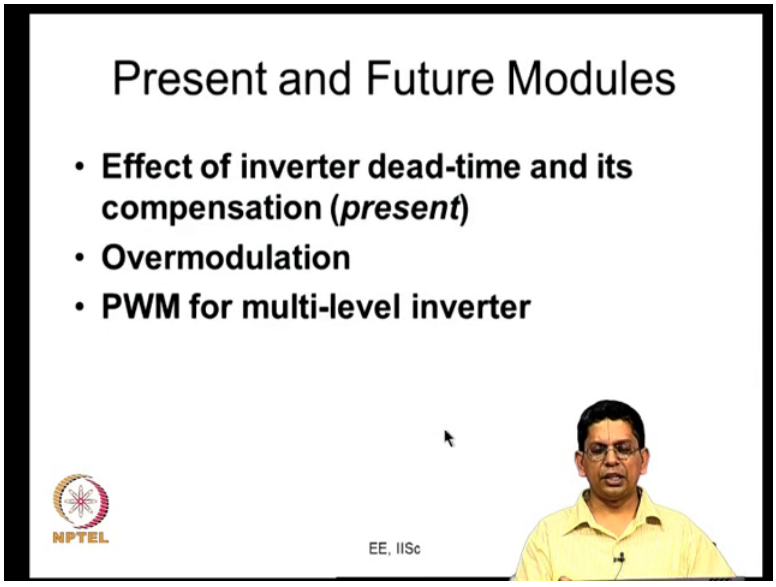

So, for example, the devices are switching in a complementary fashion; there is a finite amount of time it takes to turn on turn off. For many analyses, you can say I am going to say that it is instantaneous turn on or instantaneous turn off, but when you practically

switch an inverter you cannot ignore that. So, one of the things that you really do is introduce this so called dead time, which we just saw in the previous lecture.

So, the dead time what do you do? You are introducing some intentional delay between the switching on, of the complementary devices, they are complementary devices one is turning off, other one is turning on; do not do that to concurrently; first you turn off and then you turn on the incoming device. So, that is the idea and that is what is called as dead time.

And now we have what we have been trying to see in this module, the last lecture on this lecture is to understand the effect this inverter dead time will have on the inverter output. We considered sine triangle PWM primarily in the last lecture or continuous PWM schemes in general. And we tried to see how this little dead time, the short delay between the switching off of one device and switching on of the other device; how does it affect the inverter output voltage? So, that was our burden of argument. So, now we will look at it a little more, so we will take a quick recap of certain things and we do some things in a little more detail.

And we would also try to see instead of continuous PWM methods, if you use discontinuous PWM methods or bus clamping PWM methods; how this same dead time will affect the inverter? And we will also see how exactly you can actually compensate. So, you will get some idea how compensation can really be done now. Then we will look at in subsequent modules, we will look at over modulation and we will look at this thing.

So, over modulation is a non-linear region of modulation. So, you have a DC bus voltage and with sine triangle PWM, you are able to produce some AC waveforms. So, if you talk in terms of the peak phase voltage; so, sine triangle PWM can give you a peak phase fundamental voltage of V dc by 2 or 0.5 V dc. Then with all the common mode injection etcetera are space vector based PWM, you are able to move this all the way up to let us say 0.577 V dc or V dc by root 3; 1 upon root three times V d c.

Now, if you go to six step operation; you can go to 2 by pi times V dc; something like 0.64 V dc, but between 0.577 V dc and 0.64 V dc, you need to operate in the non-linear range; that is the reference voltage and the actual fundamental voltage will not be linearly related. So, these are certain challenges; so, how do you do that etcetera would be the burden of our discussion, would be subject of our discussion in the next module.

So, we will finally be looking at some pulsewidth modulation for multi level inverter. One reason is multi level inverters are important, they have been around for three decades and, but they have been; there is been lot of active research in the last decade and so, on. And more important than that is one reason, if we have understood the PWM for two level inverters properly, which we have been discussing all these days.

And if we have understood a multi level inverter properly, which we discussed in the very first module; then we should be able to do this PWM for multi level inverter. Rather doing this PWM for multi level inverter would be a test whether we have understood the previous issues clearly or not. So, all that we have been doing with two level inverters are actually extendable to multi level three level inverter. We just need to know how exactly to do that; including today's discussion which is really a dead time.

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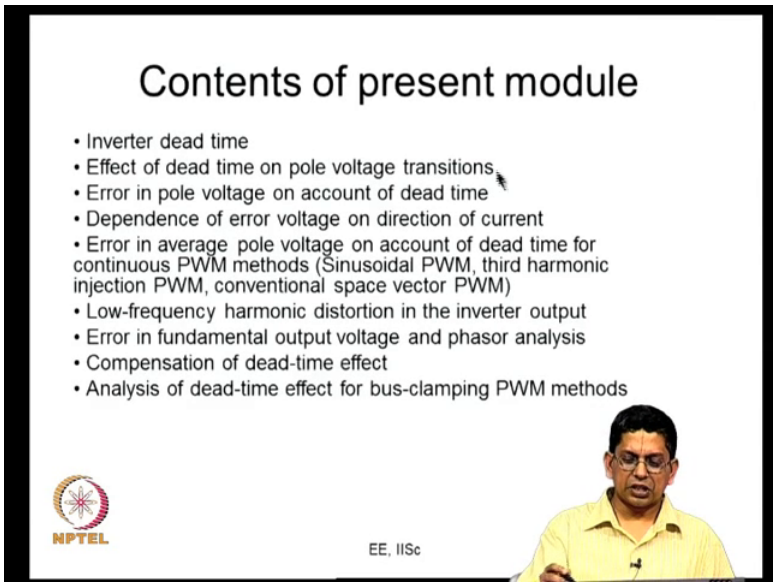

So, let us today once again come back and focus on the dead time effect for two level inverters. So, the various things that which we have been discussing in this module are what is inverter dead time? We have seen this, what is that? There are complementary devices, there are gating signals, the outgoing device is turned off first and the incoming device is turned on later.

There is a small amount of time t d is introduced between the two and that is called the inverter dead time. And what happens because of the inverter dead time? The pole voltage transitions, the instance at which the pole voltage switches from high to low or

low to high some of them change; interestingly it is not all of them changing. So, certain things change and it changes in one direction, that is sometimes all the transitions from low to high transitions their change, there is a delay.

That is if is got to change now ideally; it changes some t d later, there is a delay and, but the high to low does not change. So, and this is seem to be related to the direction of current.

So, we actually we saw in the previous lecture how exactly this pole voltage transitions are affected, it is delayed sometimes by this dead time t d. And we looked at what would be the kind of error voltage, we looked at the dependence of error voltage on the direction of current for positive current or what we call as positive current, the error is negative and vice versa.

And we looked at many continuous PWM or particular focus was on sinusoidal PWM methods and we did this now. Towards the end of the last lecture, we quickly looked at what kind of low frequency harmonic distortion you will have and what kind of error it will have and phasor analysis and so on. So, we will do recap on that and then we will see how exactly, possibly you can compensate the effect of dead time.

And more importantly in this lecture, we will look at the effect of dead time. We will analyse the effect of dead time for bus clamping PWM methods, which would be the most important topic in this lecture which we have not covered before alright. So, here we are talking of effect of dead time on inverter outpour voltage. The last lecture was primarily on continual PWM schemes which we will review now, here it is on bus clamping PWM schemes.

Remember bus clamping PWM is also called discontinuous PWM; so, what happens here? One of the phases clamped to the positive bus or negative bus at any point and other two phases are switching. Therefore, it is called bus clamping; since only two phases are switching in a given carrier cycle, so which two may change? It may be R and Y or it may be Y and B.

So, only two phases are switching in a given carrier cycle; sometimes it is also called two phase modulation, but the most common name is discontinuous PWM because the modulating signals used for this are discontinuous functions of time. So, discontinuous

bus clamping PWM is probably the most widely known name for these PWM schemes and bus clamping PWM is also used and then occasionally that name two phase modulation is also used for this.

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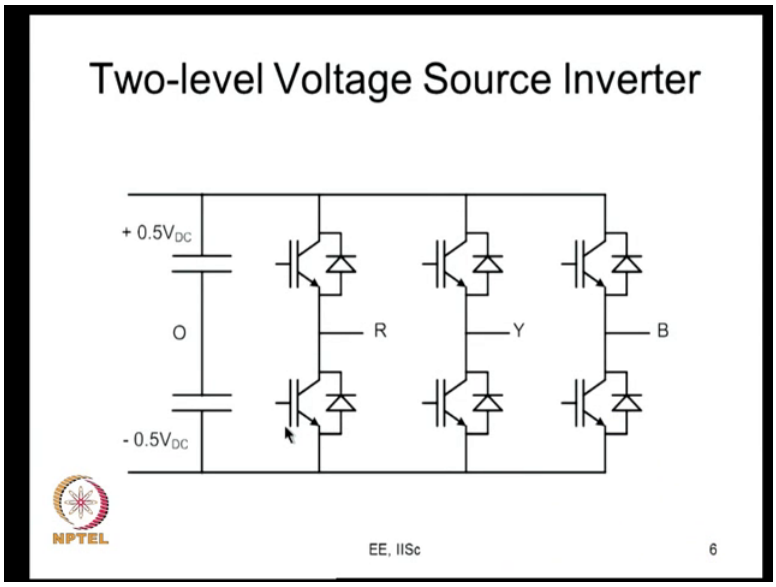

So, now we are talking of the dead time effect in a voltage source inverter. So, first quick look at the voltage source inverter; three different legs single pole double throw switch. The switches are supposed to be switching in a complementary fashion and that is where we have a difficulty now. The gating signal for the top and the bottom cannot exactly be complementary, the rising edges of both of them have to be delayed.

The outgoing device has to be switched off first and the incoming device has to be switched on next, this actually means the rising edges of the gating signals have all got to be delayed by time t d. This is where there is a very significant difference between the previous modules and now. So, they are not exactly complementary; the complementary switches their signals are not exactly complementary now, but it continuous to conduct.

So, there is some small difference; you normally you will expect this, there is a transition from this transistor to this diode and back from here and etcetera. The instance that at which you would expect this transition will now slightly change, as we have seen in the previous lecture. So, if the transition is from transistor to diode; there is no delay, the switching is as per schedule on time, but if the transition is from the diode to the transistor; then there is a delay in the voltage level changing.

So, anyway we will look at it shortly for a while now. So, we are going to look at this is a voltage source inverter, these are complementary devices, but their actual signals are not really complementary, their rising against are all delayed by dead time t d. After your PWM produces these signals for top and bottom devices, there is a dead time circuit which introduces this delay so you have these fed here now.

So, what we are going to look at is the pole voltage that is R; voltage at this midpoint R measured with respect to O. So, we have already seen that the differences; between the ideal V R O and the actual V R O; when you are looking at continuous PWM.

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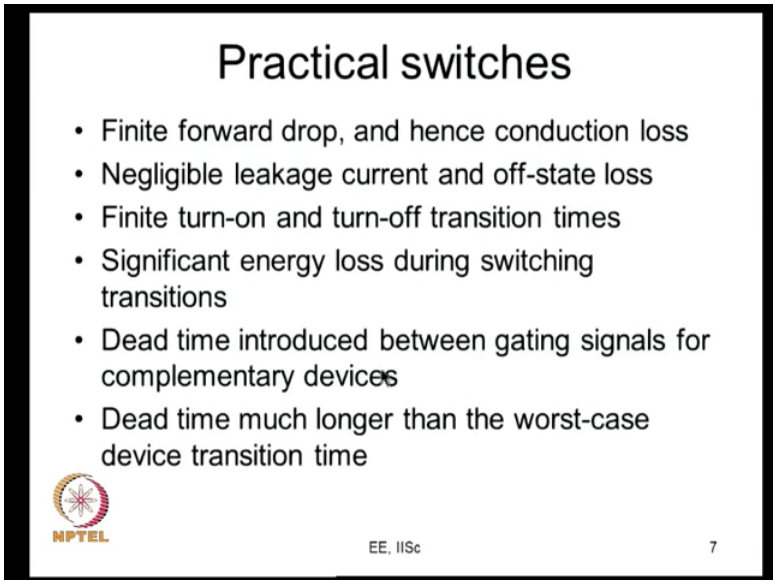

So, we will take a quick look at that once again now. So, once again the practical switches there are problems because of you know forward drop conduction loss and you may have finite turn on and turn off transition. This finite turn on and turn off transition leads to switching energy loss, this was our subject in the last module. But this module what we are doing is because there is finite amount of turn on and turn off transition, we are introducing dead time. So, we are turning off the outgoing device first and then turning on the incoming device next. And there is at this certain amount of time introduced between the intervals, I mean time is delay is introduced between the two and that is what you call as dead time.

And this dead time has got to be much longer than the worst case device transition time; this is what we saw previously.

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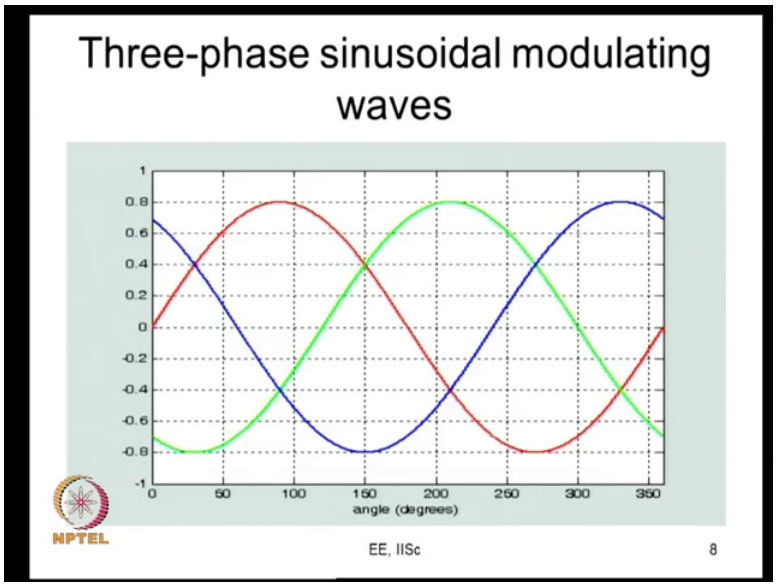

So, once again looking at the best known example of modulation methods like sine triangle PWM; three-phase sinusoidal signals, which correspond to R phase, Y phase and B phase compared against high frequency triangular carrier and you produce the PWM signals. So, the output of this gives the top device and the complementary of that would normally give the bottom device now, there is a small difference; after that there is introduction of dead time as we discussed before.

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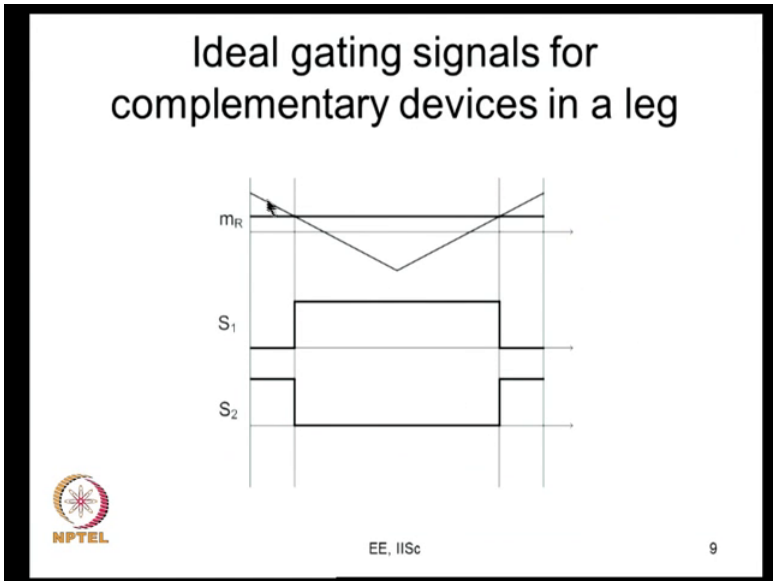

So, normally what you do? You do a comparison; we are now looking at just one carrier cycle. If this is your modulation signal for R phase you compare the output is here; the inverted output or the complementary of that is here. So, this is fed to the top device, this is fed to the bottom device; are supposed to be fed to the top device and supposed to be fed to the bottom device in the R phase like ideally, but the situation is not ideal.

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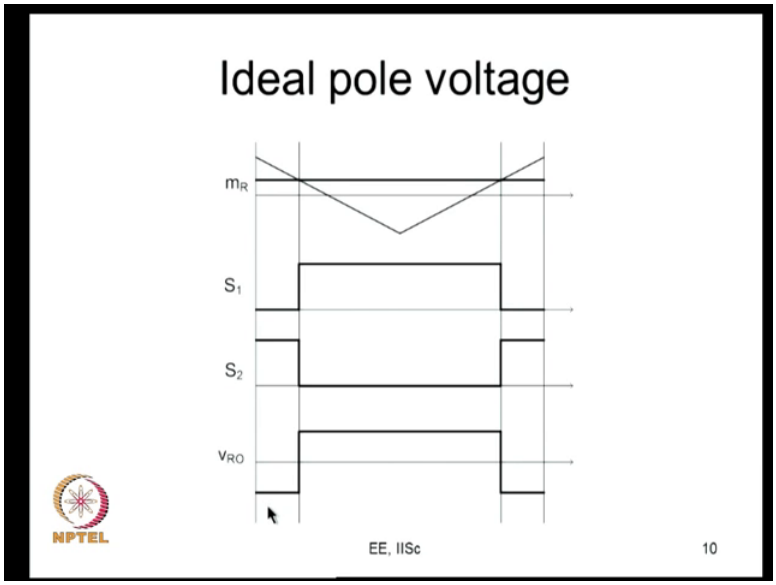

Because the devices are not ideal, the devices are practical; if it were an ideal device you would have fed like this and your pole voltage would have been like this.

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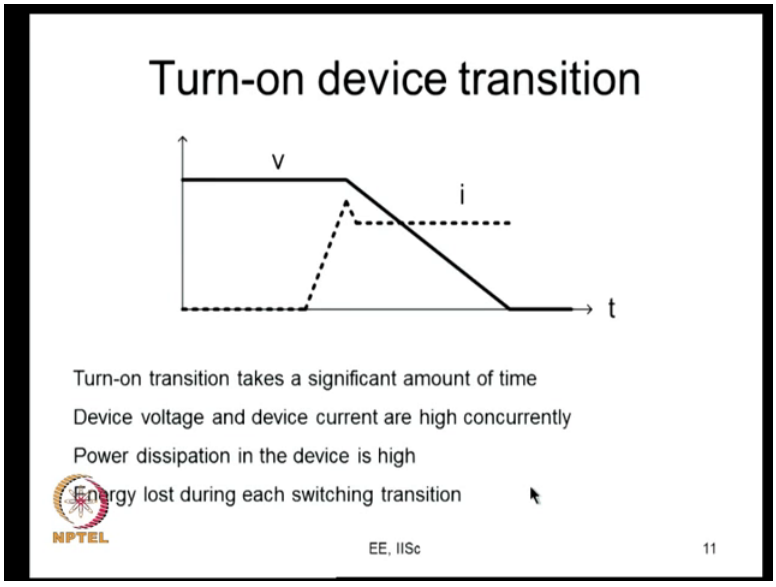

Because the devices are not ideal you need to do something that is introduced dead time. So, what is the non ideality that is affecting us? The finiteness of the transition time, the transition times are not 0, they are significant it takes significant amount of time for the device to turn on.

So, now you are gating signal might have gone high somewhere here and after that the current starts rising and after that the voltage starts following and the voltage eventually falls somewhere here. So, there is certain amount of time and you need to have a dead time duration much higher than this.

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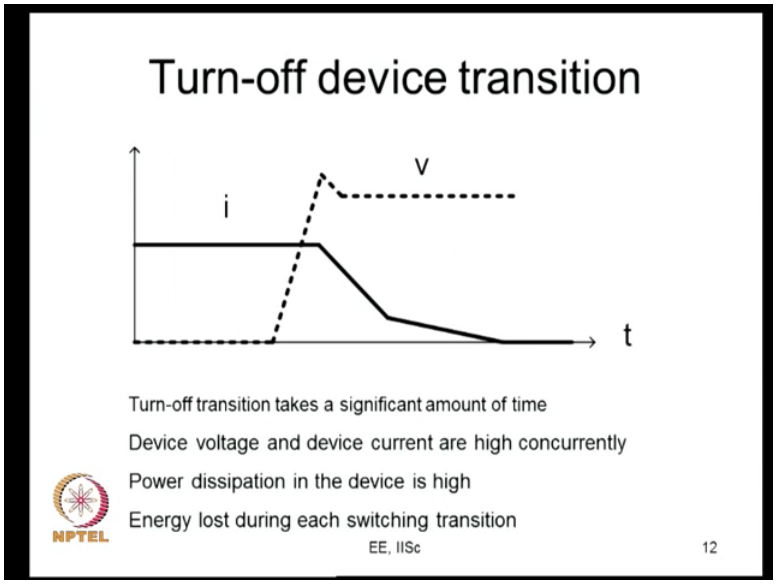

So, R it is better to look at the turning off device because you want that device to be turned off first before the incoming device is turned on. So, what you would do is, so you would have turned off somewhere here and the after certain t d off, off time delay time you will see that the voltage is rising. And after that you see that the current is falling; may be first initially falling sharply and then falling more gradually.

So, it falls here now there is certain amount of time interval you need to wait that is; after your gating signal has been turned low somewhere here, it is here that the device fully turns off. And this time can vary with the voltage level or this current level or the ambient temperature or junction temperature and so on and so forth, it can vary because of certain parasitics in the circuit and you can take no chances. You have to allow for

some time which is much longer than this switching interval and it is only after that time you should turn on the next device so that that device would turn on as shown here.

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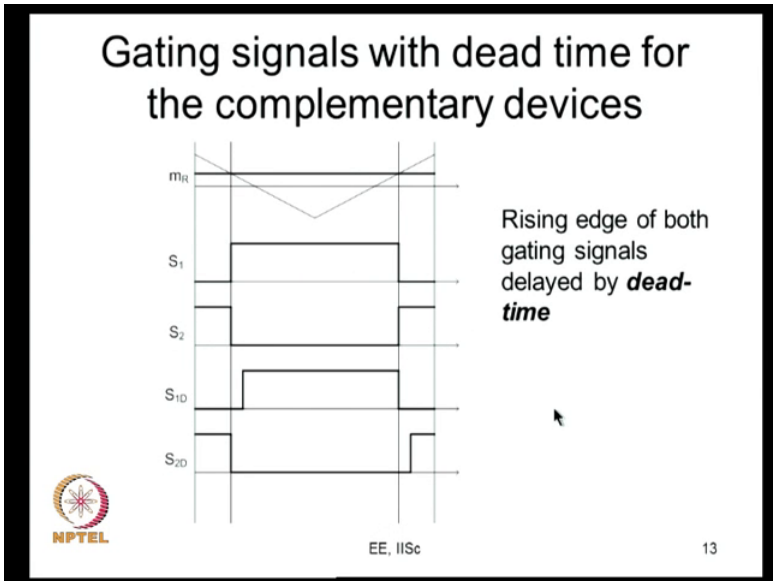

So, that is the idea of our dead time when you do the dead time, what do you do? You turn off, now in this case the bottom devices is to be the outgoing device; you turn it off first. The incoming device is the top device; you do not turn it on immediately, you delay by certain amount of time what you call as dead time.

Again, if you look at this edge the top device is the outgoing device, the bottom device is the incoming device. You first switch off the outgoing device like this; the incoming device do not switch on concurrently delayed by small time; short interval of time. So, this is what you are going to get, so in effect what are you doing? You are delaying the rising edges; if you have S 1 and S 2 you are doing nothing to the falling edges, but you are delaying the rising edges. So, this rising edges delayed by t d, again this rising edges delayed by t d; this is your dead time.

So, this S 1 D and S 2 D are not exactly complementary; in this interval, for example they are complementary, but you look at this interval and you look at this interval; they are not complementary. What else are they? They are equal; equal to what? Both are equal to 0. So, here that will never happen; if this is 0, if this is 0; this will be 1, this is 1, this will be 0. Here after you have introduced delay time, you have the situation where S 1 D is 1, S 2 D is 0 or S 1 D is 0, S 2 D is 1.

You also have the situation S 1 D is 0 and S 2 D is 0, but you will never have the situation S 1 D and S 2 D are concurrently high; what does it mean? Because it means that dead short of the DC bus, in fact your main reason why you are introducing the delay time is; this if you switch them concurrently the complementary devices, it is possible that it might get shorted and that is the reason you are delaying now. So, you do not want to go anywhere close to that 1, 1 where both s the top and the bottom could be high that is why there is now.

So, because of this what has happened? There is certain interval of time during which both the gating signals are low, but the load is an inductive load which is like a current source. During the switching transition, it will just continue to conduct; it will just demand a path for the current to flow through. So, if both the transistors cannot conduct; one of the diodes will have to conduct, which diode will conduct it depends on the direction of current. So, depending on the direction also current either the top diode or the bottom diode will conduct. So, in this interval one of the diodes will conduct and in this interval also the same diode will conduct, assuming that the current direction is the same in both these things now alright; so you go here.

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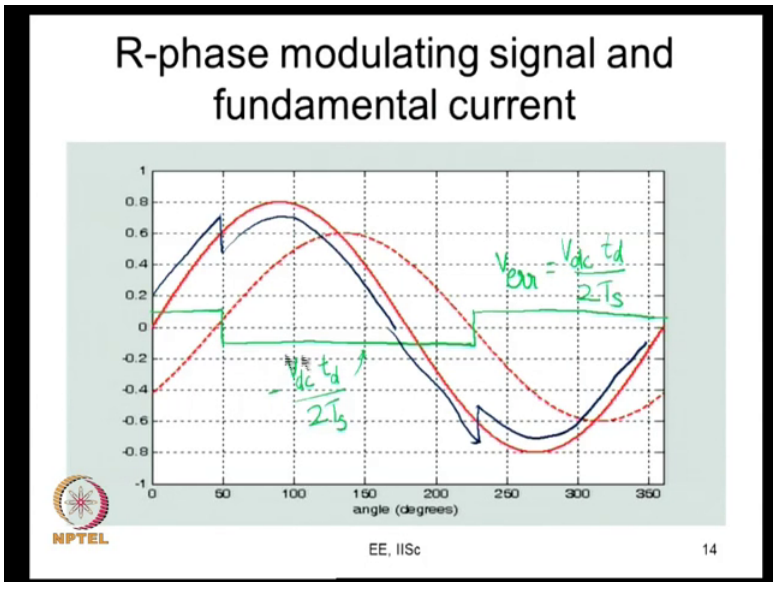

So, it depends on the current direction; so, where there is a change in the current direction. The current direction is negative here it is positive remember, we have ignored the harmonics here. Well it is alright, which is a reasonable assumption which we have

done before. We did this when we were calculating conduction loss, when we were doing DC link current analysis, when we were doing switching loss, all these high switching frequency; in the cases we have ignored the ripple there is nothing no nothing wrong in this now.

But this that will lead to one consequence what is that? If you are considering this smooth sinusoidal current on the fundamental component alone; this 0 crossing is very crisp. On the other hand, there is ripple on top of it, there is a ripple on around that what will happen is; sometimes you will have multiple 0 crossings.

So, this could make some significant difference. So, we normally assume that as I just mentioned here in the sub cycle when you are going to assume; when we did the discussions analyse in the last class and when we will be doing again today. We have been assuming that the current direction is always positive or always negative; it is never going through 0, but it could go through 0. Sometimes it can also go through multiple 0's for example, there is a ripple now let us say this is what? This is one carrier cycle time. So, let us say one carrier cycle is 200 micro seconds or this is 5 kilo hertz now, you also have 10 kilo hertz harmonics; you may also have a small amount of 15 kilo hertz harmonics.

So, if your fundamental current is going through 0 then it is ripple current that matters; it is possible that you may have a ripple current like this; you get my point? I am showing it little a exaggerated. It is quite possible that you have; this may be a very small current may be few milli amperes, but 100 milli amperes, 200 milli amperes; this current may actually fall go down and may go high. So, all these possibilities exist we are ignoring all these possibilities, but that is fine.

So, we are considering this to be a nice sinusoidal current, we are ignoring the ripple component. So, you should bear in mind that sometimes when you are dealing with a situation; when the ripple is high, so some results of this analysis you must question and you must make appropriate modifications to that; that is the reason, I am giving you this warning because there is a inherit assumption; at least note down the assumption.

So, when you are doing an analysis you should at least know the validity of this analysis. So, this analysis is valid when we are considering whenever the fundamental current is predominant and the harmonic currents are negligible; when it is like this. So, now we

can go by this fundamental current, the fundamental current is roughly equal to the actual load current now.

So, there is certain amount of error; how much is that error? This is a small amount of error; is it positive, when the current is positive that error is like this. And then when the current is negative that error changes sine like this. Here again the error changes sine, so what is this error? This is; there is an error between the instantaneous actual pole voltage and the instantaneous ideal pole voltage.

So, we have considered that error between the actual pole voltage and ideal pole voltage. After that we have averaged rate over every carrier cycle, so how much is that value will be equal to? Let us do this, so the error voltage is V dc and that voltage is same for a duration t d in every carrier cycle which is 2 upon; this two times T S; so that is this voltage level, this is actually minus V dc; t d upon 2 T S here you will have V dc times T D upon two T S.

So, let us call this as V error the average error voltage; that is the error voltage which is been averaged over every carrier cycle. So, this is the kind of error voltage; so, what is going to happen? You are not going to get a sinusoidal phase voltage like this; the phase voltage is going to have certain DC component added to that.

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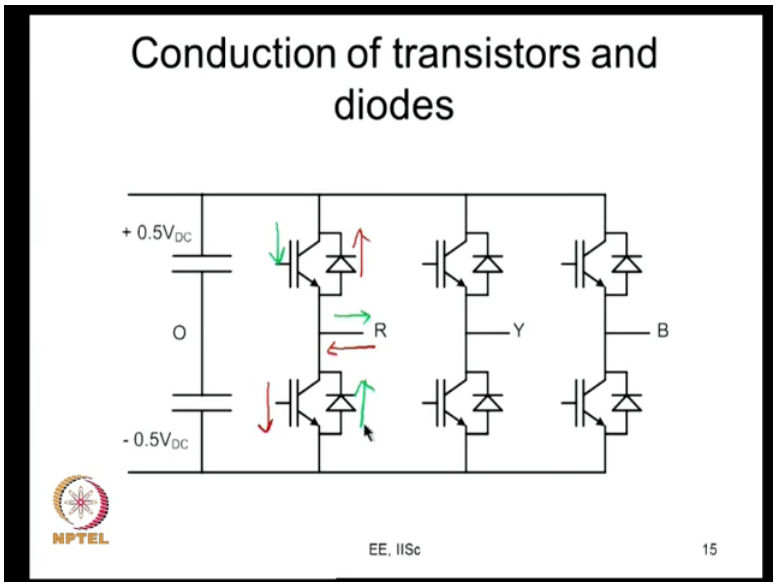

So, this just to go ahead with why whether it is positive error or negative error, we just saw that if this is the direction of current; these two conduct. For the other direction of current, let me change the colour just a moment alright; when this direction of current one of these two will conduct. So, which one will conduct? Whenever the top gating signal, the current is in this direction and the top gating signal is high; this will conduct.

Whenever the current is in this direction and the top gating signal is low, this will conduct. Again whenever you have current flowing in this direction and the bottom gating signal is high then this transistor will conduct. Again if the load current direction is like this and the bottom transistor is low, signal is low the top diode will conduct.

So, that is how the logic is; where active device they will not do this otherwise they cannot conduct now. So, if what is going to happen is the diodes conduct during the dead times. Now in this direction of current, it is this diode that will conduct during the dead time. So, during the dead time whether you like it or not the voltage pole voltage will be minus V dc by 2.

So, ideally it may be plus V dc by 2, but you will have minus V dc by 2; hence the error. Again let us say this direction of current, during the dead time who will conduct? During the dead time, this transistor is not gated high; so, he cannot conduct. So, it is this diode which will have to conduct; so, during the dead time for this direction of current R phase is connected to the positive one and therefore, your pole voltage V R O is equal to plus V dc by 2.

So, during the dead time neither of the two transistors are gated high, only the diode has to conduct which diode conducts? Depends on the direction of current and once you can say which diode conducts, you can say what the pole voltages. So, the pole voltage can be said just depending upon; during the dead time instance can be said based on what is the direction of current here.

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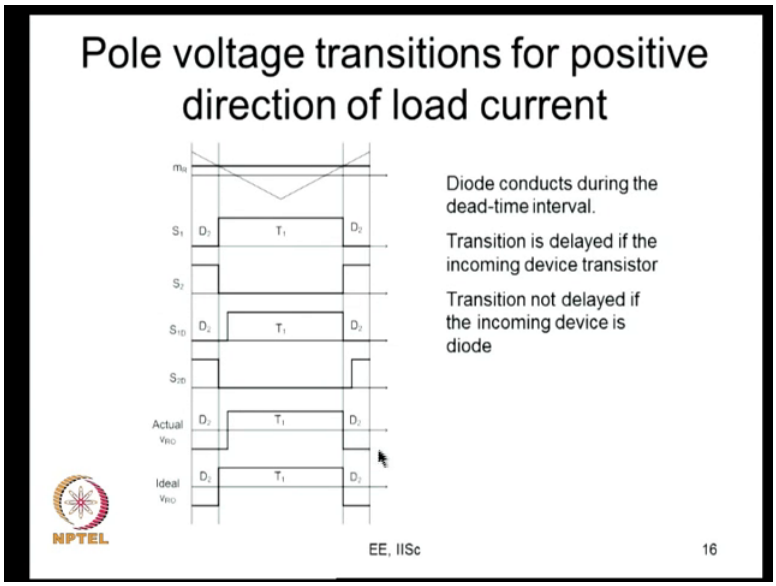

So, now this is where you go your taking a relook at the actual average pole voltage and the ideal average pole voltage now. So, like the diode conducts; so, the diode is conducting here the diode continuous to conduct during the dead time whereas, ideally it should have switched here. So, if there were no dead time between the top and bottom; so it switches here. So, it is here now again, but here what happens the incoming devices are diode.

So, the moment this is turned off, the diode comes in now. So, as I have mentioned before if the incoming devices are transistor; there is a delay the transition is getting delayed; in the pole voltage gets delayed. On the other hand, if the incoming devices are diode it does not get delayed.

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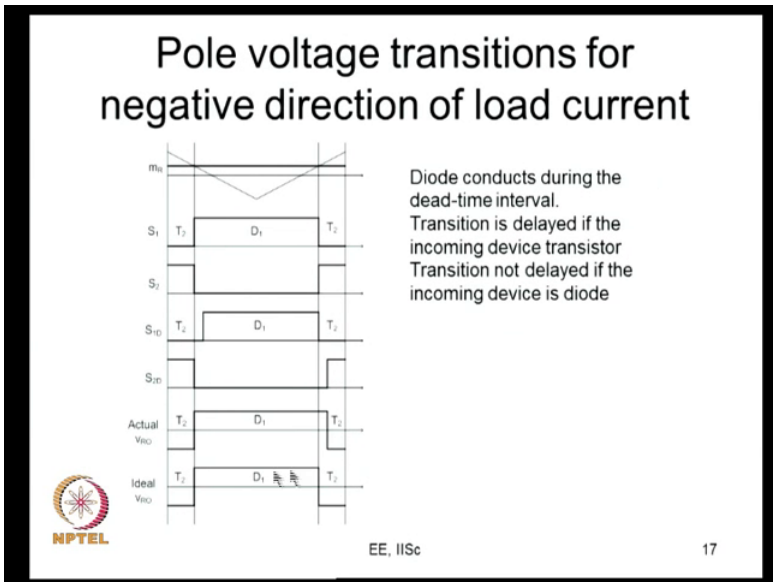

So, this is something which is given for the other direction of current, but the philosophy is same that is during the dead time, it is a diode that conducts. The transition is delayed if the incoming device is transistor; the transition is not delayed if the incoming devices are diode alright.

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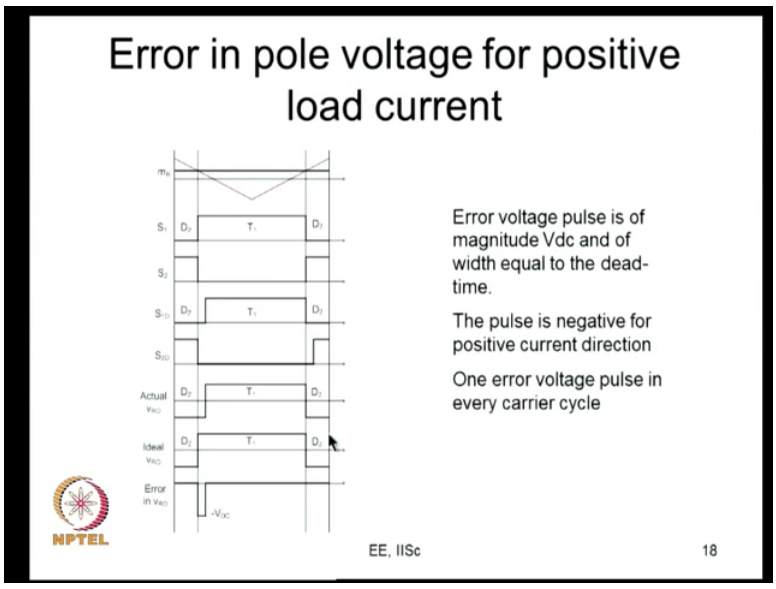

So, because of these rules what happens; whenever your positive so called positive direction load current, the actual pole voltage and ideal pole voltage are like that and you get a negative voltage pulse, there is an error voltage pulse which is a negative voltage

pulse you get. You get one such negative pulse in every carrier cycle and this is our magnitude minus V dc and this is for time duration t d.

Similarly, if you look at the positive load currents then what you will going to get? Your actual pole voltage is like this and the ideal pole voltage is like this the difference between these two will be V dc.

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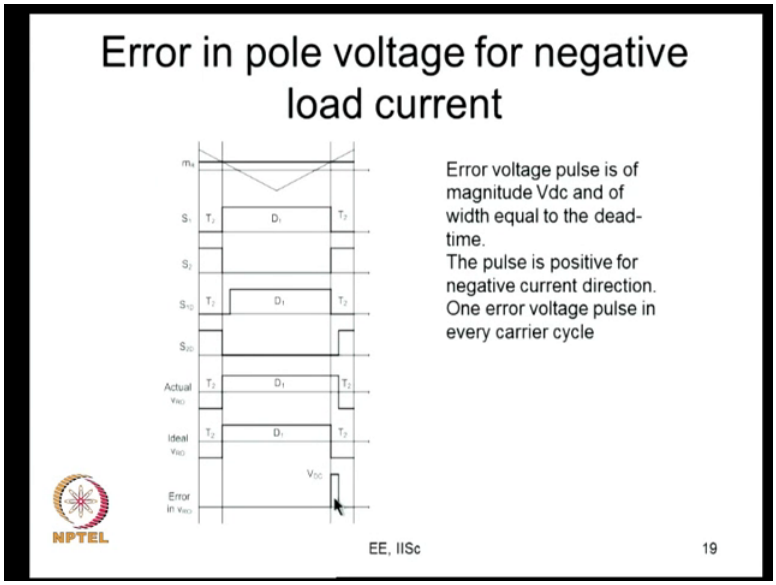

The difference between the two will be V dc, so you will get a; for the so called negative direction of load current, your error voltage pulse is positive.

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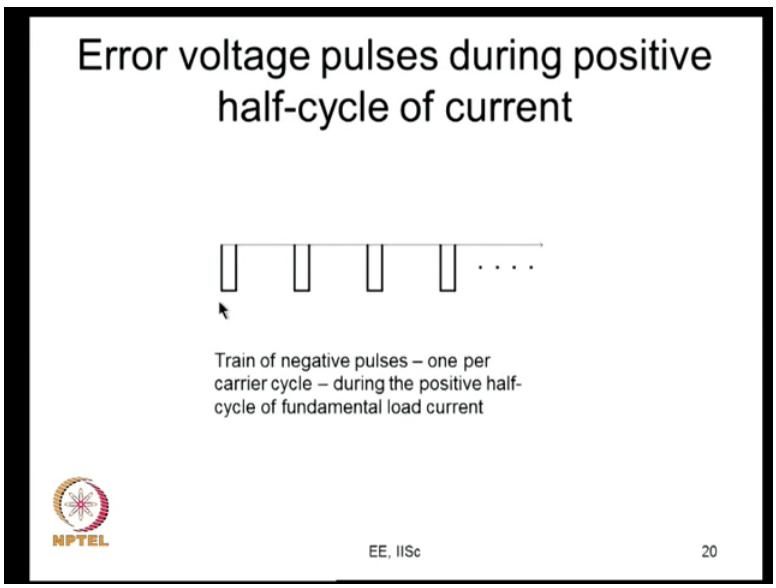

And therefore, you get like this; therefore, you get a train of negative pulses during the positive half cycle of current. So, you will see one error voltage pulse in every carrier cycle.

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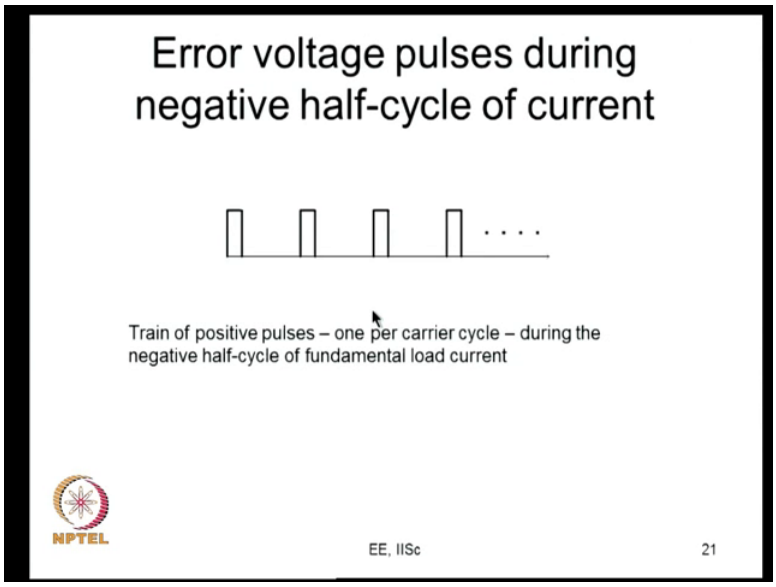

Again if you look at the negative half cycle of the current; you will look at you get one positive error voltage pulse in every carrier cycle.

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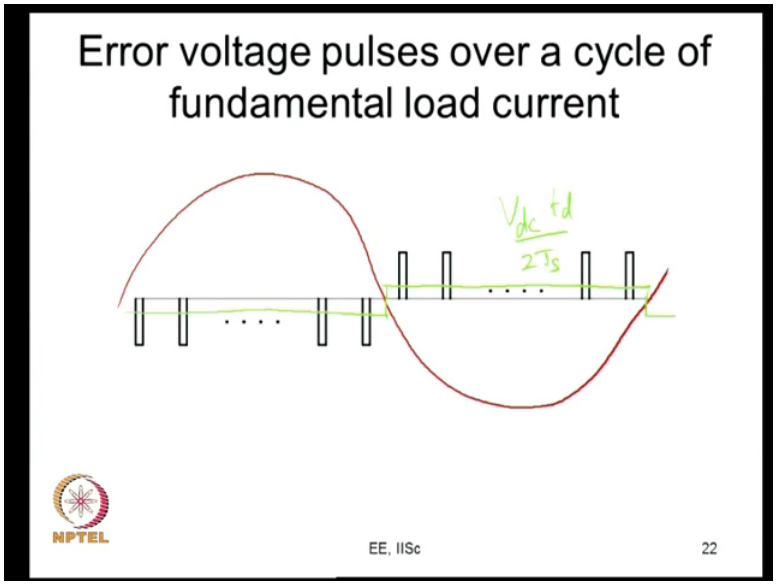

So, this is how you can picturize the error voltage pulses. So, let us say the current is like this; let us say I am sorry let us say the current waveform is like this. This is the

fundamental current waveform, the error voltage pulses will be like this. So, as I said before what we are more interested in this as far as the error voltages are concerned is; we are more interested in the low frequency components of this and not really the high frequency component of this error.

So, you can replace this by a square wave that is what your doing is; you are considering the average value of each pulse over a carrier cycle that is what you are doing. So, this is the average voltage and how much is this average voltage equal to? That is what as I said before V dc time t d upon two T S.

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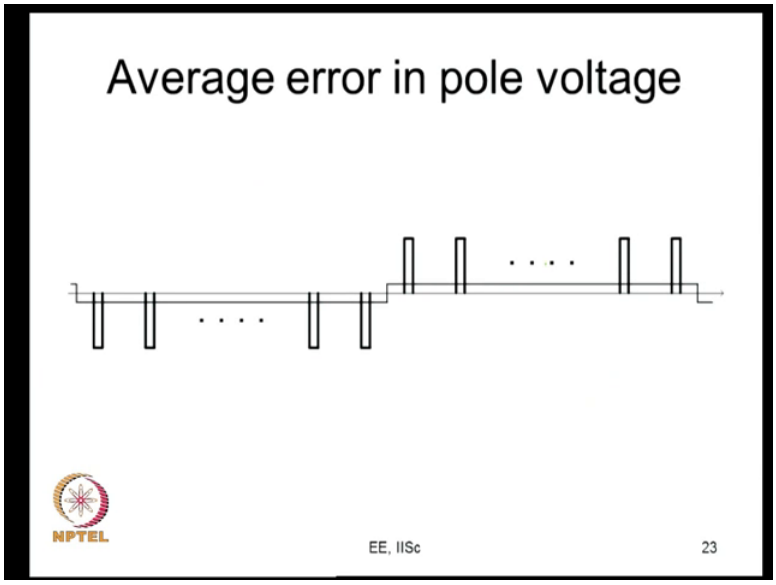

So, which is what is shown in the next slide; so, this is an important information for us and this square wave; gives a measure of how much damage is caused by dead time or how much is the; I mean the fundamental and the low frequency components which have been introduced on account of dead time, at the inverter output. So, this is the reason I drew this before when I did the sinusoidal current, this is what I did. So, this was all that; I have said now were the basis by which I did this now.

So, when I do this what happens the actual pole voltage, if you look at it let me take some other colour. The actual pole voltage is supposed to be sinusoidal as given by this line, but the actual pole voltage will fall down like this. This error voltage will get added to this; like this. So, this is how it will be correct, so it is no longer really a sinusoidal voltage.

So, it is also clear for you like what you can do to compensate now. What can you do to compensate now? What is happening because of the dead time is, the dead time is introducing a square wave which has a particular amplitude and which is in phase opposition with the fundamental current and because of that the average pole voltage changes like this, this is basically a square wave added to this sinusoid.

So, if you want to correct that what do you do? You take this you take the inverse of that and add it to the modulating signal; that is all that you do. Effectively this is what you do for your dead time compensation, so let us go back here.

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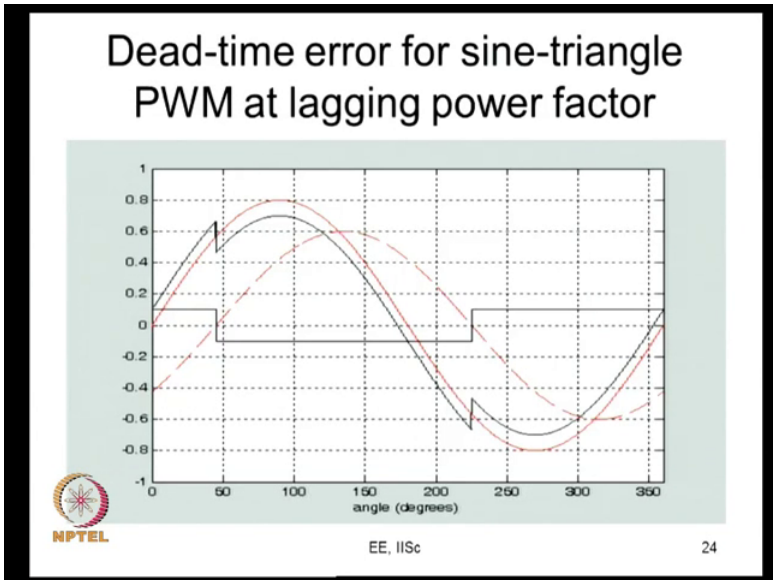

So, these are the error voltage average error in the pole voltage which we saw. So, what we are going to look at is; these are how the variations is, so this is now what I had plotted by hand; here it is shown plotted already. So, this is sinusoidal sine triangle PWM. So, the average pole voltage is expected to be like this, but the average pole voltage actually changes like this.

If you compensate for dead time; that is you add modulating I mean some signal to the modulating signal which is equivalent to the negative of this error voltage, then you can get rid of this error. So, that is what you do when you do dead time compensation here.

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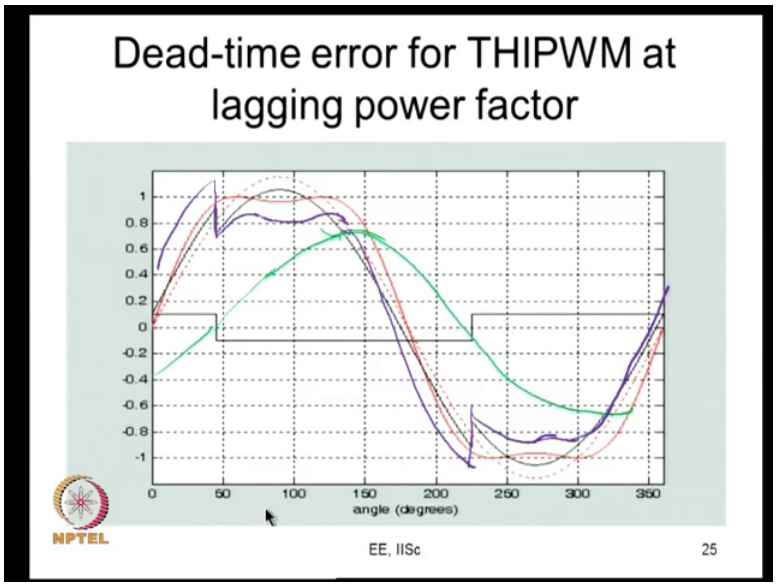

So, this picture shows the fundamental sinusoid; this is the fundamental voltage that you will get. And this is the average pole voltage; the average pole voltage contains several of the harmonic I mean the triplen frequency components. These triplen frequency components will vanish, they are in the average pole voltage they will vanish in the line to line voltage and the load applied voltage.

So, in the load when it is you look at the phase neutral voltage; you will get this sinusoid this is what you will get ideally. Now, this sinusoid actually whereas, this kind of thing added up now, but of course the third harmonic components which are there in this will not be seen. So, the black waveform here is this sum of the ideal sinusoid waveform plus the square wave added up there. If I want to plot exactly the average pole voltage what I should do is; I must add this you know here of course, the current assumed is like this; let me just draw the current here, so the current waveform assumed is like this.

So, if I actually want to draw the average pole voltage the error is negative here. So, you consider the actual modulating signal in this modulating I think I should change the colour. Choose some other colour like here, this is the actual modulating signal; this is the representative of the average pole voltage. Now the average pole voltage will be something like this, this is how the average pole voltage will be. And here the average pole voltage will shift sine; so, the average pole voltage will be something of this nature.

So, I am trying to sketch something like what would be the average pole voltage. So, this average pole voltage; it contains fundamental component, triplen frequency components which are part of the modulating signal; the common mode components and it also has a square wave and all the frequency components that are added here.

So, from this average pole voltage; if I go to average line to line voltage, similarly the Y phase will also have. So, if I subtract V R O average minus V Y O average; what will happen is the fundamental will be intact. So, but the triplen frequency components the entire amount of the common mode component will go. And also the third harmonic, ninth harmonic, fifteen harmonic components etcetera, the triplen frequency components in this wave form will go away; so remaining will be there.

So, this contributes to certain amount of fundamental voltage which will get added up to this fundamental. And again this square wave will contribute a certain amount of fifth harmonic, seventh harmonic and so, on they will actually get added up to this sine wave and they will result in low frequency distortion.

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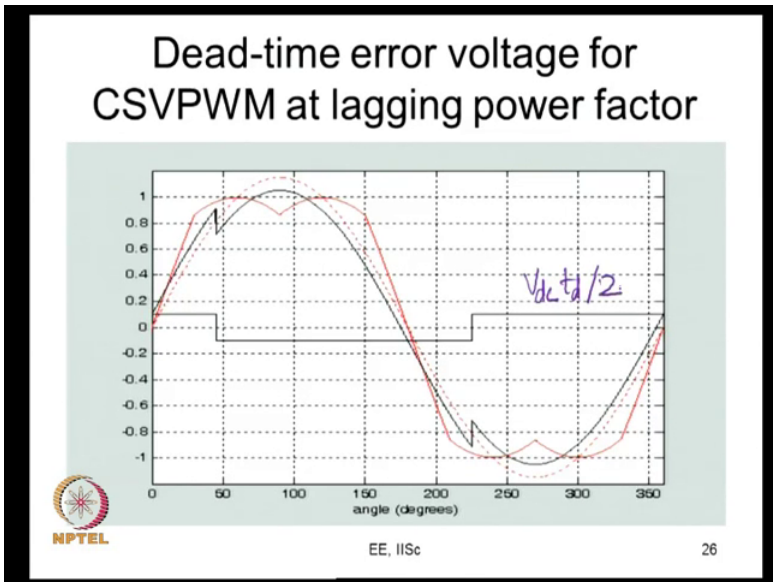

So, this is again we have given the; conventional space vector PWM and this is how the dead time error voltage is.

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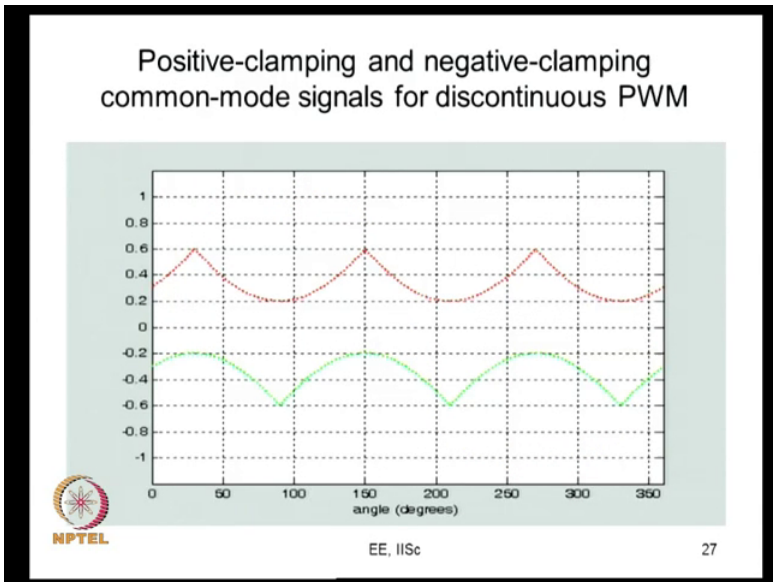

So, now it is the main thing that we are supposed to actually go into; that is bus clamping PWM. So, in all these cases what you have? You always have this as a square wave; the error voltage is a square wave and how much is that? That is actually given by V dc, t d upon 2 T S; this is what it is given by. When you go to this bus clamping PWM things are little different as we will see; why? One of the phases does not switch at all which phase will not switch? That depends on which common mode signal you have added, if you added this common mode signal; one phase will be clamped to the positive bus. And whichever is got the maximum of the three sinusoidal modulating signals, there is one phase which will have the maximum sinusoidal signal and that phase will go get to a positive bus.

Again if you are adding this common mode then of the three if the sinusoidal signals; one wave will be most negative that will get clamped to the negative bus. We fall this for 60 degree, this for 60 degree; again follow this for 60 degree and 60 degree this is what we have been doing.

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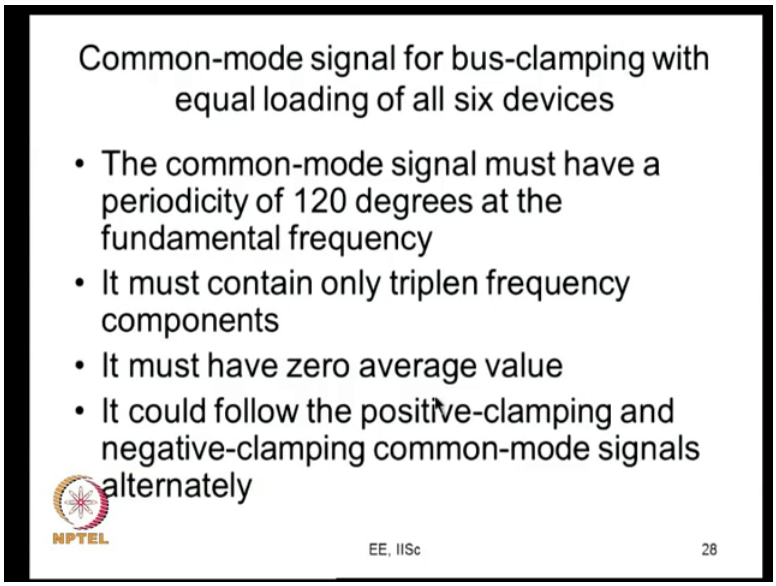

And that is what has been discussed here. So, we have a triplen frequency waveform common mode component added to that and we make sure that all the 6 devices get loaded equally that is; the common mode component will make sure is of periodicity 120 degree, it contains only triplen frequency components, it does not contain any DC component we make sure and we do this.

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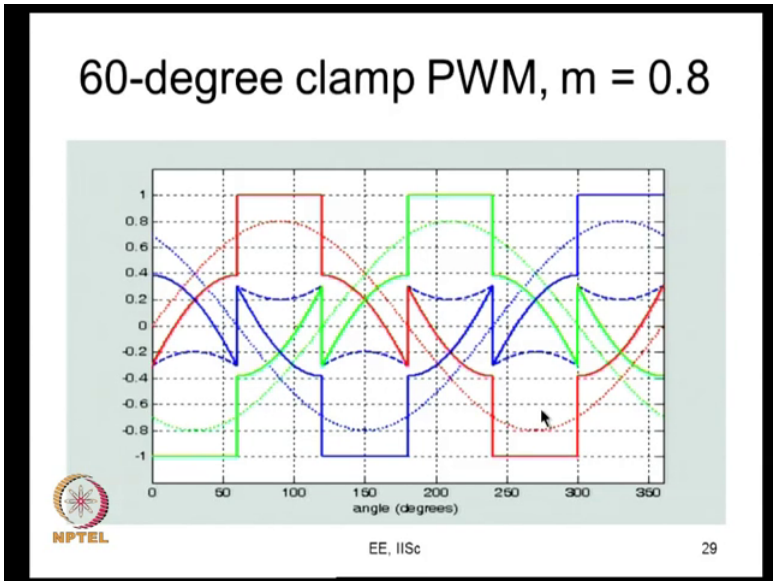

We apply range of PWM methods, so this is the so called 60 degree clamp PWM or sometime called DBWM 1, where a phase is clamped at the middle 60 degrees everywhere now.

So one wonders how will dead time affect here. What is the significant difference between here and there? Now the PWM signals you see it is clamped. Earlier when we saw the error voltage, the error voltage did not really depend on the duty ratio. Whether the duty ratio of the phase was 0.7 or 0.8 did not matter, again whether the current was 10 ampere or 15 ampere did not matter, what only mattered was the direction of current.

The direction of current determined the sine of error voltage and what was the error voltage? The magnitude of the error voltage was determined by the DC bus voltage, the dead time and the switching frequency. So, these are the ones that determined here; now this is a special case where duty ratio is 1. When duty ratio of R phase is 1; what happens? R phase top devices conducting all through it does not switch at all.

So, when it is not switching at all what is the actual pole voltage? Plus V dc by 2; what would be the ideal pole voltage? Same as that, so plus V dc by 2 because of phase does not switch at all. So, there is no you know changes in the switching transition only if the phase switches then you will have to worry about whether it will switch at the same instant or it will be delayed by t d. During this interval of time R phase does not switch at all; so, the R phase pole voltage actually and ideally in both sense, it is always equal to plus V dc by 2.

So, in bus clamping PWM; if you are looking at the error voltage; average error voltage for R phase, there will be no error voltage here. On the other hand will there be error voltage here; yes there will be error voltage in this part, there will be error voltage in this portion, there will be error voltage in this portion. Once again there will be no error voltage here because R phase bottom devices continuously conducting, there is no switching at all.

So, there is no error voltage here the same thing can be said about Y phase. The Y phase will have no error voltage here and here, B phase will have no error voltage in this region excuse me and in this region.

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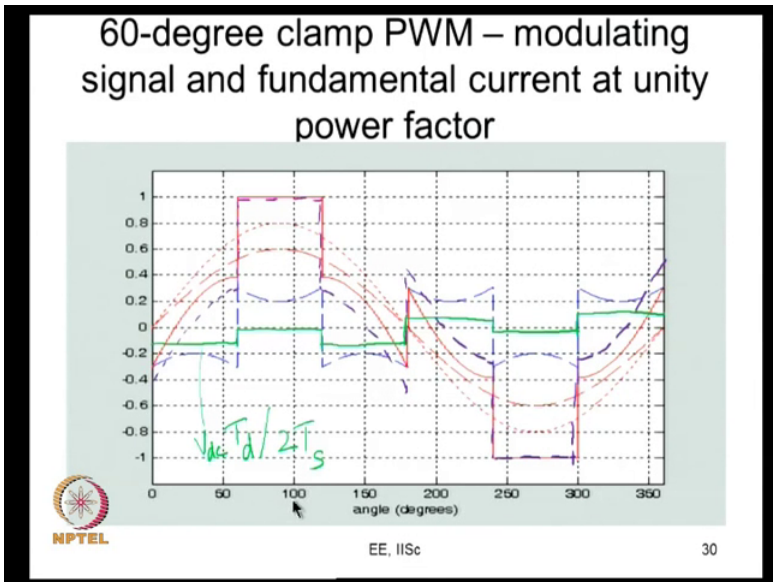

In other regions R phase has an error how much will that error be? It will be the same thing as before. It will be V dc multiplied by t d upon 2 T S and the direction or the polarity of the error voltage will depend upon the direction of current. So, now let us take one case what is this? 60 degree clamp PWM again. Here we had all the three modulating signals before, it is easier if we look at just one modulating signal that is the R phase modulating signal.

So, what is this? Actually there are many things, so let me explain it a little clearly. This is the original R phase sinusoid, you see that something of amplitude 0.8, this is the original R phase sinusoid. Now what is done is; the Y phase and the B phase sinusoids are not shown, you are getting the bus clamp; the common mode signal is being subtracted. So, you are following the positive common mode here, you are following the negative mode and this is the positive common mode and the negative common mode.

You going on like this and this is your common mode shown by this; this blue colour. This common mode is added to all the three modulating signals. The others signals are not shown Y phase is alone is shown, when I add this common mode signal to this R phase what I am going to get? I am going to get a modulating signal for R phase which is like this. It is discontinuous here hence the name discontinuous PWM, it clamps the R phase to positive bus for 60 degrees and clamps it for 60 degrees here.

Because it clamps the particular each phase to; one of the DC buses, you call it bus clamping PWM. And since it clamps for 60 degree durations continuously you can call it as continual clamp PWM and is this 60 degrees is in the centre of this, 180; I mean the positive half cycle.

So, we call it 60 degree clamp PWM here; so, when we say 60 degree clamp PWM. We mean a phase is clamped during the middle 60 degree duration of it is positive half cycle and again during the middle 60 degree duration of it is negative half cycle, so this is the modulating signal.

So, the R phase switches here, here the duty ratio is changing. The duty ratio is 0.5 here, the duty ratio is lower than 0.5 here, the duty ratio is greater than 0.5 here alright. Here the duty ratio is 1, then the duty ratio is something like 0.7 or so here and it falls, it comes to 0 and it goes something here. And the duty ratio is suddenly changes at this instant; from here to there, that is the effect of discontinuity.

Once again the duty ratio starts falling it goes somewhere here. So, the duty ratio would be something like 0.3 and then it jumps to 0; it is 0 here. This is the R phase duty ratio as you go along this now. So, whenever the duty ratio is something like this; it does not matter as far as the error voltage is concerned. Because there is going to be some error voltage, whenever the duty ratio is 1; there is no switching therefore, there is going to be no error voltage; again here there is going to be no error voltage now.

So, error voltage is positive and negative who is going to decide? The current, now we have considered a situation where we are looking at unity power factor current and so this is the current waveform that is shown. Since both of them are in red, the fundamental modulating signal as soon as current; so, that is the reason I am showing it clearly to you.

This is the modulating signal and this is the R phase current excuse me; so, this is the R phase current, so it goes around like this now. So, now this is the positive direction how should your this thing be based on your previous analysis? Let me choose some colour, should it be green let me choose green colour.

Now, the current is positive here therefore, I will have an error voltage that error voltage will be negative here. So, what will be in the next 60 degree range? I have done for 0 to

60; 60 to 120 what should I do? The current is continuing to be positive; one would expect this to continue here. The same minus V error, but this is a discontinuous PWM and the R phase is clamped here. And therefore, it has no error voltage here; the error voltage is 0. This is between 60 and 120 degree; now you go between 120 and 180 degree, what happens? The phase comes out of clamping and the current is positive and therefore, you will have you error voltage like this; this is what it will be.

Now, the current has a 0 crossing and therefore, the error voltage also changes sine and the error voltage is positive here. Again in this interval R phase is clamped though to the negative bus therefore, the error voltage is 0 and once again the error voltage is positive like this. And how much is this error voltage? As before it is V dc; t d upon 2 T S; this is what it is.

So, this is the nature of error voltage and now what you have is this error voltage is getting applied, what you are going to get is not this sinusoid, but along with this modulating signal; this will be your average pole voltage, but on top of it this error voltage is also getting added. So, this is what will happen now, if I do that let me choose another colour of ink. So, if I subtract this error voltage what happens? I get something like this.

So, here there is no error voltage; so, here it is no error. And what happens here? It switches up then there is positive thing here, the error is positive then the error is 0 and once again the error is positive. So, what is it that I have drawn here? The original red one is the modulating signal and it is the scaled version of average pole voltage. This is modulating signal already normalised with respect to the peak of the carrier, you multiply this by V dc by 2; this is your average pole voltage V R O average alright.

Now, what we are going to get is average pole; this is the ideal average pole voltage, but the non ideal average pole voltage and account of dead time is what is shown by here. So, what is the effect of this? It is certainly going to change the line to line voltage; it is certainly going to change the line to neutral voltage that is applied on the load. So, in effect what happens is you see this wave; this is no longer a square wave, it is sometimes minus V error; 0 minus V error plus V error 0 and plus V error. So, but nevertheless it has a fundamental component. So, that fundamental component will be reflected in the lower voltage also.

So, the fundamental component is going to change; this will have third harmonic, ninth harmonic etcetera; they will get cancelled off, but this will have fifth harmonic and seventh harmonic; they will get applied across the load. So, the fundamental component of this error voltage fifth harmonic, seventh harmonic etcetera will get applied onto that. And therefore, there is going to be low frequency distortion as we mentioned before, the main difference between continuous clamp PWM and discontinuous; in all the continuous clamp PWM, you found this error voltage to be a square wave.

This V R O as constant and it was negative for the positive currents and it was positive for negative currents, it was a square wave. It was only shifting in phase, but now you see that it sometimes goes to 0 also; that is a significant difference between bus clamping PWM and these ones.

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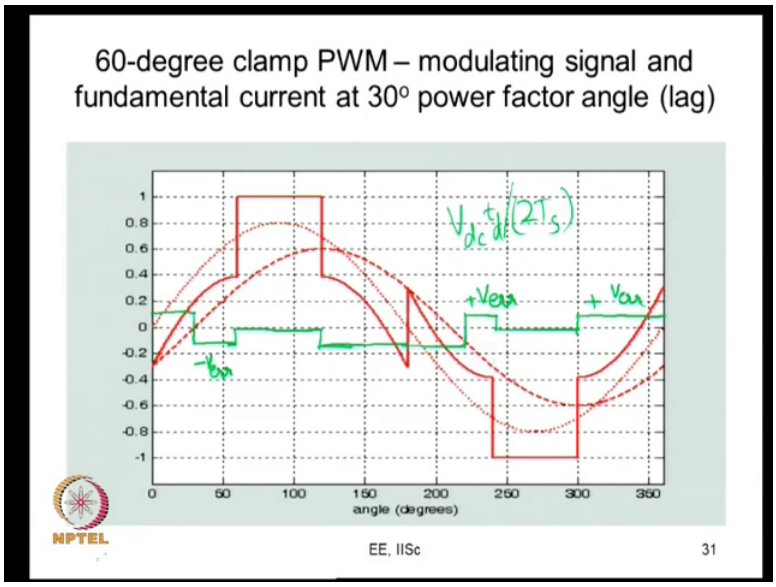

So, let us now look at the next example the same 30 degree and 60 degree clamp PWM, but at 30 degree power factor angle now; so, let me do this error voltage business. So, what is the error voltage here? First consider 30 degrees; so, what is the direction of current? The direction of current is negative up to this point and therefore, my error voltage will be positive.

This is the current; so, here the current changes direction therefore, the error voltage becomes negative. So, this is my minus V error; average voltage the same V dc; into t d upon 2 T S that I wrote now. In this duration, the R phase is not switched at all therefore,

it is like this, now what happens? The direction of current has changed; let me be clear where is the direction of current. This is the current waveform, up to this point is negative; here it changes and therefore, the error becomes positive, then it is like this up to this point. Now here it is clamped, the phase is clamped and therefore, the error is 0 once again it goes like this.

So, this is plus V err; here also plus V err and what is this V err? 2 T S you know V dc, t d divided by 2 T S; same as before, but the wave shape is different. So, this itself was different from what we had, it is not a square wave; it had 0's. Now you see this same 60 degree clamp PWM, but at a different power factor; you have this. So, the nature of this error voltage waveform now depends on the PWM method and even for a particular discontinuous PWM method, it depends on the power factor angle.

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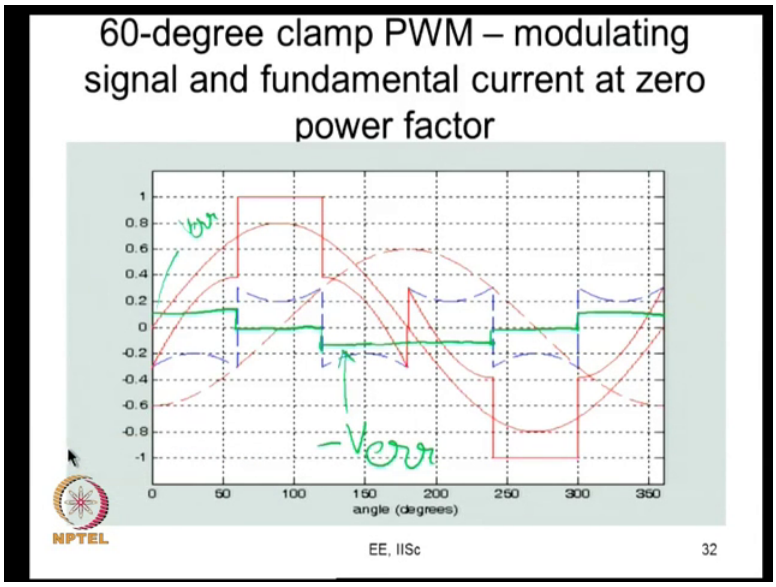

You can do this exercise quickly for let us say another power factor. Now where is the current waveform? This is the current waveform; this is represents the fundamental voltage, this is fundamental current now; so let me do this. Since the current is negative here I should have positive voltage here. So, the positive error voltage is positive, but only up to this point; now it is clamped. so it is 0. Here the error voltage is negative; it continues it goes on like this, it is negative. So, here the error voltage is 0; so, here the current direction is negative and therefore, the error voltage is positive.

So, once again I should emphasize that this is V error as before and this is minus V error as before, but these value has not changed but the waveform has changed that alright.

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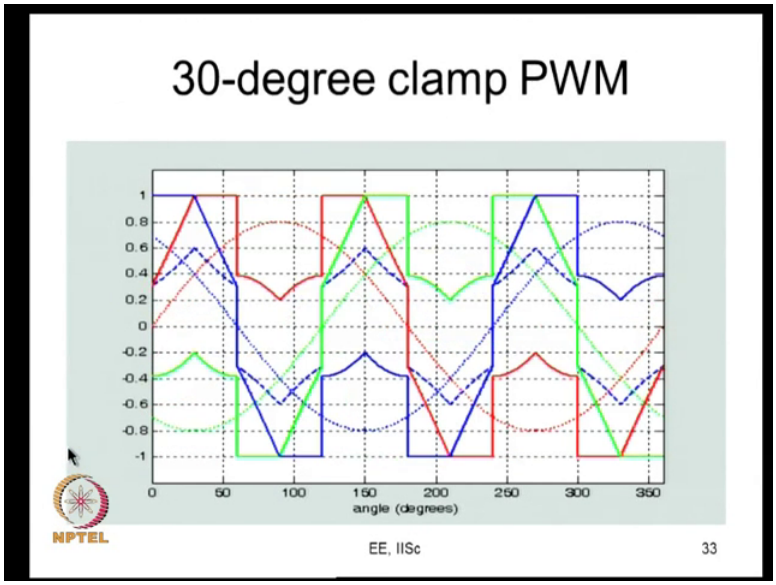

So, let us look at another case; this is 30 degree clamp PWM; what happens here, the phase is clamped between 30 to 60 degree and 120 to 150 degree; when here R phase is clamped. So, in the middle 30 degree of every quarter cycle 0 to 90 degree is one quarter and in the middle 30 degree; that is 30 to 60 degree it is clamped again in the middle 30 degree of the next quarter it is clamped. So, that is 30 degree clamp PWM.

Another very nice PWM method, this is the PWM method which gives you the lowest harmonic distortion among all the bus clamping PWM methods as I have mentioned before.

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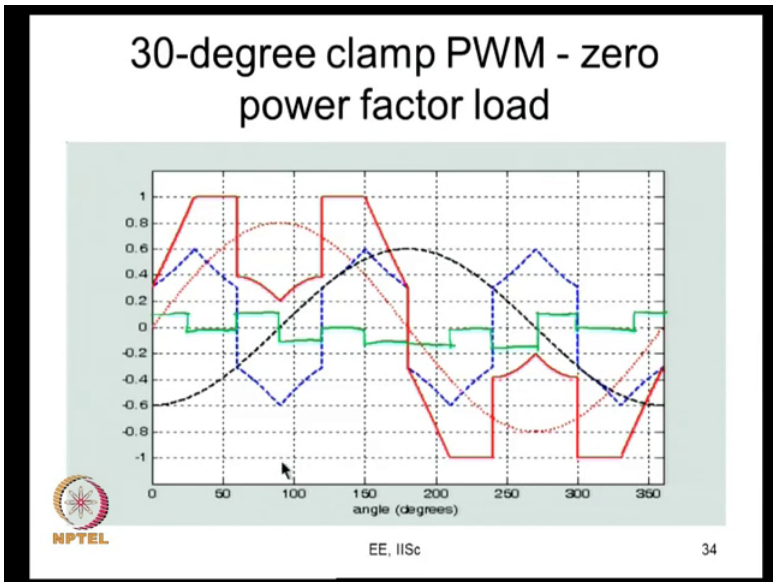

So, now let us say you consider 30 degree clamp PWM and you consider 0 power factor load; how is that if you do that exercise? How are you going to get it? Let us say I will choose the same colour here fine.

So, the current is negative here; the current is shown in black colour, the current is negative therefore, you would expect the voltage to be positive the error voltage to be positive. But since the phase is clamped here; the error voltage becomes 0 again what happens? It is positive. At this instant, the current crosses 0 and therefore, the error becomes like this the error is now negative; once again the error is 0 because the phase is clamped.

So, here what happens subsequently the current is positive, the error voltage is negative like this. And it goes on; it goes on here the error voltage is once again 0 because the phase is clamped and now the current is negative therefore, it is like this. Here the current changes direction, the error voltage changes sine and once again the error voltage is 0 because of clamping and then it goes like this.

So, you look at this waveform now you look at this is plus V R, V error 0 plus V error minus V error 0; here it is minus V error 0 minus V error plus V error 0 and minus V error; those are the values. This waveform is very very different from the previous waveforms you have seen. So, this shows that when you change from one PWM method

to another PWM method; one bus clamping PWM method to another bus clamping PWM method is the waveform is going to change very significantly.

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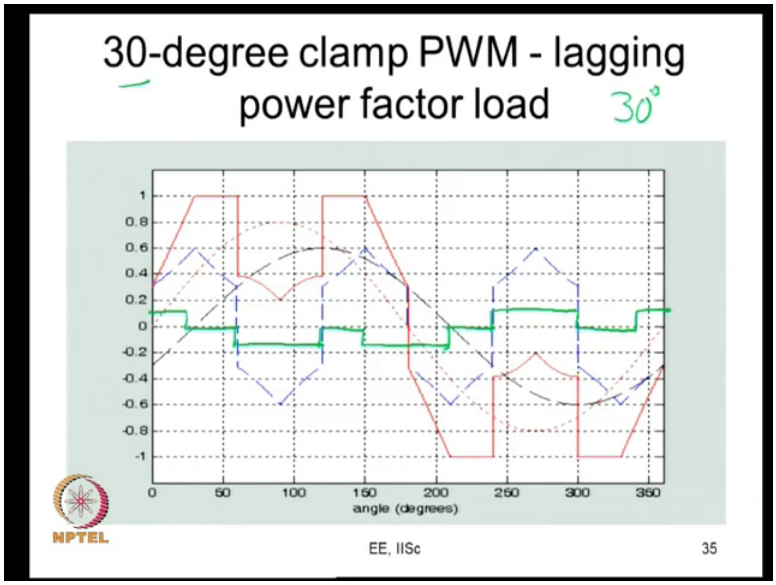

In the same way you can do this exercise for 30 degree clamping PWM for some other value of that. So, here again I have negative current; so, let us quickly identify wherever you have clamping. So, wherever you have clamping it is 0 that is one way of doing it quickly, so the error voltages are 0. Now here the current is negative and therefore, it is positive here the current is positive therefore, this is negative, here the current is positive therefore, it is negative; yes here the current is negative, this peak and so, positive.

So, this is the error voltage waveform for the same 30 degree PWM, but it is some lagging power factor angle this is incidentally 30 degree lagging angle; so, you see how it differs.

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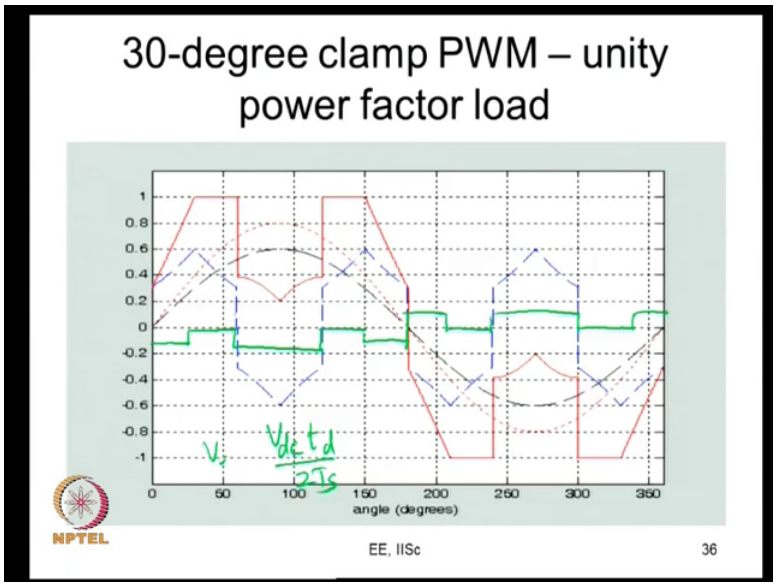

You can do this exercise for any given bus clamping PWM that is any modulation signal and any power factor. Again we have this of unity power factor; so because the phase does not switch, there is no error voltage in this regions means this is switch, there is no error voltage in this regions. Then you have positive; therefore, if the error voltage is negative here; again the current direction is positive means negative here, the current having negative the current changes sine; the error voltage changes sine. So, the current is like this, error is like this.

So, now, you see at a different power factor the same 30 degree clamp it is different now, but the V error value is still the same. Even it still depends on the same thing; V d s into should I write it again? Is the same V dc; t d upon 2 T S; that is given V error.

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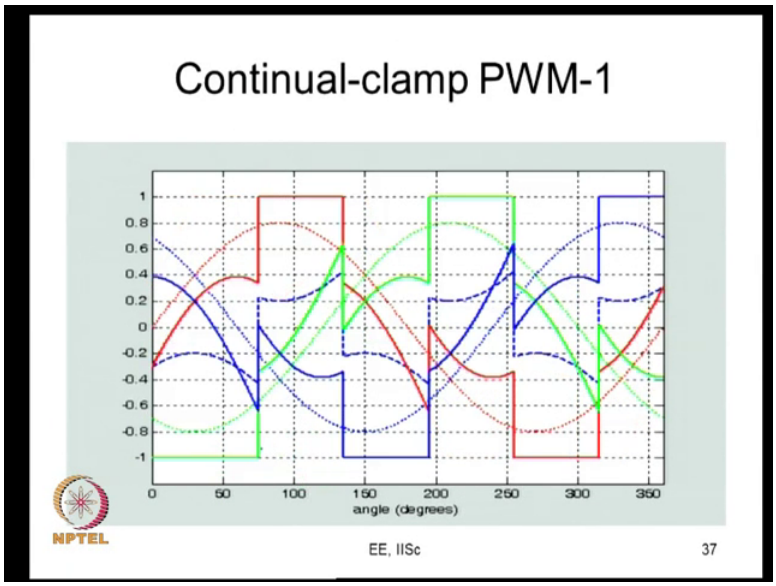

So, you can do this for anything, this is continual clamp like where you have clamped like this continuously for 60 degree.

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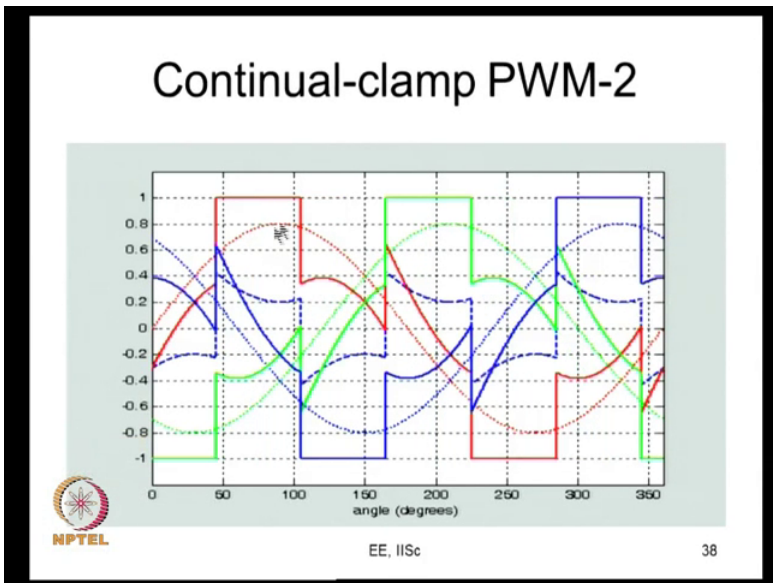

And this is continual clamp where this is; when we saw for switching loss, this is for the lagging power factor load this is to reduce switching loss and leading power factor loads.

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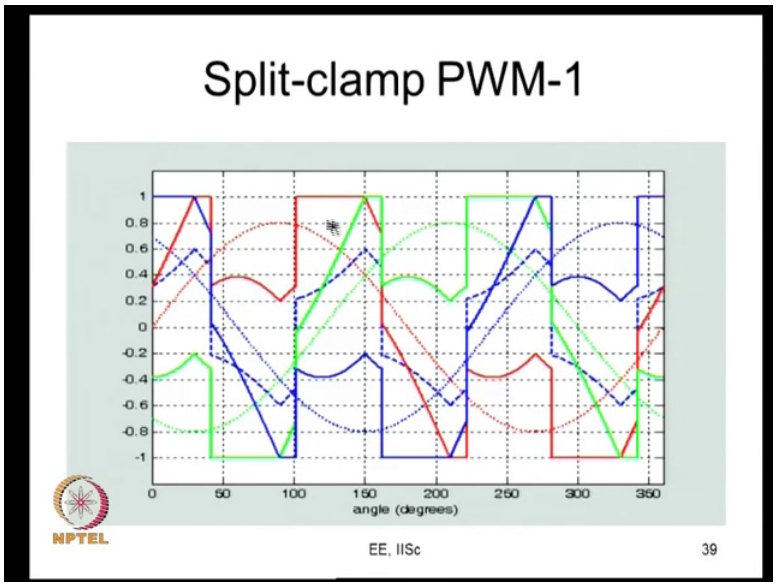

This is split clamp PWM which is good for from the point of view of switching loss, it is good for a loads having power factor angle between 60 to 90 degree.

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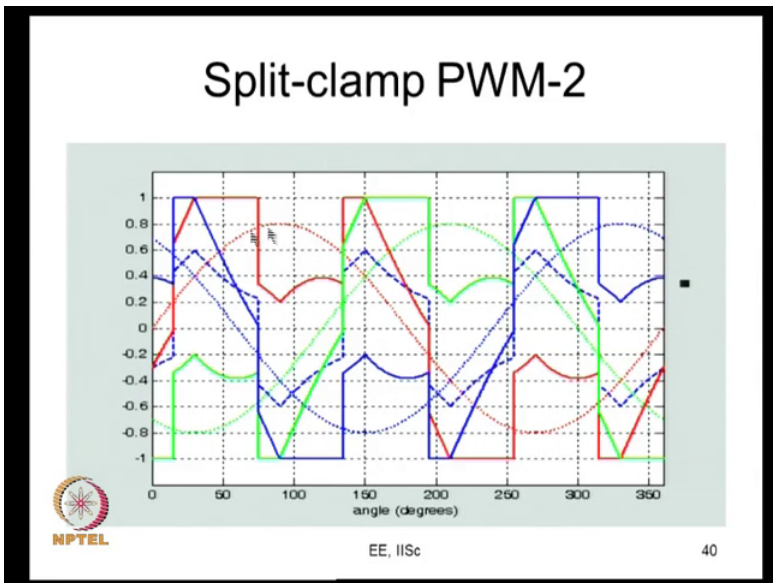

And this is for 90 degree lead; it is I mean this is peak clamp 2, here the sum of these two clamping durations anyway add to 60 degree.

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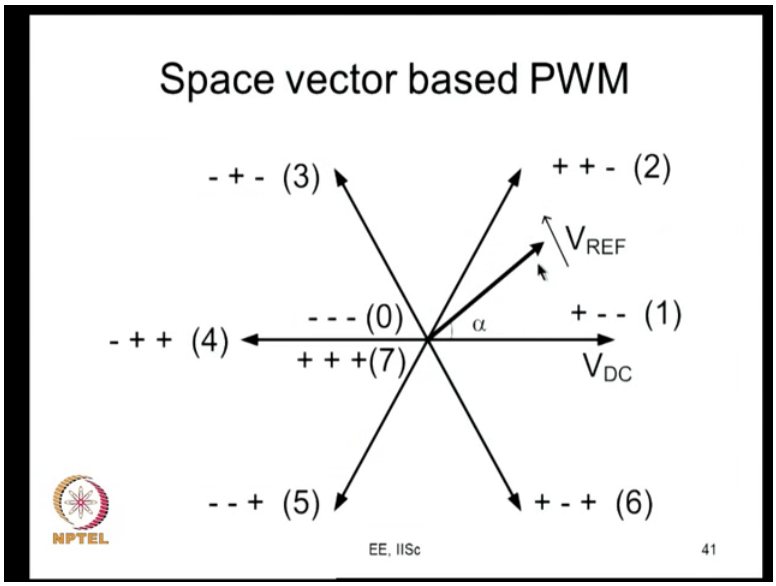

And this continual clamp and split clamp can be seen on this space vector domain. So, where you have a revolving reference vector you sample it.

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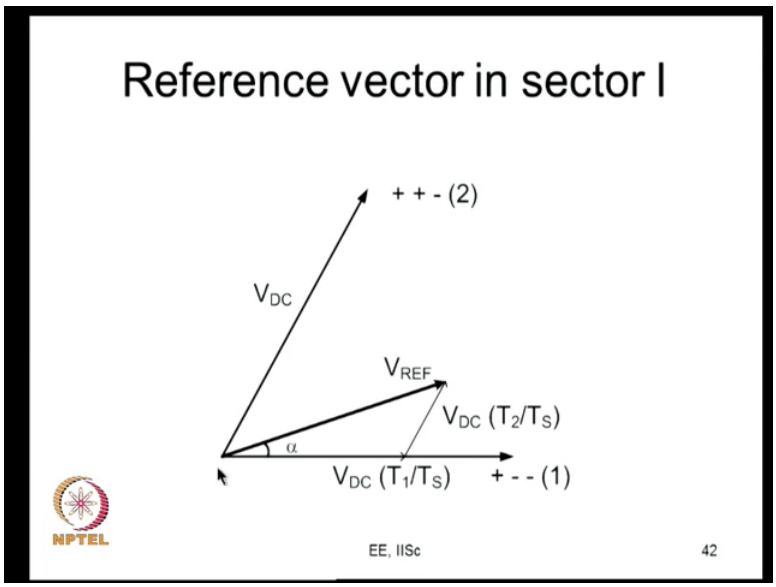

And you time average these vectors and produce the reference vector.

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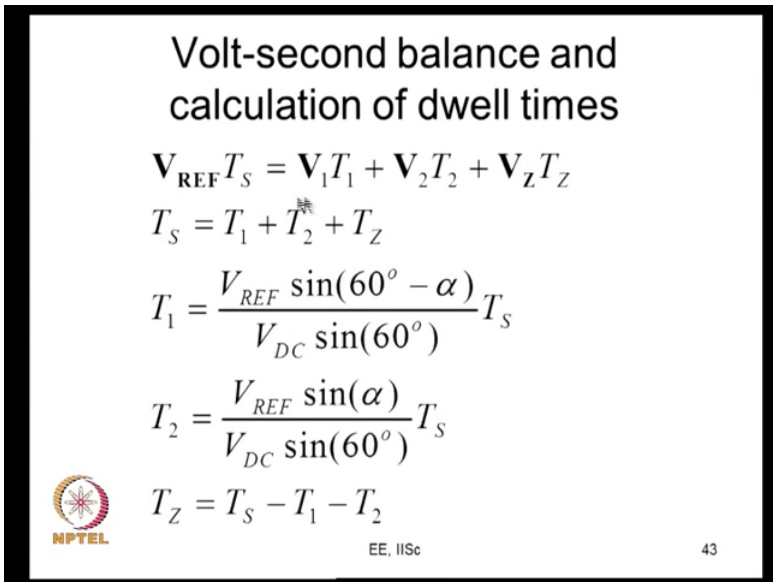

And that for time averaging these are the equations, you apply the three vectors like T 1, T 2 and T Z; as shown before as we have discussed all these many times over the space vector module this based PWM module.

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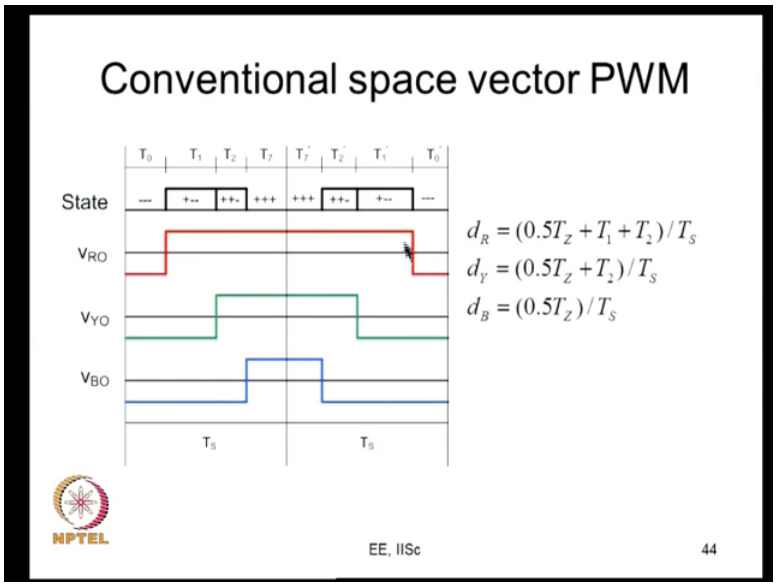

And you are applying your inverter states like 0, 1, 2, 7, 7, 2, 1, 0; so all.

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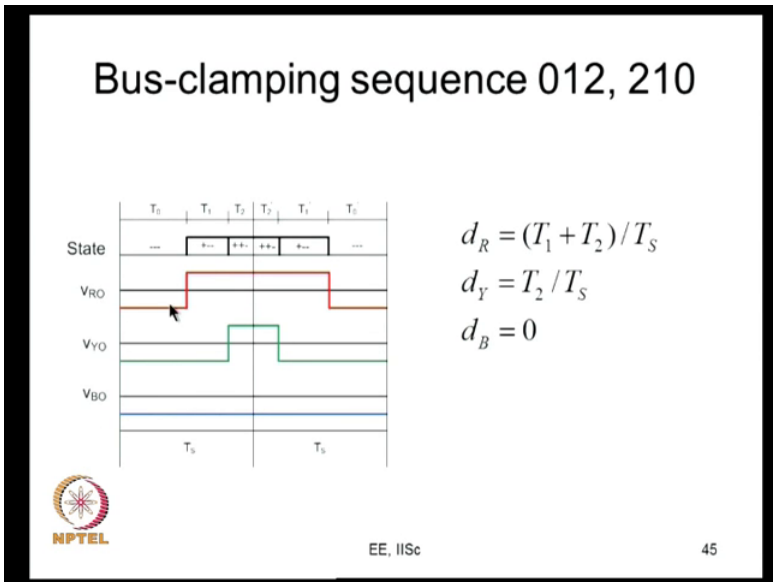

With bus clamping sequences; you apply them as 0, 1, 2, 2, 1, 0, and so on.

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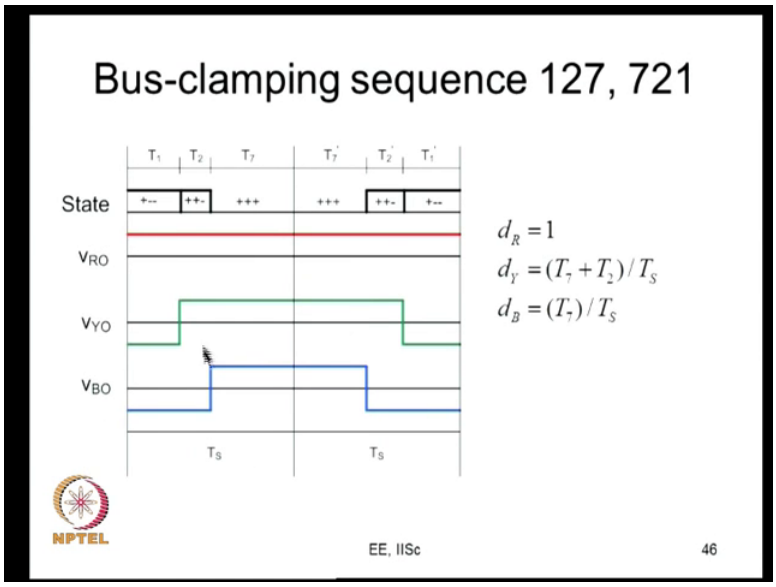

So, the switching sequence is 0, 1, 2, 2, 1, 0 and switching sequence is 1, 2, 7, 7, 2, 1.

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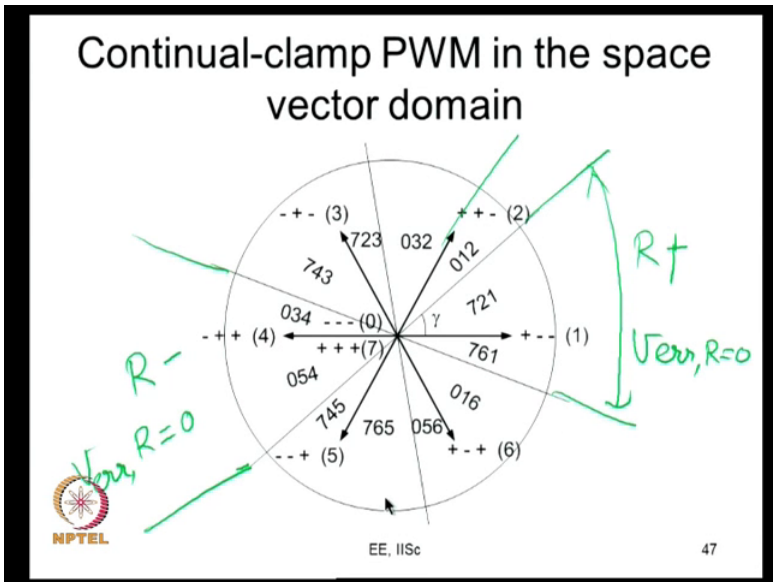

So, now if you look at the continual clamp in the space vector domain, what do you have? This is how you can look at, this is continuous PWM; so, here there is this region over which R phase is clamped to positive bus. And again this is the region over which R phase is clamped to the negative bus, you can see that it is clamped to positive. So, here what you will have is V error for R phase will be 0 in this region.

Again V error for R phase excuse me; V error for R phase is 0 in this region. In the other regions, it will be for R phase V error in this region for example, it will depend on the current direction, it will be plus; I mean plus V dc; t d by 2 T S or minus V dc by 2 T S now.

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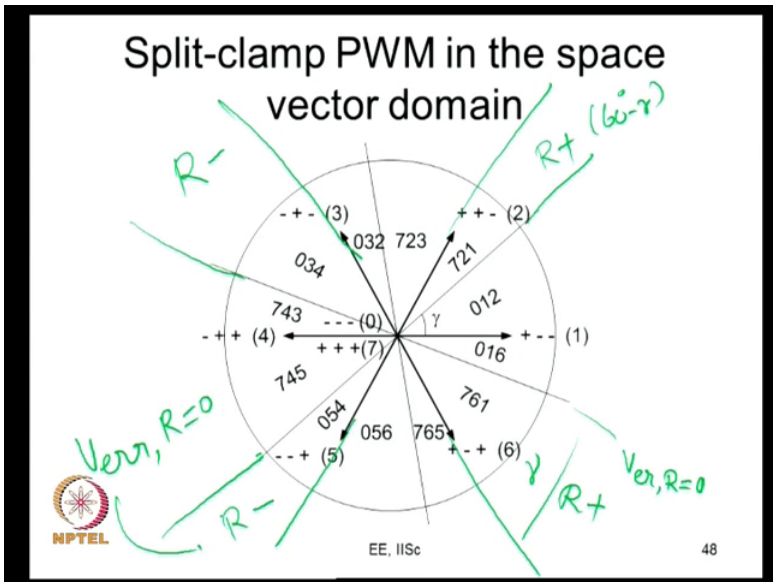

Again this is the split clamp PWM, which when represented in the space vector domain. You can see that R phase is clamped here and again R phase is clamped here. So, these two durations add up to 60 degree; this is gamma, this is 60 minus gamma; these two add to 60 degree. Again you have the same scenario here; here R phase is clamped to negative bus, here also the R phase is clamped to the negative bus. So, this is for a duration; 60 minus gamma and this is for a gamma; so, they add up to 60 degrees now.

So, this is for example, gamma this is 60 minus gamma, so they add up to 60 degree. So, in this case the error for R phase is 0. So, here also you will have V error for R phase is 0 whenever it is clamped it is 0, otherwise it is that plus average V error or minus average V error. So, this is how you can actually do it; you can for any PWM method.

So, that is any bus clamping PWM method, so the bus clamping PWM methods have to be either continual clamp or this split clamp PWM method. So, for any of these PWM methods it is possible for you to analyze the effect of dead time. So, once you have that square wave, you can do the harmonic analysis of square wave; the fifth, seventh etcetera would be the low frequency distortion; the fundamental component that you really have you can once again do that.

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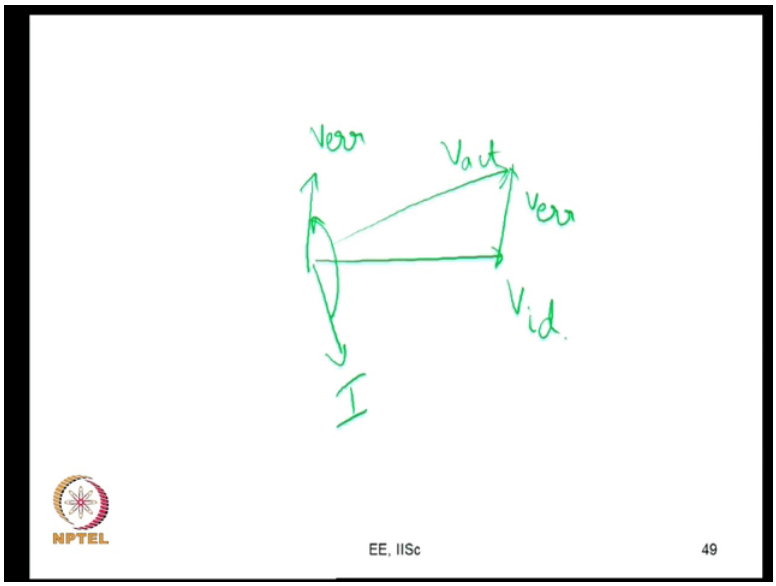

This is your V ideal and you have your current, now there will be an error voltage that is V error; this need not be at 180 degrees; this angle is not 180 degrees now; that will change from PWM method to PWM method and power factor also, this V error is added to that and now this will be your V actual.

So, what happens is also there is a drop; difference in these voltages V actual and V ideal. So, this can actually be seen as an I R drop, so in induction motor drives this can be seen as some additional stator resistance. And when the stator resistance is high, it causes instability. So, this though I have not discussed it here in this module; dead time also has the effect of increasing light load instability in induction motor drives; which is also something that you can find in certain papers. If you compensate for a dead time, you can handle light load instability; it will become good.

Thus, you know we have discussed this dead time, I hope you found this lecture useful and I hope that you would follow the remaining lectures with continued interest.

Thank you very much.