Pulsewidth Modulation for Power Electronic Converters

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Lecture - 34
Effect of dead–time on inverter output voltage for continuous PWM schemes

Welcome back to this lecture series on Pulsewidth modulation for power electronic converters.

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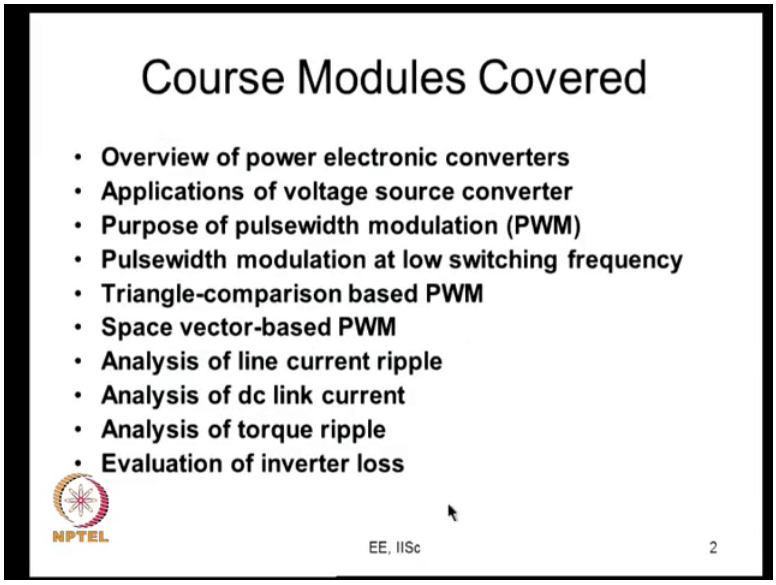

So, we have been going through several modules in this course, until the last lecture we have covered these up to ten modules. So, the first module was entirely on the power converter topologies then it is on the applications. So, these two are kind of applications of voltage source converters, these two are kind of general with things which you might as per you find in some part of power electronic courses and you know in the second part of course, you would certainly find and So if the some overlap with other power electronic courses. So, from the third part onwards we have actually been working on pulsewidth modulation proper. So, the third module is a very short module where we looked at some basics of pulsewidth modulation and then we looked at how to generate pulsewidth modulation for PWM waveforms in low switching frequencies, then we looked at them at the same thing as high switching frequencies.

So, how do you do it high switching frequencies the traditional method is to compare 3 phase sinusoidal modulating signals with triangular carrier? So, instead of sinusoidal you can use several other kinds of modulating signals also where you know you would have had some common mode voltage and you compare 3 phase modulating signals against a triangular carrier, then we also looked at this space vector based PWM. So, you know historically this was seen as something and later on you know I mean they realised that well there are lots of similarities between the two so and so far.

And at some point of time it was filled that they are entirely the same, meaning it is just an approach how you exactly implement whatever PWM waveform you can generate by comparing some set of 3 phase modulating signals against to triangular carrier, you can do the same thing using space vector base PWM. And whatever you can generate using space vector based PWM could be generated by comparing appropriate modulating signals against triangular carrier was the generally he will believe. But the lower recent advances show that this space vector based PWM is more general than the triangle comparison based PWM.

There are what are called as advanced bus clamping PWM methods which are space vector based PWM methods, this the waveforms produced by these methods you know they require these kind of space vector approach or rather you cannot compare 3 phase modulating signals against triangle carrier, to produce the same waveforms produced by those so called advanced bus clamping PWM methods. So, this is more general than that and we have also emphasized on the continuous and discontinuous PWM methods, which are common to both the approaches and the advanced bus clamping PWM which is which comes under this space vector based PWM all these have been emphasized reasonably well in this course up to this point of time, then we actually looked at the analysis of line current ripple.

So, this is particularly considering higher switching frequencies,- we did it in the space vector domain we considered the error voltage vector and tried to integrate that error voltage vector to get a measure of the flux ripple or which is equivalent to current ripple and thereby how you could go about the evaluating RMS current ripple and how you can compare PWM methods based on this RMS I mean current ripple so and so far.

Then we went to the analysis of DC link current. So, a motor is operating you know like I mean inverter is operating it is feeding nice sinusoidal voltages, I mean sinusoidal voltages with harmonics to the load, but the harmonic the load currents are you know almost nearly sinusoidal, but then how are the DC link current that is the question that we looked at. So, the DC link current has a different kind of harmony spectrum it has a DC component which essentially comes from let us say the rectifier or whatever and it has lot of ripple most of the ripple flows through that DC capacitor. And so this also gives us an idea of how to calculate the capacitor current through I mean the RMS current through capacitor, which you need for a sizing the capacitor and also for calculating the losses in the capacitor now.

Then we also did this analysis of torque ripple. So, like we considered both the low frequency PWM and the high frequency PWM in one lecture we focused on the low frequency PWM, looked at the corresponding flux harmonics current harmonics and so on and then how they I mean they would produce 6th harmonic torque and 12th harmonic torque and so on in another lecture in the same module we looked at the high frequency PWM we tried to analyse that. There once again we looked at the error between the applied voltage vector and the reference voltage vector it is just very similar to what we did in the case of line current ripple now. So, those 3 methods were actually an analysis.

So, they are there we wanted to analyse the line current ripple, the DC link current and the torque ripple, then subsequently we have started looking at so I mean in some sense I would say when you are generating PWM you are focuses on the fundamental and in some sense in these modules you are focuses on the harmonics, I mean the non sinusoidal components which are there in the inverter output and now we are moving onto certain non idealties, up to this part we actually considered the inverter to be ideal there is not much of not non idealties considered.

Here we looked at started looking at the certain non idealities. Firstly, with the non idealities in the devices so there is forward loss I mean the drop, therefore the conduction loss and there are switching losses. So, we spent about 3 lectures on how you would calculate these losses and the first one on calculation of conduction loss and the second one on calculation of switching loss and we did the third one where we tried to get a feel for certain PWM methods, which can be designed to reduce and which are designed to

reduce the switching loss in the inverter, on the power conversion loss in the inverter. So, that was the last module so we have covered all this.

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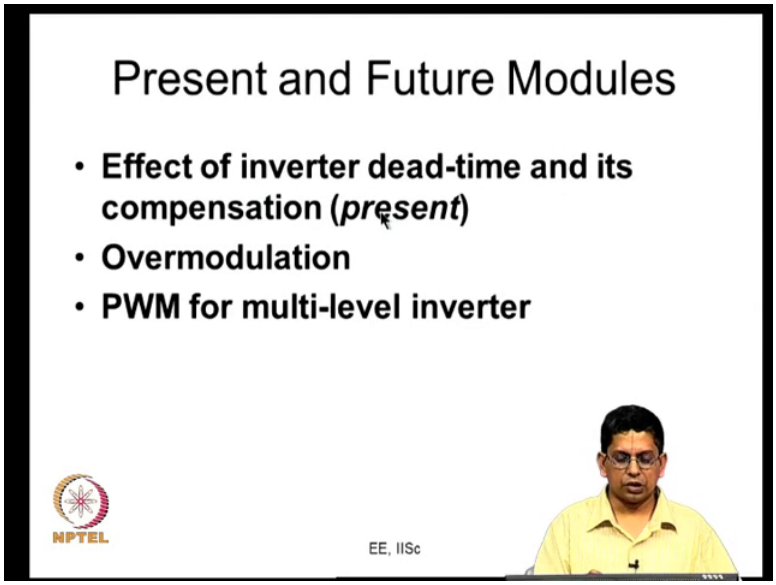

Now, we are onto this module today, this lecture and the following lecture we will be focusing on the so called the dead time in an inverter and what is it is effect and how you could possibly compensate for that is where our burden of discussion will be. So, this is then subsequently we will have another short module on over modulation, probably for two lectures and we will finally have this PWM for multi level inverter. So, whatever we tried to do like this centre angle PWM and space vector PWM etc for two level inverter, you would try to quickly see how you could do those for a 3 level neutral point clamped inverter so that would be that last one now.

So, let get onto our present module which is actually the effect of inverter dead time and it is compensation all right so here we get going.

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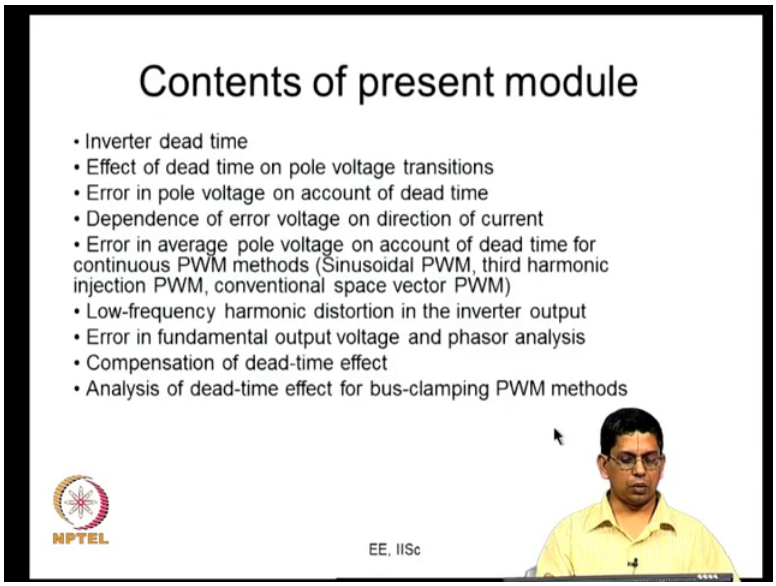

So, what we have is we have the inverter dead time. So, we have the inverter dead time this is one of this that we will be looking at today. So, the first thing if you want to know what is the effect of dead time? You need to start with what is dead time or why is that necessary. So, that is one of the first thing that we would look at today, what is this inverter dead time or why do you need this now then when you have this so called dead time. What happens is there is some change it makes to the pole voltage transitions, what do you mean by pole voltage pole stands for the pole of a single pole double throw switch that is every leg is a single pole double throw switch the midpoint is a pole.

So, the voltage at the pole is what is pole voltage and in this course we when we say pole voltage we normally mean the voltage at the midpoint of the leg measured with respect to the midpoint of the DC bus, that is what we mean by pole voltage here and this pole voltage has transitions from like you know pole voltage can be either minus Vdc by 2 or plus Vdc by 2 so there are some transitions. So, these transitions actually get effected by this inverter dead time, so they you know they occur there is some change there is some delay sometimes in certain pole voltage transitions so we need to find that out. So, we are going to discuss what is dead time and then once you have this dead time you have this dead time incorporated and how does it affect the pole voltage transitions.

So, the pole voltage transitions are not going to be where they were originally, when you did not consider dead time or you know you they are going to be little different. So, there

is a difference between the ideal pole voltage and the actual pole voltage because of this dead time. So, this is what I call as an error in the pole voltage on account of dead time. So, we would look at this also. So, we would see how much is the error between what it is the kind of nature of error between the ideal pole voltage and the actual pole voltage now.

Then we will also see that this error in the pole voltage you know that error voltage it depends on the direction of current, this is something that we will see the error voltage will be positive for one direction of current and it may be negative for another direction of current. So, once we have done these things what we will do is I mean by default we will consider sinusoidal PWM sine triangle PWM, but we would today you know, but after that we would like at sine triangle, third harmonic injection, convectional space vector, PWM etc all these continuous PWM methods, you will essentially be showing that the dead time effect can be analysed in the similar fashion for all these continuous PWM methods now.

So, you know once we are in a situation to do that, you know because of the dead time what happens there is certain inverter output, that inverter output is different from the ideal inverter output in what sense actually it would have introduced certain low frequency harmonic distortion in the inverter output, this is unexpected otherwise in an inverter why you have an inverter let us say it is switching at 5 kilo hertz frequency the fundamental frequency is 50 hertz. So, you needs output what frequency components will expect, obviously you will expect 50 hertz and you will expect some components are on 5 kilo hertz like 5050 hertz or 4950 hertz, 5150 hertz and you know 4850 hertz, similarly you will expect components are on 10 kilo hertz. So, you will you will get high frequency components on what you will expect, but this dead time brings in certain amount of low frequency components in the inverter output, this is one reason why it is not desired there is going to be some impact on the quality of waveform.

Then we are also going to look at what could actually be a more important aspect of the dead time affects, the fundamental output voltage it is not what it is supposed to be there is certain amount of change the fundamental voltage amplitude may be changed. I mean the fundamental output voltage the ideal value and the actual value could be different, they could be different in terms of their amplitudes or in terms of phase or both. So, that is something that we would look at and then we will also see how to compensate for this

effect, once we understand what this effect is it is also reasonably is you know easy for us to you know it should be easy for us to compensate for that. So, that we get an inverter output which is as close as possible to the ideal inverter output, as though there are no dead time period.

So, then finally, we would also look at the analysis of dead time effect for bus clamping PWM methods, this is something that we would be at mostly be dealing with in the second lecture within this module. So, in today's lecture we will focus on the initial portions which are basic here.

So, let us get started with the lecture say I have given you a very you know clear I mean fairly detailed description on the course on the present module. So, for this specific lecture we are going to be focusing on effect of dead time on the inverter output voltage for continuous PWM schemes. What I mean here is we have a voltage source inverter we are looking at the 3 phase voltage source inverter, the 3 phase voltage source inverter is being modulated using a certain continuous PWM schemes, we will start with sine triangle PWM by default we will assume that it is being modulated with sine triangle PWM and so we will see first start seeing what is dead times and what is it is effect on the voltages.

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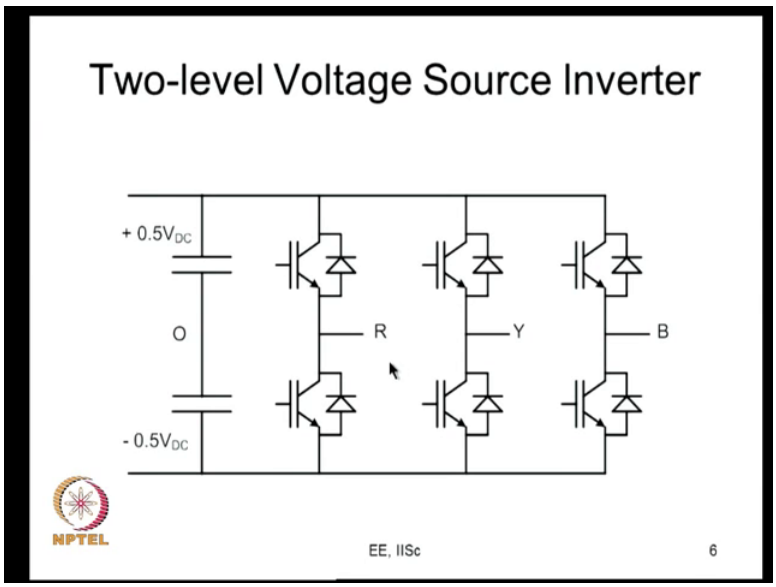

So, this is where we have a 3 phase inverter which we have seen several times and you connect the 3 phase loads, here this is the midpoint which is a load terminal and you

have this when I say pole voltage, what I mean is voltage at this point measured with respect to o. So, voltage at this point measure with respect to o this is what is called VRO, the R phase pole voltage similarly this is VYO the Y phase pole voltage this is VBO the B phase pole voltage. What we are going to see shortly is this VRO is going to change on account of dead time.

So, VRO actual will be different from VRO ideal when there is dead time introduced between the top and bottom devoices, but of course you need to introduce dead time between the top and bottom devices in a practical inverter as we will just shortly see.

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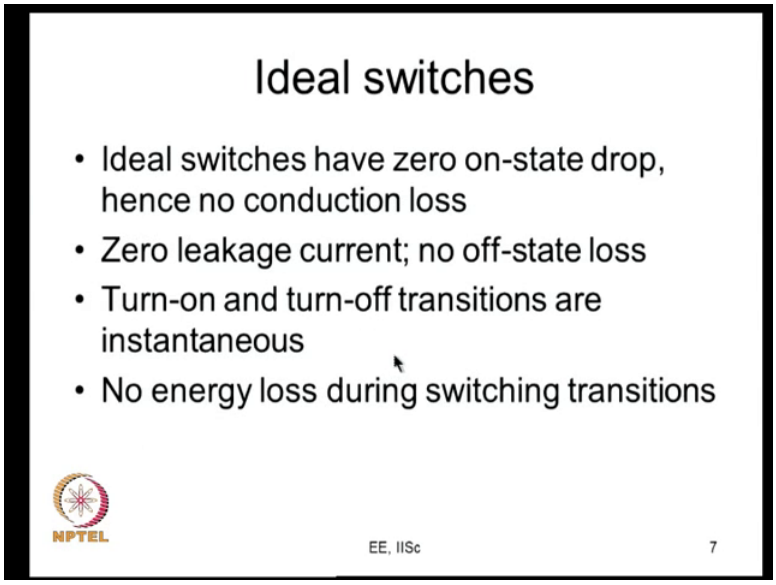

So, first we have to see what is this dead time? So, what is that dead time it is actually sometime interval you know between the switching of the top and the bottom devices. So, actually you have to get back to what switches RRY there. So, this is a ideal switches we have seen number of times we have discussed this idea you know earlier and particularly when we were discussing the losses when ideal switches suppose to have low 0, I mean no forward drop and no conduction loss. It has no leakage current and no off state loss and the turn on and turn off transitions are instantaneous and no energy loss during switching transitions, so this is what it is ideally.

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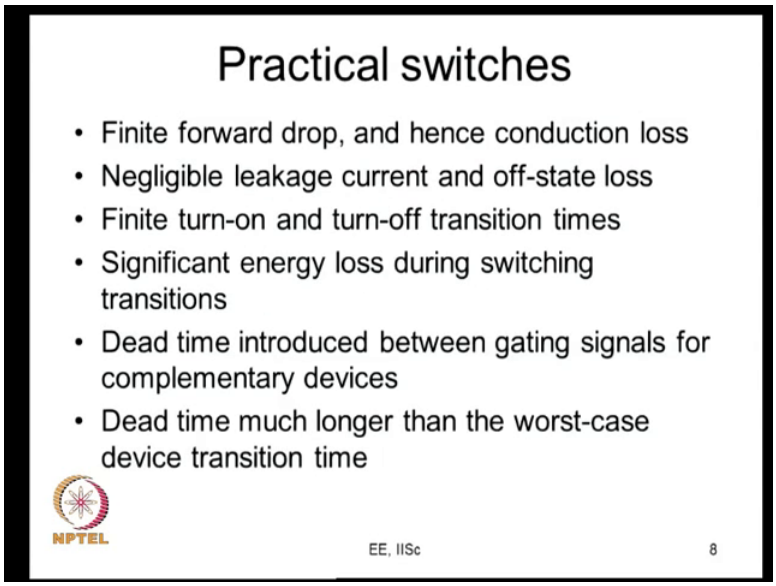

But in a practical case you know you say that it is a finite forward drop and hence there is conduction loss. So, we discussed it on this conduction loss on 1 of the previous lectures.

This is negligible leakage current and there is no off state loss. So, we did not discuss off state loss at all because you know in most power electronic devices the leakage current is quite negligible,. it has finite turn on and turn off transition times. So, one consequence of this is that there is a significant amount of energy that is lost during switching transitions, we focused on this over the last couple of lectures, in one lecture we tried to see how to evaluate this loss in the other lectures. The focus was relatively on how you would design a PWM method which will reduce the loss or how you will compare the switching loss between 2 methods.

So, this is what we this is one consequence of the turn on and turn off transition times you know being finite, other consequence is that there is a dead time which needs to be introduced between the gating signals for the complementary device, then the device is turned on and turn off in an instantaneous fashion you can switch the complementary devices with gating signals which are exactly complementary to one another.

Now, if they take a certain amount of time to turn on and turn off, now what you want to do there is a particular device is on you want to turn on this second device. So, can you do that 2 simultaneously it is better not to, what you need to do is there is a device which

is on you first turn off the device and then you turn on the next device. So, you wait for a short interval between the 2 and that short interval is what you call as dead time. So, this is the dead time is introduced between the gating signals for the complementary devices which are actually the top and bottom devices in an inverter leg. Now how short is the short or how long is long, this has got to be much longer than the worst case device transition time.

So, device takes certain amount of time to switch on or switch off. So, and this transition time is depend on the operating condition they change, now what happens you have a situation you know certain condition where the device transition times are longer. So, you consider the worst case device transition time and you choose your dead time to be much longer than that. So, I can give you some example there are IGBT whose switching you know typical device transition times, could be like harder hundreds of nano seconds or so but the dead time would be something like 2 micro seconds. So, I have that is probably the rise time etc. But it may be a sub micro seconds still the entire device transition time, you take it like something like 2 micro seconds here.

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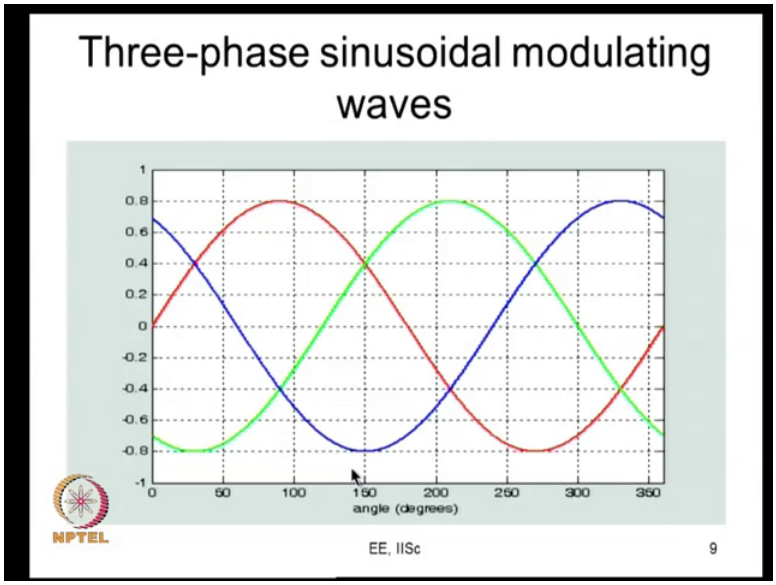

So, let us go further and see a little more clearly and what is dead time. So, which is these are 3 phase sinusoidal signals and we are looking at 3 phase sine triangle PWM now. So, r phase y phase and b phase what is not shown here is a high frequency triangular carrier and this high frequency triangular carrier you know is used to produce

PWM signals the like all the 3 are compare with a common triangular carrier and if the modulating signal is greater than the carrier, the top device of that like this on otherwise the bottom is device is on that is the logic that we use now.

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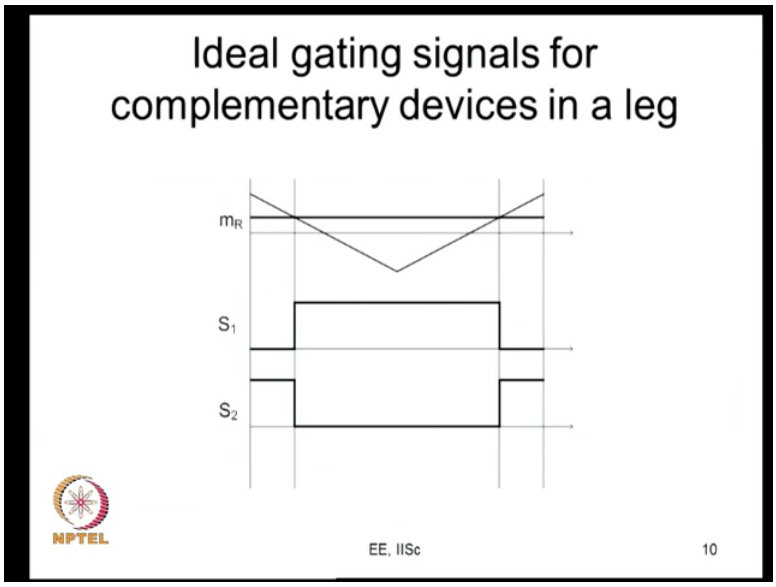

So, let us look at one particular carrier cycle, I mean it is not the entire line cycle. Now it is one particular carrier cycle we are looking at only one of them let us say mR this is in the positive half cycle of mR the R phase voltage. So, the mR is something like this we are considering one carrier cycle. So, what happens to this one carrier cycle you have this so you are comparing. So, once you compare these 2, whenever the modulating signal is greater than the carrier the gating signal is high. So, this is for the top device this is true for the top device, so you compare you produce this and here the carrier is greater than the modulating signal so this is low.

So, this is really the gating signal, but this is the gating signal for the top device of R phase and how it should it be for the bottom device ideally this should be exactly complementary. So, S1 I call as the gating signal for the top device of R phase S2 and you know by S2 I mean the gating signal applied to the bottom device in the R phase leg. So, this is ideally when the devices are you know having no, I mean when they are when the switching is instantaneous however. The devices are finite amount of turn on and turn off transitions as we know that.

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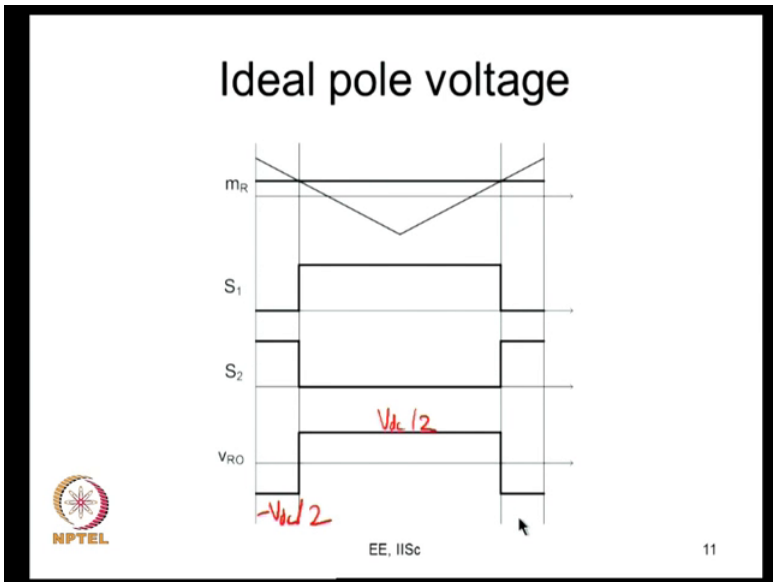

So, but before that we will see, if the devices are like instantaneously ideally what happens this is your switching signal and S2 is exactly complementary of that. So, your ideal pole voltage will be exactly like this. So, when S1 rises and S2 falls your VRO which is actually equal to minus Vdc by 2, where it is negative it is actually minus Vdc by 2, from minus Vdc by 2 it goes to plus Vdc by 2 you want me to write that here I can do that. This will be Vdc by 2 and this is minus Vdc by 2.

So, again what happens it there is a transition so it changes from plus Vdc by 2 to minus Vdc by 2 this is how the pole voltage is ideally, when there is no dead time in one carrier cycle let is now move on.

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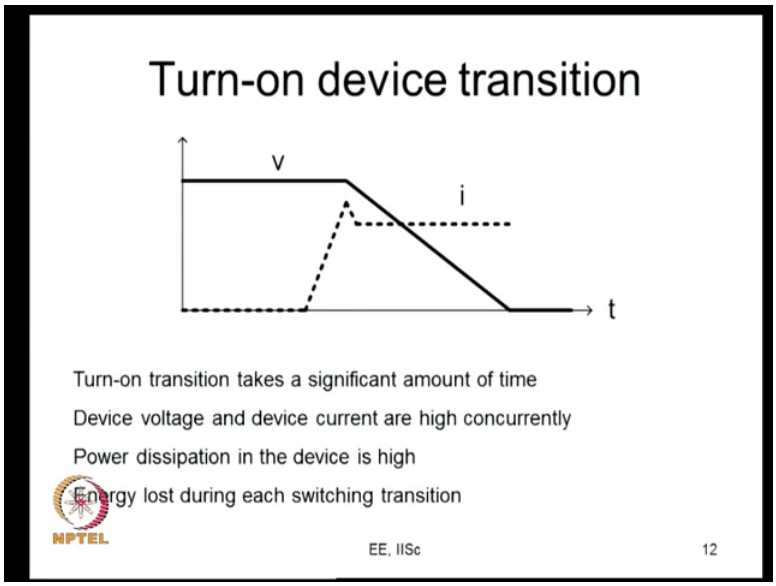

So, but this situation is no longer ideal because the devices take certain amount of time and this is some illustrative figure which shows you know that the device transition. So, it is more for an illustrative purpose. So, what we found is it is turning on the device voltage falls for certain interval of time, before the you know voltage starts falling even the current has reason fully and this is what we found was actually the reason for a high amount of energy loss. So, the current starts raising some instant before that and even before the current starts raising somewhere here the gate signal would have been turned high.

So, if you look at the entire switching transition time it could be somewhere here, where the gate signal went high to somewhere like this when the voltage has collapsed down to 0 and in between the current has raised to the full value now. So, if there significant amount of time that is taken for turn on transition, so device voltage and device current are high concurrently. So, in the last couple of lectures our focus was on that, was on this power deception and how much would be the energy lost when you are doing such switching transitions, but now what we are going to do we you know this is our now focus is on looking at the transition time and we are not worrying in this lecture about the losses, we are going to be worried about the dead time. So, if this is your interval for switching interval your dead time has got to be much longer than this.

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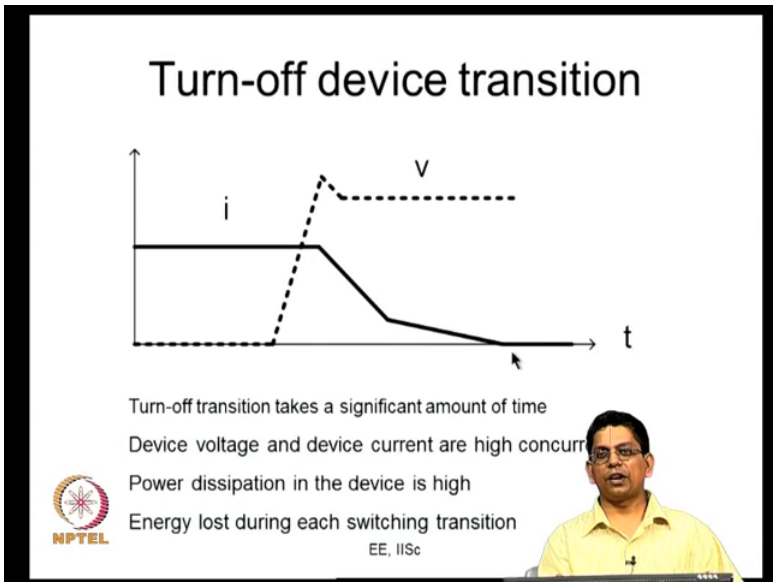

The same way you can look at the turn off transition a device current falls so it falls rapidly in this case it is shown to fall rapidly and then it kind of tapers of sometimes you call this tail current and even before the current starts falling, the voltages reason more or less to it is final value and the voltage actually started rising well ahead of that and then you know when the gating signal would have been turned off that was even well ahead of this. Now which is not shown in this curve because the VG, I mean the gate voltage applied and the actual gate meter voltages are not shown here now.

So, you will have a longer switching interval. So, this takes a finite amount of time of course, you have voltage and current or concurrently high and therefore the product is high, therefore power deception is high and there is certain amount of energy loss from this interval, these were things which we are concerned earlier. Now what we would want to says because there is a finite amount of time you need to wait, you know you once you have I mean you turn off a device. So, to turn off a device you know you turn off the gate signal, but the device is going to take certain amount of time you might have turned off here, but the device would turn off only here and it is its only well after this you can give the turn on signal for the next 1.

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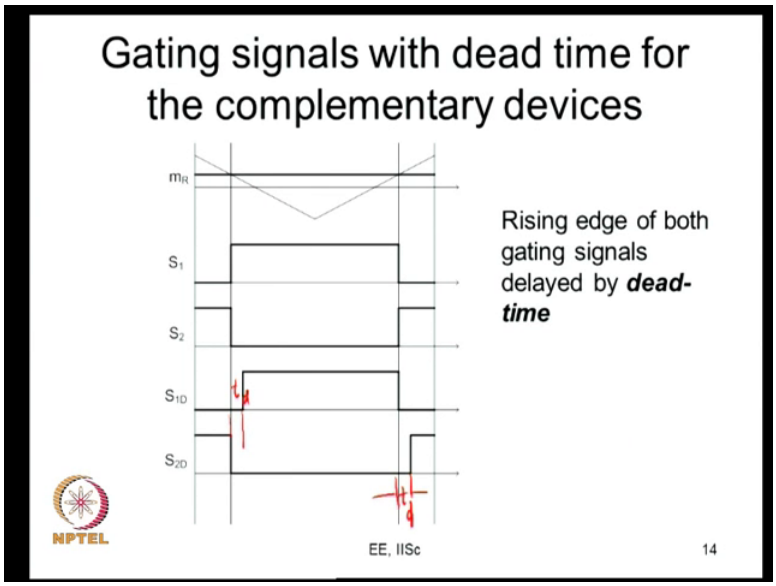

So, let us go ahead with this now so you have gating signals with dead time for the complementary devices. So, what are you going to do you cannot have say S1 and S2 switch in a complementary fashion not exactly? So, what you do you have to delay, what has to be delayed if a device is turning off the device should turn off first and you should allow sufficient interval to make sure that it has turned off and then you must turn on the next device, so that means here you expect S1 you know the top device should turn on and S2 the bottom device should turn off. So, the one that is turning off you give priority to that. So, you turn it off first then the one that is going to turn on you wait for a while and then apply this signal.

So, this gate rising edge of this S1 you delay it and this is the time you know, this much amount of delay time is what we call as a dead time, we let us say td. So, this is dead time you want shall I write it down here. So, I can call this time as td this is the amount of time. So, it is right it is delayed is that only for here and how about here, S1 is first turning off the top device is turning off and the bottom is supposed to turned on. So, we turn off on schedule, but the turn on you will delay it a little further. So, once again this is your td, so this is what is you td. So, there is certain so what is happening whenever you have falling edge, the falling edge is not changed significantly whereas, the rising edge is changed, the falling edge continuous to be wherever it is here an here the falling edge is same, but the rising edge is delayed.

So, the rising edges of this we gating pulses are delayed by certain interval of time called td and that td is the dead time. That is what is defined as dead time. So, why do you need this because they take finite amount of time, so it is better to give certain amount of time before you turn on a device? So, otherwise there could be a short there is a possibility of the DC bus getting shorted by the 2 devices conducting concurrently, ok.

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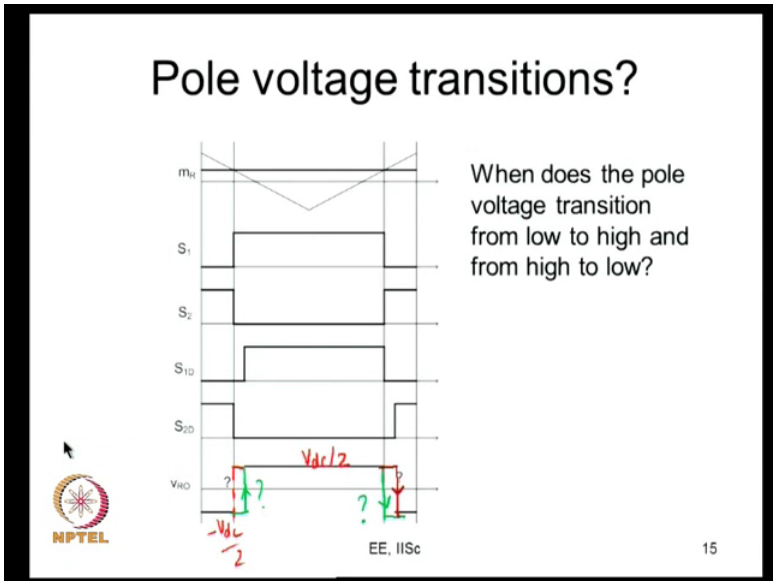

So, what is the problem now you have your S1 and S2 ideal signals, these are generated directly by comparison. Now after do that doing that what you do is you are introducing a dead time your shifting the rising edge by td you also shifted this by td now. So, the trouble is now you have to find out we have what is your pole voltage and that is a little difficult, now why because you see that you know there is a S2 this is going low the bottom signal is going low the top signal is going high a little later. So, I do not know VRO is initially minus Vdc by 2, that part is very clear it is minus Vdc by 2 and then it becomes plus Vdc by 2.

That is also clear the problem is when does it switch at this instant, if it switches at this instant it is like this or does it switch at another instant, for example does it continue to be negative for a while and switch here does it switch like this or here you do not know the same way here also does it switch like this does VRO make a transition like this or does it make a transition at this instant we do not know. So, how can you find that off

that actually depends upon, who conducts transistor or diode or which transistor which diode. So, let us see how that can be resolved.

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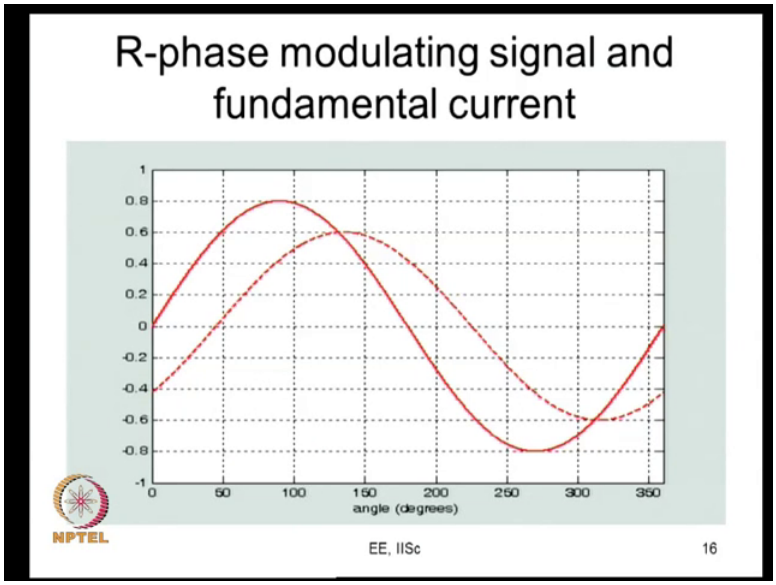

So, now what does this show, this shows the modulating signal of R phase and this shows the fundamental current with certain amount of show when the load is has it is only lagging power factor load this is some 45 degrees lagging here now. So, what you find is you find that the current is positive here the load current is positive here whereas, the load current is negative here once again the load current is negative here.

So, the devices the actual devices that conduct are different when the load current is positive and when the load current is negative, you remember always you in your leg one pair of device will conduct. I mean like the top transistor in the bottom diode will conduct during one half cycle and the bottom transistor and the top diode will Conduct during the other transistor, I mean during the other half cycle.

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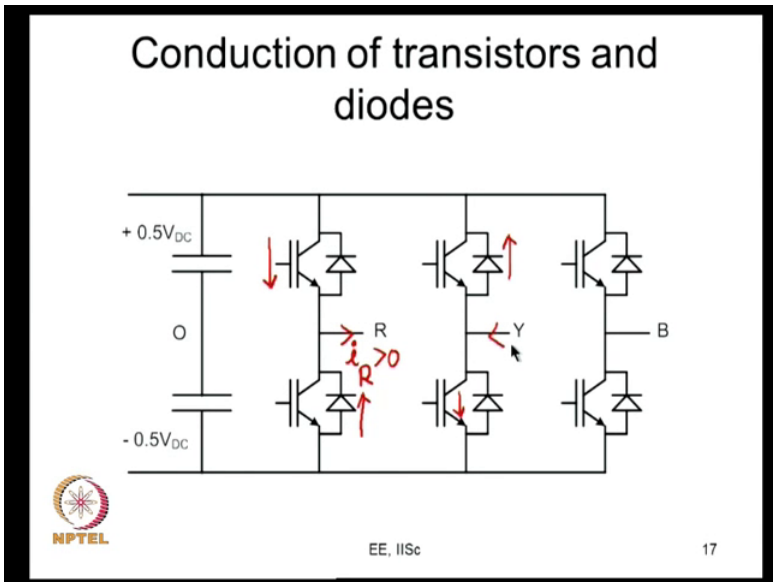

So, let come over here so let me say this is my iR this is the positive direction of iR. So, this is where an iR is greater than 0 this is the direction, if iR is in this direction then who will conduct, the top transistor will conduct if it is gating signal is high the bottom diode will conduct if the bottom gating signal is higher than the top gating signal. So, this is how the conduction will be this we have seen even earlier.

So, when iR is negative the current will be in the opposite direction. So, let us look at the next 1, you know let us say let is consider this case let us say the y phase current is flowing like this, we are in the negative half cycle of y phase. So, who is going to conduct now it is going to be this transistor or this diode, these are the ones that are really going to conduct now is it all right. So, now whether the top transistor and the bottom diode conduct or the bottom transistor and the top diode conduct depends on what depends on the current direction, we designate this direction is positive direction and this direction is negative direction. So, that actually tells us who is conducting right.

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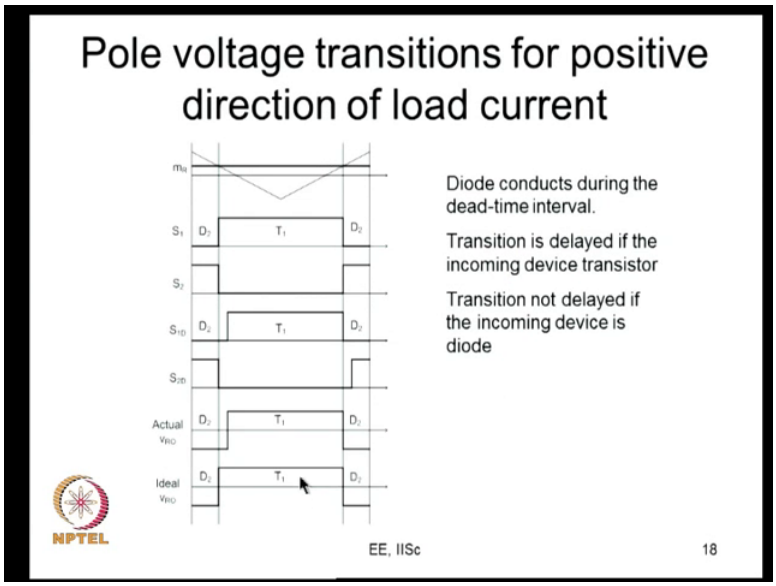

So, now if you look at here the same carrier cycle, the same modulating signal this is the ideal gating signal for the top device, this is the ideal gating signal for the bottom device. So, who is going to conduct it is the top transistor is going to conduct here, initially the bottom diode then the top transistor and once again the bottom diode D2.

So, the signals are delayed. So, D2 is conducting here T 1 is conducting here again D2 is conducting here. So, there is some uncertainty about what is going to happen here, what has happened the edges being delayed, here also the rising edge has been delayed. So, who will be conducting here who will be conducting here you can see that both the gating signals are low. So, neither the top transistor nor the bottom transistor can actually conduct it has to be only one of the diodes, which diode will conduct the same bottom diode will conduct; why that is because of the load current direction. So, the bottom diode was conducting will continued to conduct here.

So, during the dead time interval the bottom diode will conduct, so once again what happens here again the falling edge is wherever it was originally, but the rising edge has been delayed and there is this amount of time which is the dead time now. Who is going to conduct during the dead time duration, you see that once again you know both the signals S1 D and S2 D both are concurrently low and therefore neither of the transistors can conduct it, only the diode has to conduct one of the diodes and which diode it is D2.

So, when you shifted like this and for this positive direction of load current, in this carrier cycle the diode 2 was conducting that is continuing from the previous carrier cycle and diode D2 conducts all the way up to here and from this instant to this instant transistor T1 conducts and from this instant to that instant diode D2 conducts, that this comes later does not matter the diode starts conducting here is it all right. So, this is what happens now, so what are you going to say here there is a transition you S1 D and S2 D.

So, the diode continues to conduct it, where does the pole voltage go up. So, the incoming devices are transistor cannot start conducting, if simply here the bottom transistor gating has become low, but the top transistor gating has not yet become high therefore the top transistor cannot start conducting, the bottom diode will continue to conduct. So, that is what happens here hence because of that what happens your average pole voltage is like this it goes beyond that ideally, the average pole voltage would have switched here the transition would have been here now the transition is here now.

So, what are our assumptions here we are saying still that you know we are drawing this by a straight line is it all right, yes what we are saying is this so called voltage rise time the voltage. Rise time is still much less than the dead time is what we are trying to say and that is the reason why we are representing this by a rise and so although that this is an actual thing I mean we are actually considering a practical device, the voltage rise time of the device is much smaller than the dead time. And therefore we are still representing the actual voltage I mean pole voltage transitions is also is vertical lines you get that. So, this is a vertical line the only question was whether the vertical line would go up here or would go up here and now we have to say that it is going up here. So, whenever the transistor is an incoming device the actual pole voltage gets delayed.

Now, what happens next the incoming devices are diode, so the moment the top transistors gating signal has been made low the top transistors stop conducting, but who is should start conducting now it should be the bottom diode. So, the bottom diode starts conducting right at this instant. So, the bottom diode comes into conduction right here therefore, diode D2. So, if there is a transition from transistor to diode then there is no delay in the pole voltage, on the other hand when the transition is from diode to transistor there is a delay. When the incoming devices are transistor there is a delay, when the incoming devices are diode there is no delay; so this is what is actual pole voltage and while this should be the ideal pole voltage. So, you see that dead time is affecting what is

affecting the transitions in the pole voltages it is shifting it, what would have been here it has shifted here, in this case it is not affecting that.

So, there is actually an error between these 2 this is what we will see in a short while from now, this is when you consider the positive direction of load current what we are going to do now is to look at negative direction of load current.

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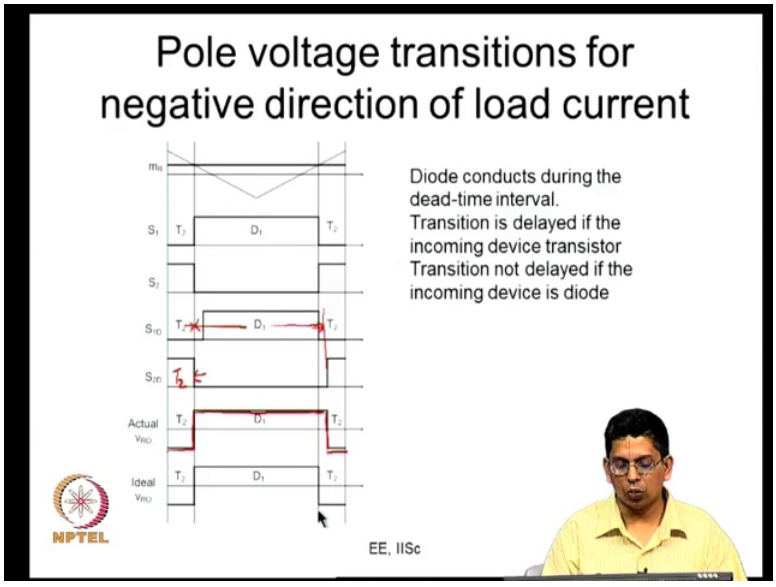

So, this is the negative direction of load current for that, I mean you are we are considering the same carrier and the modulating signal and these are the same idealised switching gating signals for the 2 devices all right. So, S1 D what is happening here the rising edge has been delayed by certain time and here this rising edge has been delayed by certain amount of time. So, this is what we have done all right. So, the rising edges have bend delayed these are the S1 D and S2 D now.

So, what happens to your actual pole voltage it no depends on who is conducting the current direction is no negative. So, whenever the gating signal is high for the top device, the top one should conduct, but it may be either the top transistor or the bottom transistor. I mean the top transistor or the top diode you take this interval the top gating signal is high, the bottom gating signal is low. So, the bottom transistor can certainly not conduct, so who will conduct it is a top diode that will conduct now. So, the top diode will conduct and prior to that it would have been the bottom transistor.

So, the transition is from the bottom transistor to the top diode and back to the bottom transistor. So, this is how they are going to conduct now. So, let us look at these intervals and see where this stops and where that begins now all right. So, this is the transistor which is one the bottom transistor, the bottom transistor will conduct when it conducts here up to what time it conducts only up to this interval. Why after that the bottom transistors signal is low so it cannot conduct. So, who conducts during this interval the diode already starts into conduction. So, the diode conduction begins right here and how long does the diodes continue to conduct.

The diode conducts certainly up to this instant; at this instant what happens at that instant the transistors get this signal is going low this signal is also low. So, there is no transistor that can conduct. So, the diode will have to continue to conduct up to this instant, so the diode conducts during that interval of time. So, what happens because the diode comes into conduction here itself, it takes over from the transistor to diode your pole voltage is switching like this, then it follows like this. Since the diode conducts all the way, I mean up to this interval here should it is the pole voltage is positive and it goes like this now. I hope this point is clear I hope this point is clear now.

So, once again what do you find that during the dead time intervals both the gating signals are low. So, who will conduct it is one of the diodes and which diode because of the current direction it is the top diode, here again you see that the switching interval both the gating signals are low. So, neither of the transistors can conduct it is the bottom diode that will conduct. I mean the top diode that will conduct on account of the current direction now right. So, you are now looking at a transition this is a transistor diode transition. So when the diode is the incoming device, so the diode is incoming device you know it comes an immediately and starts conducting whereas, the transistor is bit of a protocol man I mean is it is actually an active device unless the gating signal is high, it cannot conduct what you have done is you made sure that the gating signal to the top transistor is low. Here, but you are still not made the gating signal for the bottom transistor high, which you are making only here. So, up to this point the transistor waits it let is the diode conduct. And therefore it happens like this and therefore you find that you are actual voltage is little different from the ideal voltage, this transition now which is high to low transition is got delayed by TD.

In the earlier case it was the low to high transition that got delayed by TD, now in this case the high to low transition has got delayed by TD. So, there is certain amount of error between the actual pole voltage and the ideal pole voltage.

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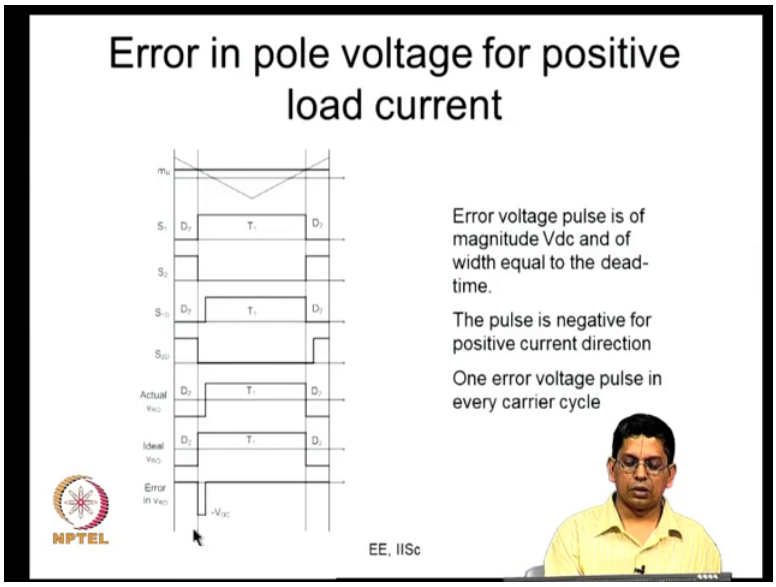

What is that when I have reproduced the same thing that we have had before for the positive load current, now the low to high transition is delayed here and therefore you have minus Vdc is the error between these 2, this is for the positive direction of load current and so this is a pulse the error voltage is a pulse of magnitude Vdc. Where Vdc is a DC bus voltage the sign is negatives, here what is the width of the pulse is equal to the delay time TD. So, you will get such a pulse in every carrier cycle, now if you are looking at the negative load current.

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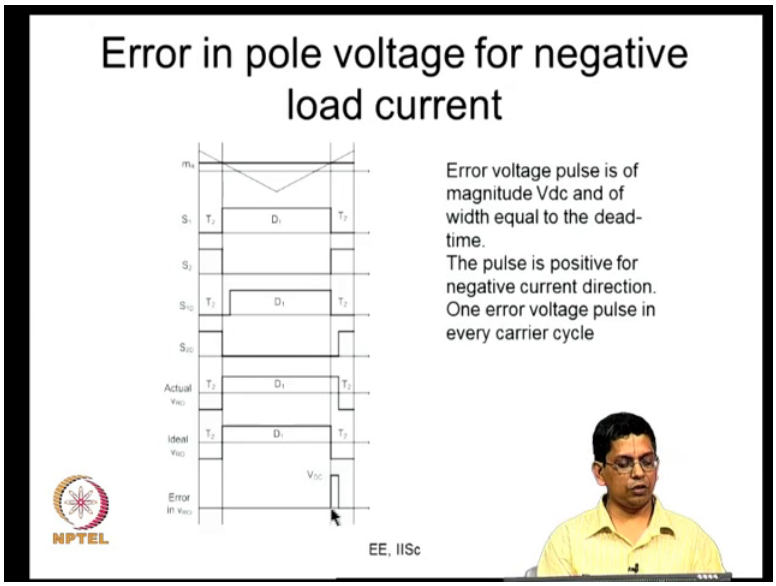

What you will have for the negative load current there is actual pole voltage and there is a ideal pole voltage, the difference between the actual pole voltage and the ideal pole voltage is like this it is like that. So, here it is a positive pulse the same Vdc it is positive this is time durations td so this is what you have. So, there is error between the actual. So, what do we see dead time is necessary, what is that the switches take finite amount of time to turn off and turn on. So, when you are switching complementary devices you must first turn off the device and then you should turn on the device, which is the incoming device the outgoing device should be turned off and the incoming device should be gated high only after some finite interval of time which is called dead time T D and this T D has got to be significantly higher than the worse case device transition time.

So, that you have do it from the point of view of protection. So, once you do it that has an influence on the average pole voltage, what it does is it shifts certain transitions depending on the direction of the current, either the low to high transitions or the high to low transitions, it is just shifting that you know the instance at which the pole voltage shifts now and that leads to certain error now, for our convention positive direction of current has negative voltage pulses and negative direction of current you have positive voltage pulses now.

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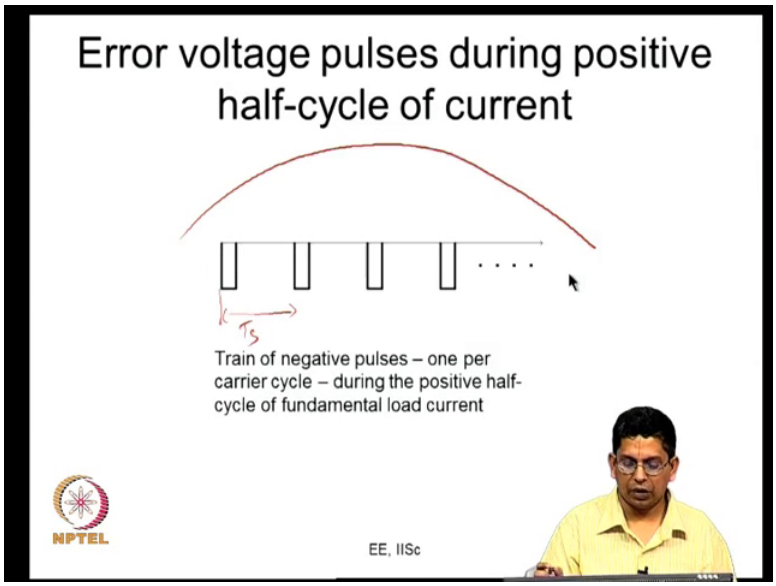

So, if you are looking at the negative half cycle or the positive half cycle of the current, this is a complete positive half cycle of the current I mean waveform let me just draw this here. So, the current is going through the positive half cycle, let us say it goes through the positive half cycle. So, the error voltages are negative here this is every carrier cycle this is like each carrier cycle, this distance is one carrier cycle this distance is one carrier cycle it is not necessary that the carrier cycle is starting here and it is ending here, but you get one carrier cycle in every, I mean one pulse in every carrier cycle. So, you see a train of negative pulses at the rate of one per carrier cycle, during the positive half cycle of the fundamental load current.

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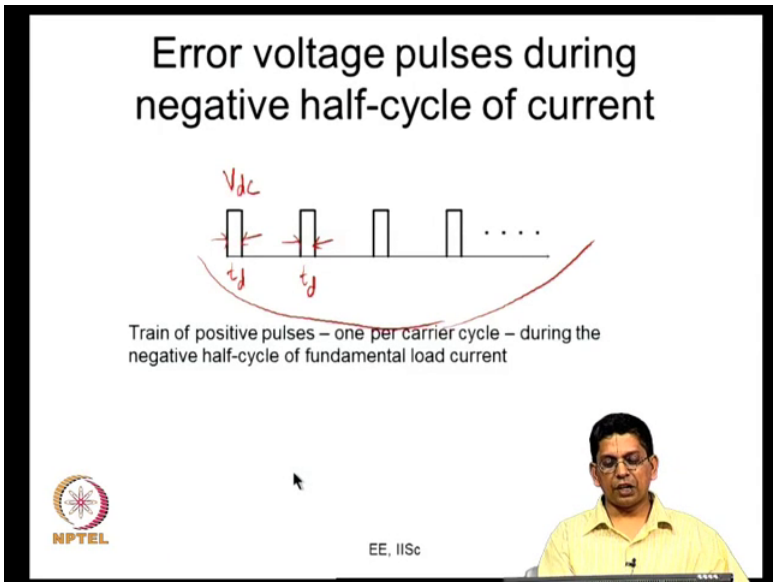

Next what happens let us say you are looking at the negative half cycle of the load current, you have the negative half cycle of the load current like this. So, during the negative half cycle you have these pulses. So, these pulses are what is the height of this pulse it is the same thing the height of the pulse is Vdc and the width of the pulse is T D. So, you have such kind of things, so you know what we wanted to do is when we are using dead time we cannot, but use dead time and once you are using dead time you have to find out how the actual pole voltage is.

So, what we are trying to do is we know what is the ideal pole voltage and we know; what is the error between the actual pole voltage and the ideal pole voltage. So, it is easy to come up with that so this is what we are coming up with so we will combine our understanding that we have during the positive half cycle and the negative half cycle of the current.

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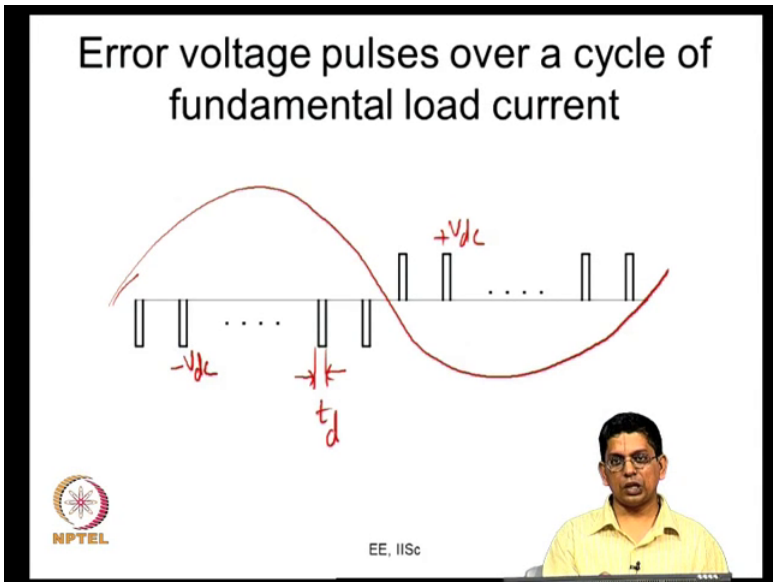

So, now what you have is let us say you have current which is like this. So, in the positive half cycle of the current you have these negative pulses and in the negative half cycle you have positive pulses, once again you know at this is minus Vdc this is plus Vdc and what are the width, it is width is delay time td. So, this is really the error between the ideal pole voltage and the actual pole voltage, when you do your sine triangle comparison and what you get that whatever the waveform gives is actually the ideal pole voltage, after that the dead time circuit there is something called dead time circuit which is part of the modulator or may be just outside the modulator depending on it is implementation.

The dead time circuit does this job of delaying the rising gate signals and that is what uses this now. So, the actual pole voltage is a little different from the ideal pole voltage, now what we are trying to do is rather than predict the actual pole voltage we are trying to predict the ideal pole voltage, which is easy to predict because it is directly from comparison and we are also predicting the error between the actual pole voltage and the ideal pole voltage. So, that is our combined output now. What is our actual inverter output? The inverter output now is the ideal output plus this error added to that that is what we can see.

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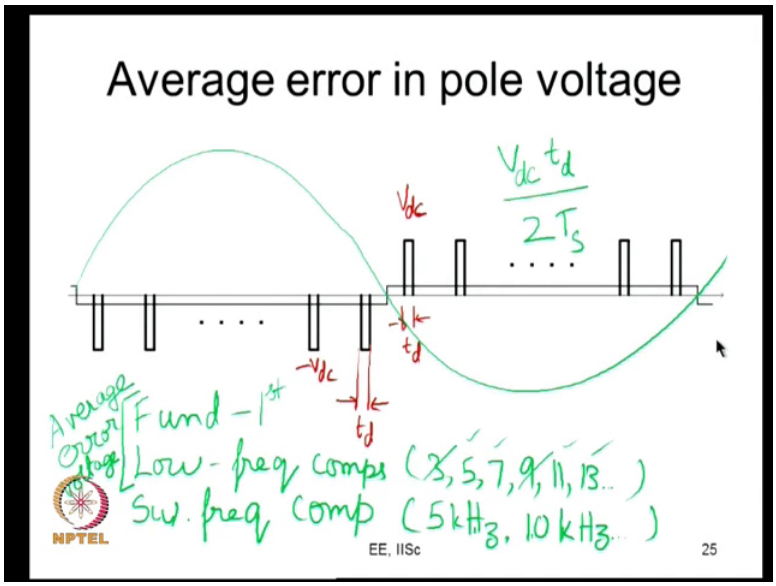

So, now these pulses are repeating everywhere this is once in every carrier cycle. So, it can be averaged over a carrier cycle now incidentally it has got the same height and the same width in every carrier cycle and therefore it has the same average value in all the carrier cycles. So, you can actually approximate this by a square wave. So now let us say what is this square wave business this is the error voltage and now these are this is our magnitude Vdc and this is of width td the same way this is minus Vdc and this width is td. So, this is error voltage pulses so what kind of waveform this is this is a periodic waveform yes this is a periodic waveform. So, what is it is periodicity it is periodicity is actually the fundamental frequency, so In fact you really have your line current flowing like this your current is like this ok.

So, it is like that so it is periodic and what are the frequency components it will have, it certainly has the fundamental component. So, that is let is call it 50 hertz let us say the fundamental frequency is 50 hertz. So, this error pulse waveform will have what all components will have it will have 50 hertz, it will have 150 hertz, it will have 350 hertz, 250 350 450 550 everything it will have all the odd harmonics it will have because you know it is roughly half your symmetric. So, you can say the even harmonics might not be there and all the odd harmonics you are you going to expect them there now.

So, you are going to have very high frequencies also because these pulses are repeating at this switching frequency. So, you are going to have fundamental component, you are

going to have low frequency component and you are also going to have switching frequency component these components are there. So, there are various low frequency components, so these are like 3rd 5th 7th etc 9 11 13 etc and here this is are all switching frequency.

So, let us say switching frequency is 5 kilo hertz, this may be like 5 kilo hertz 10 kilo hertz these are around 5 kilo hertz not exactly 10 kilo hertz so and so far. So, you are not particularly worried about the switching frequency component, they are already there is some amount of things what just troublesome is these 2, the error voltage has a fundamental component. So, what does it mean? So, you have your ideal fundamental voltage this error is going to get added up phasorily to that. So, your fundamental voltage actually could be a little different from what you expect. So, there is a trouble for you so you need to find out whether it is different? How it is different is it significant and can I correct it that is not the only trouble there is also the low frequency components.

So, in a inverter if you are switching an inverter, let us say having a DC bus voltage of 600 volts at a modulation index of something like 0.8 or 0.9 at a switching frequency like 5 kilo hertz, what kind of output you will expect you output which contains the fundamental component like 40 hertz or 50 hertz, whatever I said let us say 0.9 modulation index at 45 hertz. So, 45 hertz you will have the output, but you know the frequencies the harmonics will be around 5 kilo hertz 10 kilo hertz, which is called the first side band and second side band and so on, you will not have this 3rd harmonic and you know 4th or 7th harmonic or whatever.

So, now there is a problem why because the low frequency components are all introduced by this fellow. So, there is some issue so you have to actually avoid that. So, this is low frequency components which are there in the pole voltages, this will actually get neglected as you we can also see a little later as we already know. So, this 3rd will not appear in the line voltage 9th will not appear in the line voltage, but 5 7 11 13 etc will appear and the fundamental component is also going to appear. Now you want to combine all these. So, what you can do is you can go in for average, you go for average error voltage this average error voltage is something which will contain the fundamental and the low frequency components of the waveform, but it will not contain the switching frequency components here.

So, it would contain only these things let me clear this up, so it contains this. So, you go for this low frequency what is that error this is the error, I mean what is the average voltage? how much is this average voltage? So, if this is Vdc the average voltage is Vdc multiplied by the width td and this occurs once in carrier cycle which is 2 times Ts and this is what I will probably call that as average error voltage. The instantaneous error voltage is Vdc and happens for time T d; so the in once in every 2 Ts and so this is what I would call as the average error voltage. Now this average error voltage now I can represent this by a square wave, that square wave comes I mean it contains all the fundamental and the low frequency components which are present in that now so let is look at this analysis. So, what are we going to do here?

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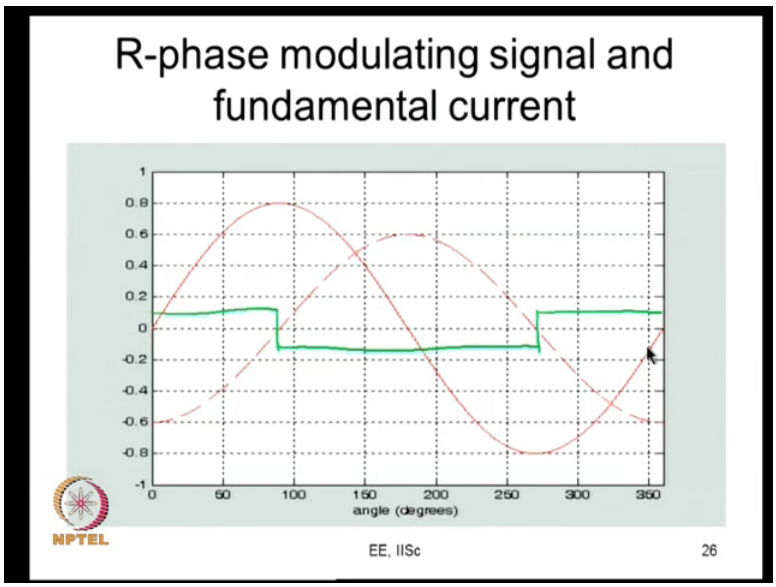

So, this is some amount of current that is flowing here all right. So, there is going to be some amount of error voltage how is that error this error is going to be negative, there is some negative error voltage and the load current is positive and vice versa. So, this is the kind of error voltage that will be seen in the output, this fellow the modulating signal is supposed to give you the ideal one and on top of it there is going to be an error voltage like this.

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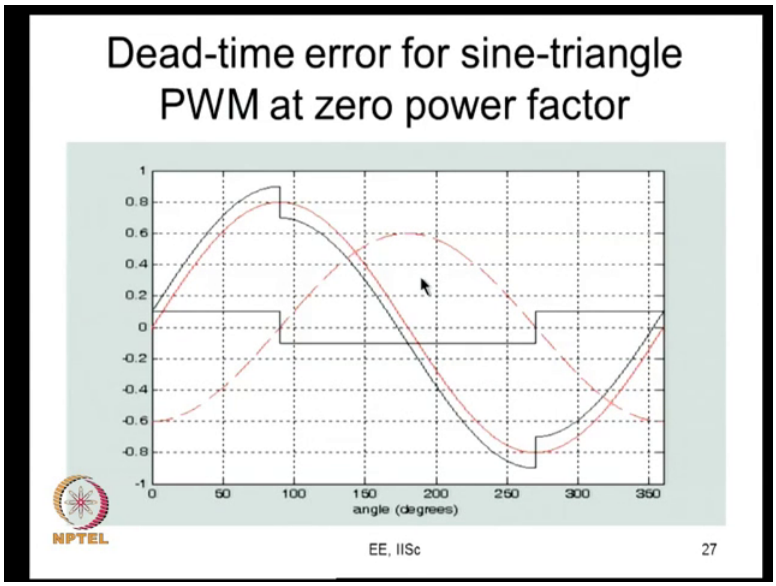

So, which is what I have tried to show you in the next figure? So, this is a error voltage it may not be. So, high I have shown it as some 0.1 per unit where your fundamental voltage is like 0.8 per unit it will not be so high, it depends on you know how high is your dead time and how high is your switching frequency. The switching frequency is very high this might become significant, but still may not be I will show that slightly exaggerated at point on p or may be lower than that.

So, what happens now you see that there is an error voltage so your average pole voltage. What do you mean by average pole voltage? you know what is pole voltage that is the potential at the midpoint of the leg measured with respect to the DC bus midpoint and that is the pole voltage that is r phase pole voltage, that r phase pole voltage can be averaged over every half carrier cycle and every sub cycle that you will call as the average pole voltage.

Now, this average pole voltage what happens there is an error on top of it. So, rather than being this sinusoid, there is some something added here again this negative number is added here. So, it comes like this. So, this is your average pole voltage now. So, your VRO average is not as sinusoidal, as it is expected to be in the ideal situation it is sinusoid with some square, wave added to that the square wave is amplitude depends upon the dead time the DC bus voltage and the switching frequency and this square wave

is out of phase with the fundamental current this is what you can say, this is true not only for this power factor which is incidentally 0 power factor

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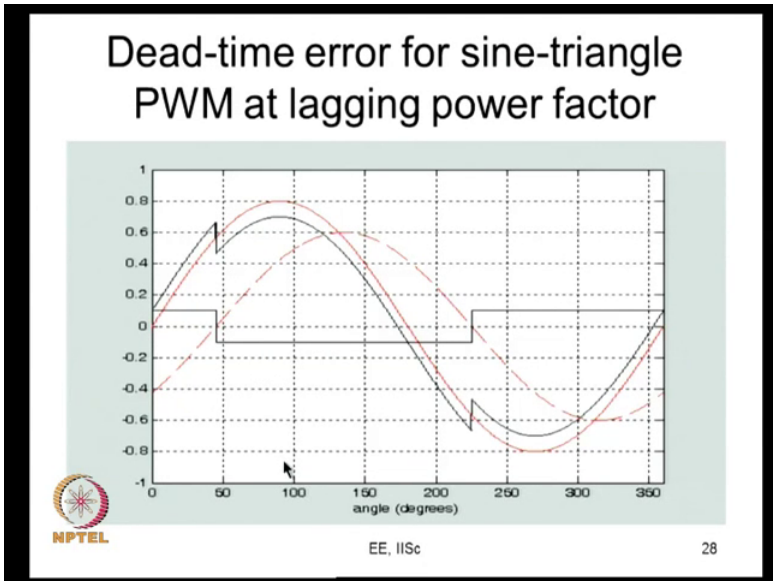

This is true for every other power factor; here we have shown something like 45 degrees lagging current same sinusoidal PWM. So, if this is the error voltage square wave same amplitude out of phase with the fundamental current. So, it also does not depend upon the amplitude of the fundamental current, the fundamental current instead of .63 it may be .4 or it may be 0.8 it does not really depend on that, it rather depends on the direction of this value, only depends on Vdc td and your Ts or your switching frequency. So, that is what it depends on now. If you operate the inverter at low switching frequency your T Sis high and therefore, this will be very negligible.

Once again if your td itself is very small this will be very low. So, it is it depends on the ratio of td upon Ts. So, that is what it really depends upon now so this is showing at 45 degree lagging power factor angle.

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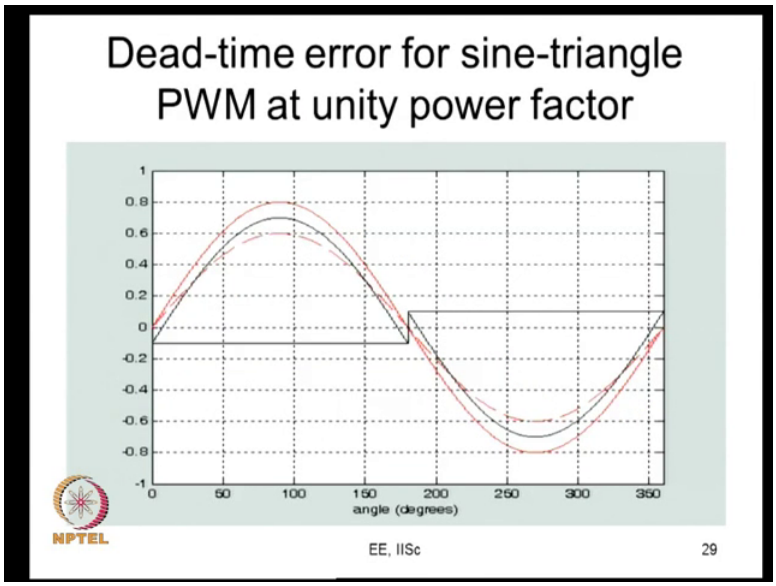

Now, I am look at I am looking at unity power factor, this is the fundamental voltage and this is the fundamental current. So, what I am trying to do is trying to look at the error voltage, the error voltage use the average error voltage is square wave like this and this is added up to the modulating signal this is the fundamental or the average pole voltage. The average pole voltage is this black one now it is like this it is shifted it is come back to this now so this analysis is true.

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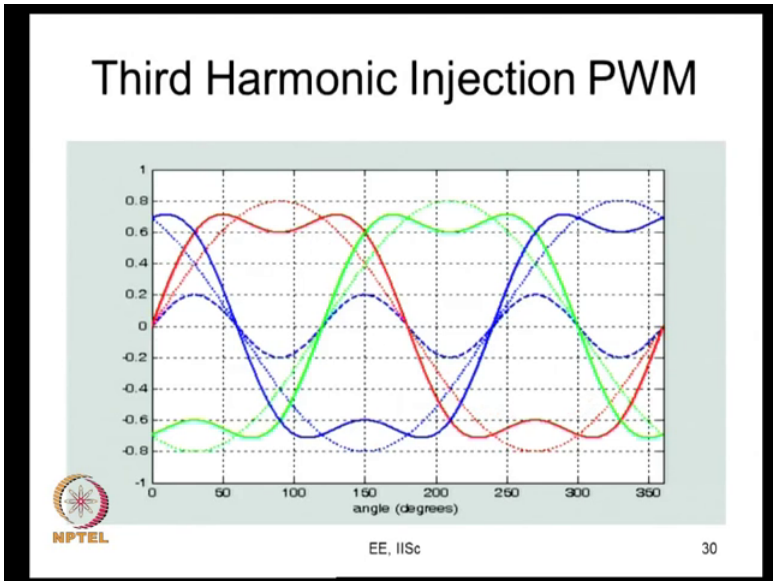

For all these power factor so if that is sine triangle PWM, now what are you going to look at we are going to look at third harmonic injection PWM . So, why are you have this 3 phase sinusoid and you have this 3rd harmonic triplen frequency component. I mean third harmonic added and incidentally it could be 1 by 6th here and so you get this modulating signal, this is your R phase this is your Y phase and this is your B phase modulating signal all right.

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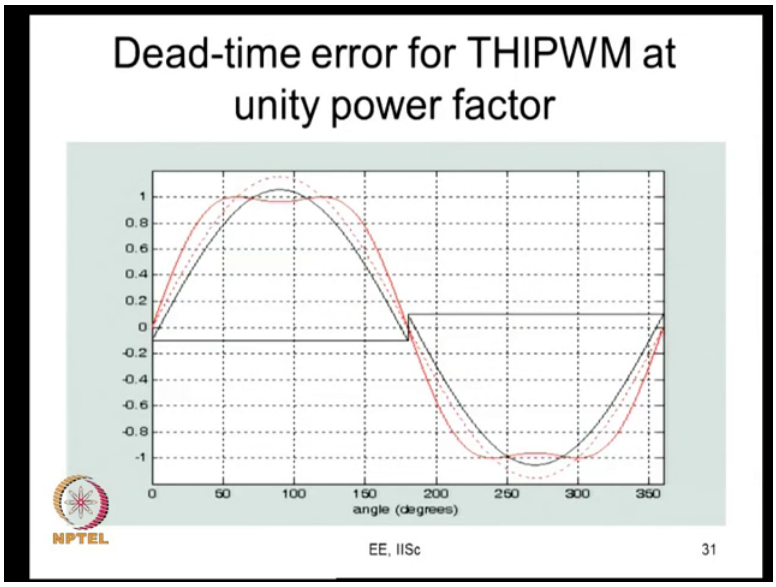

So, here what we do let us look at one of them let is look at the y phase I mean the r phase modulating signal, here again let us say we have unity power factor current. When you have unity power factor current once again, the dead time error is the same this is the average dead time error it is the same. So, when the current is positive there is a negative error and when the current is negative it has positive error. So, it does not actually depend up on the duty ratio.

So, for example if the duty ratio here is something you know it is like 0.8 if the duty ratio is 0.8 or 0.9 it does not seriously matter on that, but it matters if the duty ratio is 1, if the duty is one then the phase does not switch at all and there will be no error voltage again if the duty ratio is 0, there will be no error voltage at all because the phase wont switch at all, but for any duty ratio that is between 0 and 1 are not inclusive of 0 and 1. The error voltage does not depend upon anything it depends only on the direction of current. So,

the polarity depends on the direction of current and it is amplitude deepens upon Vdc td and Ts as I mentioned before so this is for third harmonic injection PWM.

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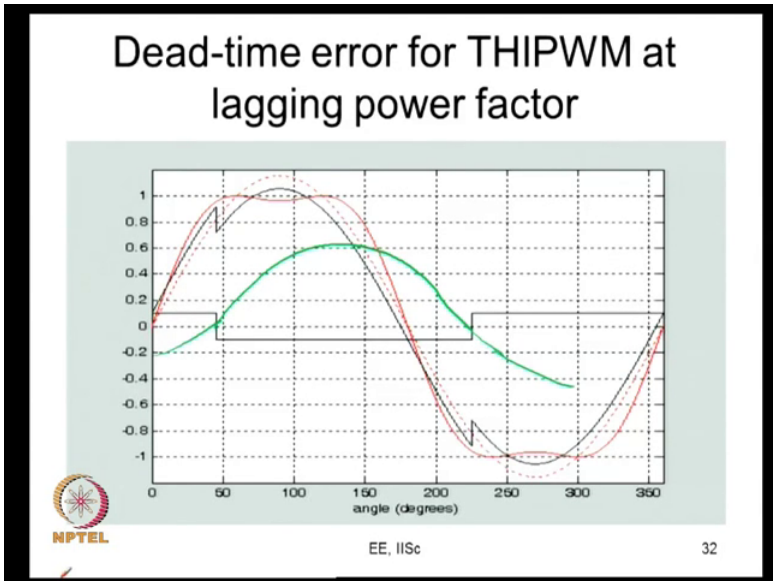

So, let is look at the next one this is also third harmonic injection PWM, but now we are looking at a 45 degree power factor angle. So, once again you know the same thing that is said there is current and this is going to be in phase with the current, there is some error in the current has been plotted here as though it is said unity power factor rather the current is not shown. So, the current should really be here let me draw the current. So, the current should have 0 crossing like this, is how the current is this is how the current is every regret this error. So, this is how the current is all right so this is how it is now.

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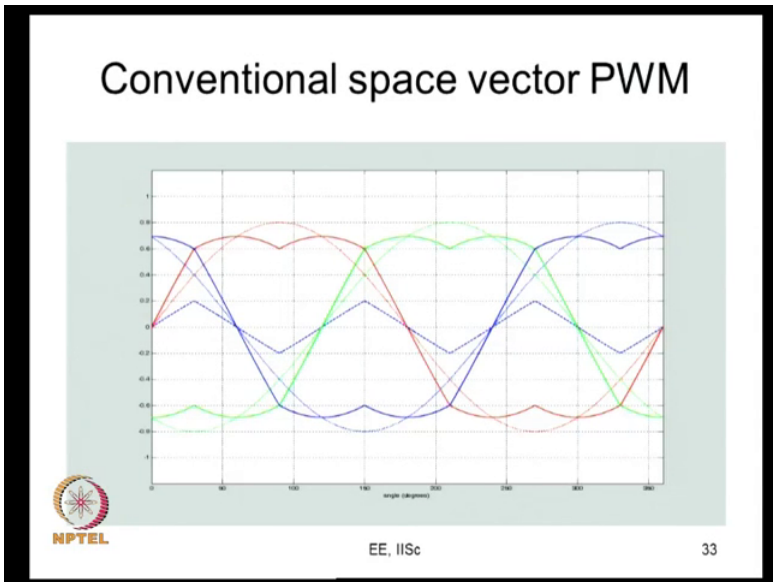

Then we are considering conventional space vector PWM, this is again a continuous PWM method where this is the r phase sinusoidal modulating signal and you are adding this common mode to all the 3 of them. So, you are r phase modulating signal actually become something like this and so this is compared with such 3 phase signals are compared with triangular carrier and this will give you equal division of null vector time. So, whatever time for it is this 0 vector is applied both these 0 states will be applied for equal durations of time, as I have mentioned an number of occasions before.

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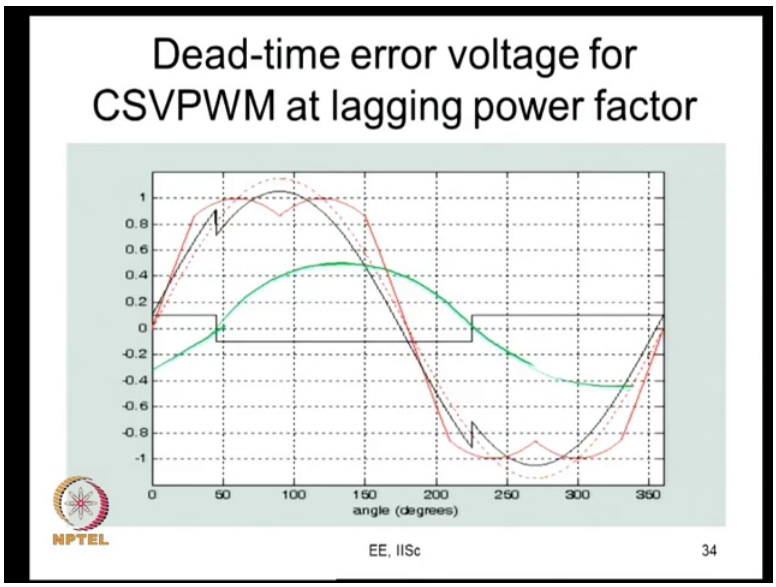

So, here if you take here so what is going to happen here, once again I have shown the sinusoidal modulating signal this is actually greater than 1 because of addition of the common mode it actually just touches 1. So, you can see that the DC bus utilization is here more we are looking at some modulation index of 1.15. So, this is the highest modulation index possible. So, in this what is not been shown here is actually the current waveform.

So, the current is really like this is how the current is this is the current. So, when the current is going through positive half cycle, the error voltage is negative the negative half cycle the error voltage is positive; this error voltage gets added up to the average you know pole voltage. So, you know you if this incidentally is what is shown here this is the sinusoidal component of the modulating signal plus this error voltage is shown here, all that the modulating signal contains the triplen frequency components will go away, when you subtract one pole voltage from the other they will go away, but this all of them will not go away.

So, this square wave what happens is you know this square wave also has 3rd harmonic 9th harmonic they will go away, but whatever is the fundamental component 5th harmonic component and 7th harmonic component etc they will not go away now. So, what is actually shown here is the sum of the modulating sinusoid plus the error voltage is what is added and shown there. So, it is not exactly sinusoidal that is what you know we are trying to see here now.

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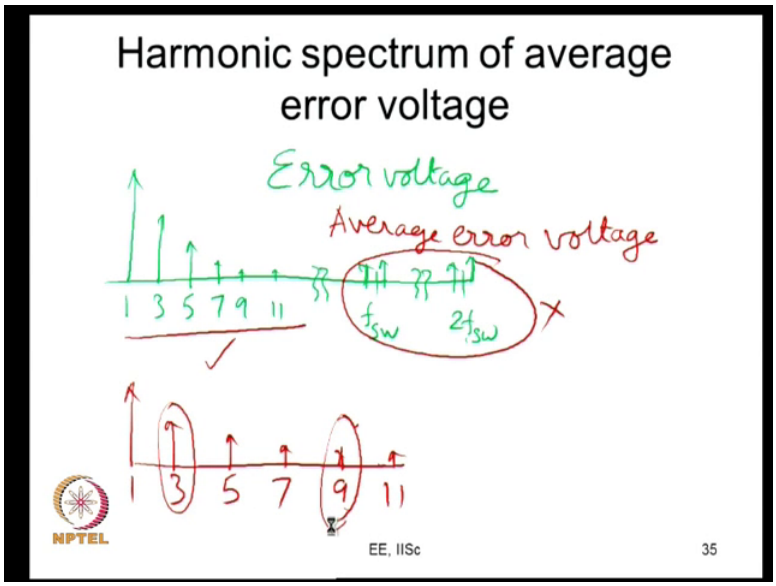

So, let is now look at the harmonic spectrum of the average error voltage little clearly. So, what I originally said was you have a signal that is your pluses. So, you have your fundamental here this is I am talking of the error voltage. So, the error voltage will have 3rd harmonic will have 5th harmonic will have everything like this, then it will also have around switching frequency. So, you will have some components like this will also have some components here this is the error voltage, the voltage harmonic spectrum of error voltage.

Now, I am going to look at the harmonic spectrum of the average voltage, now I am going to look at the average error voltage. So, the average error voltage retains all the low frequency components from the error voltage that misses out all these, this is all not there in the average error voltage, but these are all there. So, this is how the harmonic spectrum is let me just redraw that you may have some fundamental voltage, there is some 3rd harmonic some 5th harmonic some 7th harmonic 9th 11th and so on, this is how your harmonic spectrum will be this is in the error voltage in R phase.

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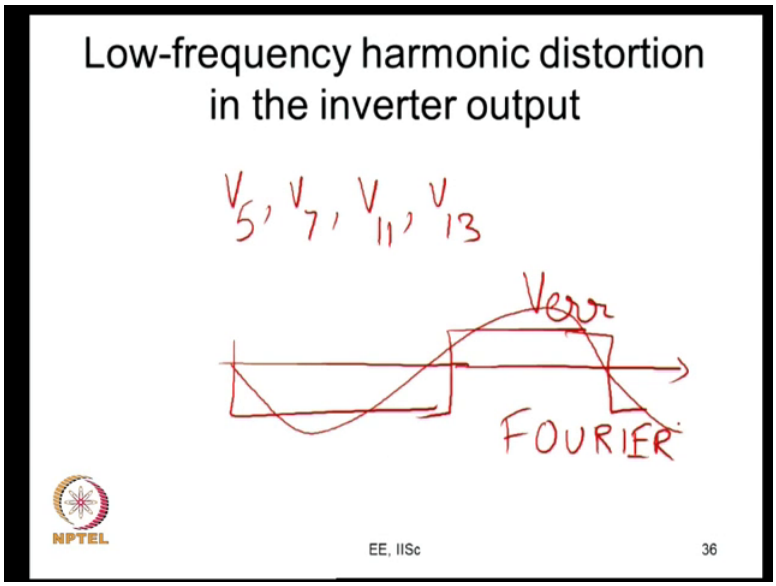

So, now what will happen all these error voltages, these will eventually get cancelled out this same amount of error voltage will be there in y phase also same amount of error voltage will be in b phase. So, when you subtract the pole voltages to obtain your line voltages these will go up. So, what you will get here is you will get your low frequency distortion. So, you will get your harmonics which will be like v5 v7 v9 v 11 v 13 etc. How can you reduce these values no problem, this is just a square wave right is just a square wave.

So, this is just your square wave you have to do the Fourier analysis of this square wave and that can give you all your low frequency components, the trouble with low frequency components is they are low frequency components they are going to you know affect your waveform quality.

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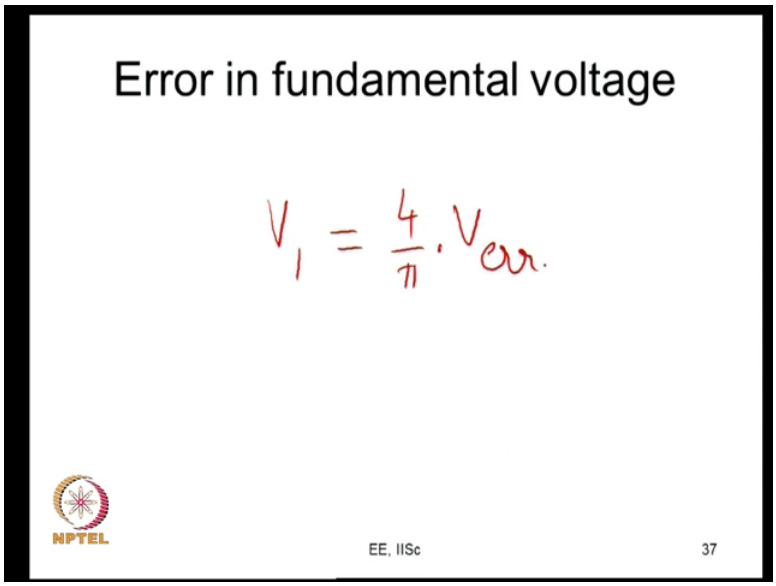

The next thing is about the fundamental voltage, this square wave also has a fundamental component this also has a fundamental component and that fundamental component is 4 by pi times whatever is the average error voltage that you have.

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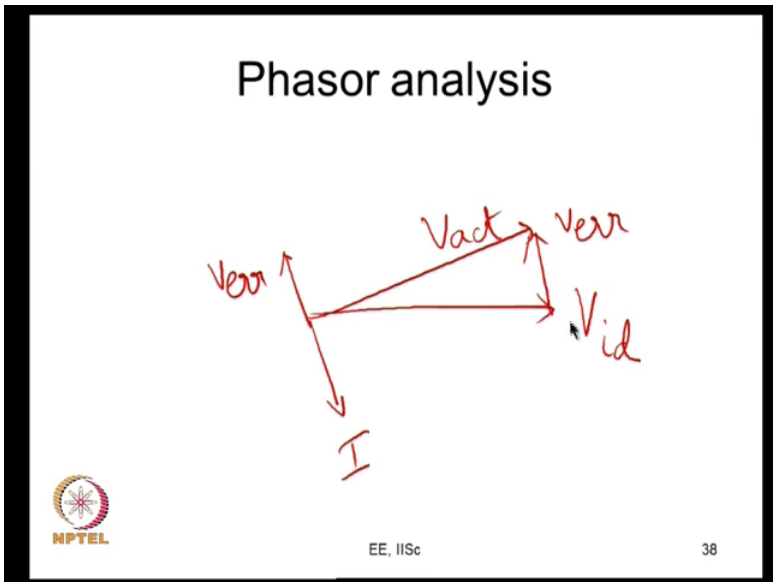

So, you can actually look at it as there is some ideal fundamental voltage, there is certain current now this is error voltage like this your actual voltage, is this error voltage added to that this is your actual voltage. So, it is affected your dead time excuse me the dead time changes your ideal voltage like this. So, this is how it is going to affect and you can

read more of this on how to compensate for this and from here and in this paper you find several lots of previous references this is essentially on how you compensate.

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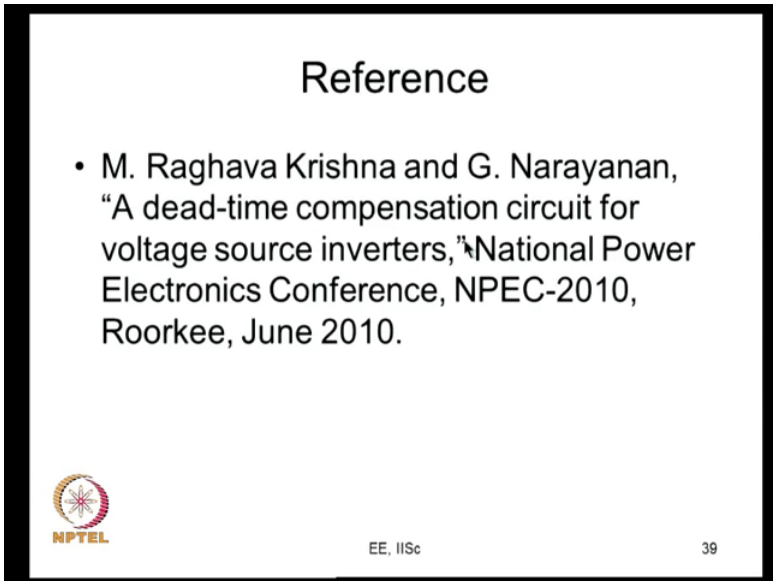

But you have lot of previous references also it is given and there are also other papers where you would can get this analysis of this. So, this is how about dead time and we primarily focused on continuous PWM methods.

In the next lecture we would look at the bus clamping PWM methods. And so till now we will do the similar kind of exercise on the bus clamping PWM methods. So, I hope that you know this one was interesting to you and I look forward to your continued interest in for the remaining lectures in this series.

Thank you very much.