Power Electronics and Distributed Generation
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Module - 3
Lecture - 26
Inverter Switching and Average Model

Welcome to class 26 on topics in power electronics and distributed generation. So, we have been looking at the currents, in current components in a single phase inverter and especially and the single phase inverter with a capacitor centre tap configuration.

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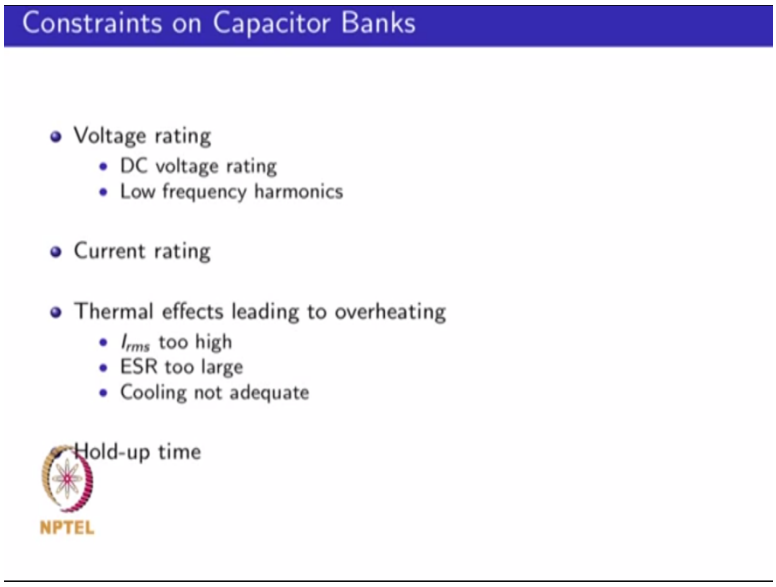

We looked at the started off with a DC specification of the, of the voltage which is linked to the ac terminal voltage specification with some additional inverter parameters. So, the other thing that we need to consider is, so the DC voltage rating was considered. So, we have to consider the effect of a low frequency harmonics on the voltage rating, in the last class we looked at, took a close look at the current rating. We saw that the current rating has thermal implications and it has implications on power loss and cooling and the temperature of the capacitor core which has reliability implications. There are other factors such as hold up time of the capacitor which can be important in d g application from the reliability perspective. We looked at a simplified model of the component, the capacitor component as a bath tub curve which is a commonly use model for reliability

and we came with a estimate for end of life. So, if you look at the model that we had for the capacitor.

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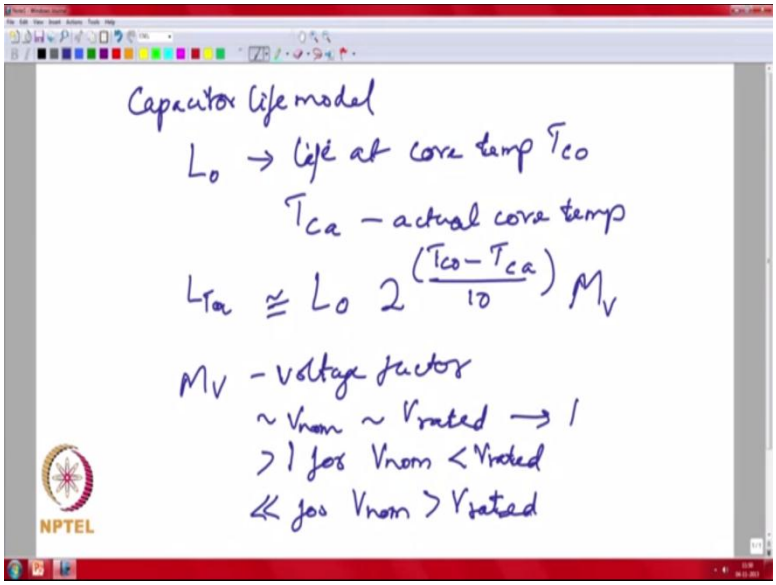

So, if we have the manufacturer specified L naught as the life at the at a test measurement point from the manufacturer T c naught and if you have data at the actual core temperature of T c a. Then, the life at the actual temperature is approximately given by L naught and we are considering a doubling of life for a 10 degree reduction in temperature of the core T c naught minus T c actual by 10.

You could also have a voltage multiplier effect. So, one factor is that effect on the temperature which is actually a very significant effect, so you could also have a voltage multiplier effect. So, if you are operating close to V nom is equal to V rated, then this has a value of 1and it is great greater than 1for V nom nominal operation of the capacitor to be less than V rated and rapidly degrading.

The capacitor, if the actual operation of the capacitor is above its rated voltage, so many times you can have a 400 volt electrolytic capacitor for a short duration for a few seconds. You might be able to take it up by few tens of volts above 400 volt, but if you hold it at that level for a long time. It will actually a get damaged in a matter of settings and, but for a short duration you can actually take it above rated voltage. It is not recommended for continuous operation or design.

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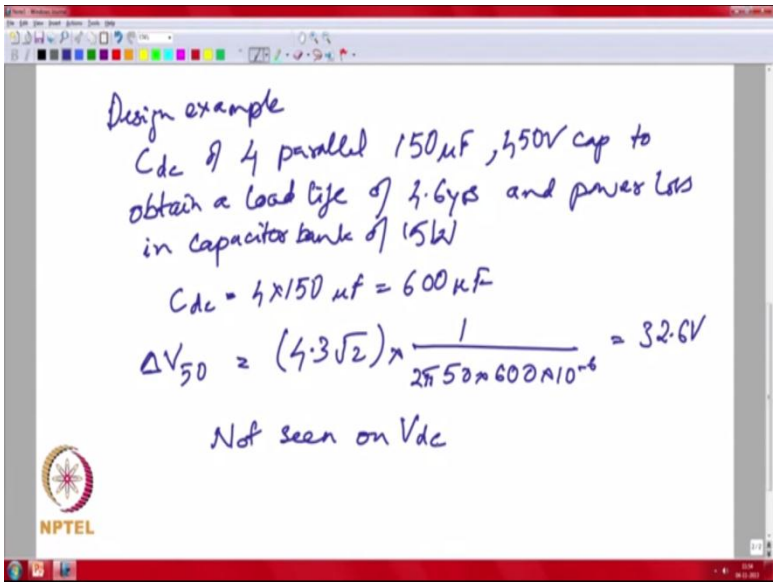

So, in the last class for a design of the capacitor one of the design points that we had chosen was, we considered a capacitor C d c of 4 parallel 150 micro farad 450 volt capacitor to a obtain load life of about 4.6 years and power loss in capacitor bank of a 15 watts. So, essentially what we had done was we calculated the current components.

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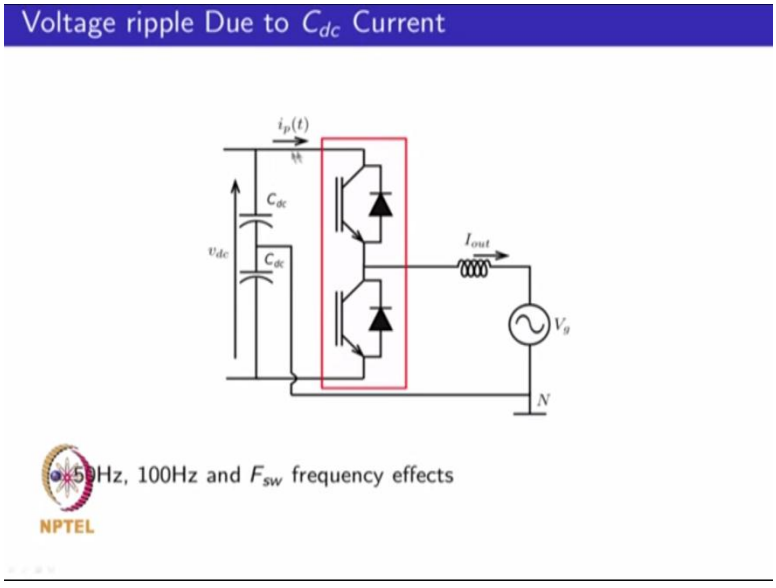

Then, we looked at what the thermal impedance, the from core to ambient is and we looked at the E S R. The values of E S R at the different frequencies and calculated the temperature. So, we got4.6 years and the loss in the capacitor in the E S R because of

varies current components totalled in both the top bank plus the bottom bank, each bank consisting of 4 parallel capacitors to be 15 watts.

Now, we are left with a to look at what is the final voltage ripple? That happens on this a capacitor banks because of the different frequencies. So, one frequency is the 50 hertz which goes to the centre tap another frequency is the 100 hertz which comes on the d c bus. Then, you have the switching frequency effects because you have the output low frequency which is getting chopped by the action of the invertors.

So, you have the high frequency effects, so to look at these individual components we have c d c, c d c is 4 into micro farad is 6100 micro farads. So, if you look at the 50 hertz voltage rippled your voltage rippled at 50. So, this is we had 4.3 amps flowing per capacitor bank at 50 hertz. Then, root 2 for the peak and the impedance of the capacitor to be 2 pie 50 into 6100 into 10 to the power of minus 6. So, this is about 33 volts, so we also can observe that this 50 hertz applies plus say, for example, if the current is positive it will charge up the bottom bank and discharge at top bank.

So, you might have plus 33 volts may be at one instant, but the top bank will have minus 33. So, the total voltage across the entire bank would be not affected by this 50 hertz or in another instant bottom might be minus 33 and the top might be the other polarity, but their polarities cancel, but on a individual bank bases. This is a important factor to consider, however on a total bank bases it may not be observed, it is not observed. So, it is not seen on V d c if you look at the 100 hertz effect.

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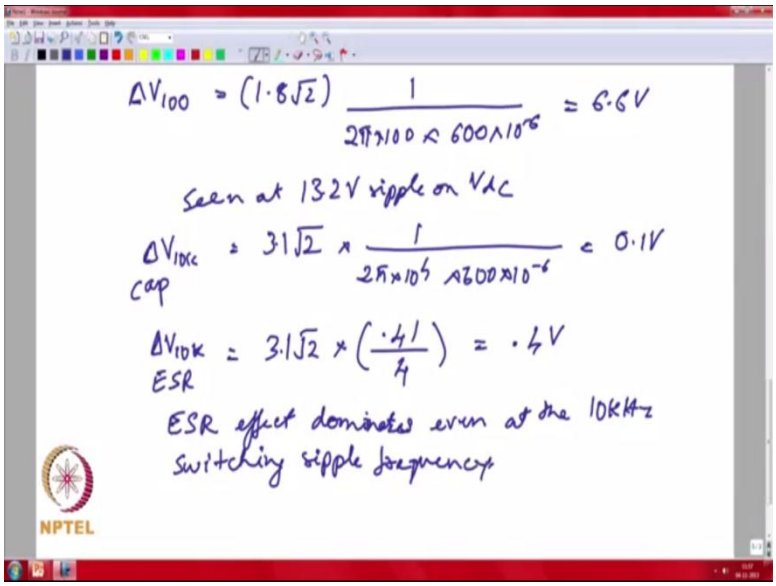

So, this is we had 1.8 amps flowing through the capacitor times root 2 to get the peak. So, the impedance is 2 pie into 100 into 600 micro farads. So, it is 6.6 volts per capacitor bank. So, it is because this voltage is actually getting this current is flowing as a differential mode current through the bank. So, you have plus 6.6 on top and plus 6.6 at the bottom. So, it adds up, so seen as it is seen13.2 volt rippled on V d c, if you look at the switching frequency effects and the switching frequency. We have considered is 10 kilo hertz, we have 3.1 amp of ripple again we are approximating it to be a sinusoidal component at a single frequency. So, 3.1 into root 2 and if you look at the capacity voltage drop, this is 2 pie into 10 to the power of 4 into 600 micro farads.

So, you have about point one volts. So, hardly it ripple at the switching frequency if you look at, so this is because of the capacitive effect. If you look at the ripple because of the E S R in the capacitor with a similar switching frequency current flowing through, so this is now the E S R of the capacitor .41 ohms at the 10 kilo hertz. There are 4 capacitors in parallel. So, you have about .4 volt due to the E S R of the capacitor .1 volt because of the actual capacitance.

So, at the switching frequency you could almost consider only the E S R effect the capacitive is the capacitor is behaviour starting to behave more like a resistor rather than as a capacitor even at the switching frequency. So, if you so the E S R effect dominates. So, if you look at what is a maximum voltage?

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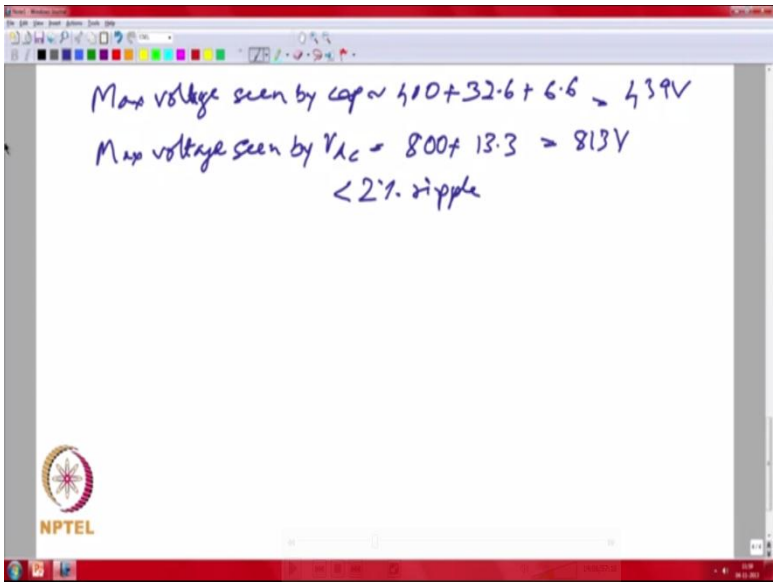

The maximum voltage is seen by the individual capacitors and just a assuming a worst case scenario. We would have a 4100 volts nominal for the individual capacitors d c value you have 33 volts because of your 50 hertz effect you have about 6.6 volts because of your 100 hertz effect. So, you have about 440 volts on seen as the voltage on your individual capacitor bank. So, you have actually a very tight margin of just 10 volts. So, your control has to be very effective, so that you do not have larger over shoots etcetera. When you are actually dynamically controlling the d c bus where as if you look at the overall total capacitor bank voltage.

So, this is now twice your 4100 volts which is eight 100 volts which was a d c value plus 13.3 which is twice 16.6. So, about 800 and 13 volts is your total voltage seen by the whole plus top and bottom capacitor back. So, if you look at the ripple voltage above your nominal voltage, so the ripple voltage is about 2 percent ripple overall which might seem reasonable it is a tight design, but it is actually durable. So, you might have to be conscious about your control design, so that you do not have large over shoots on the d c bus capacitor. So, you have to pre-charge it slowly, etcetera.

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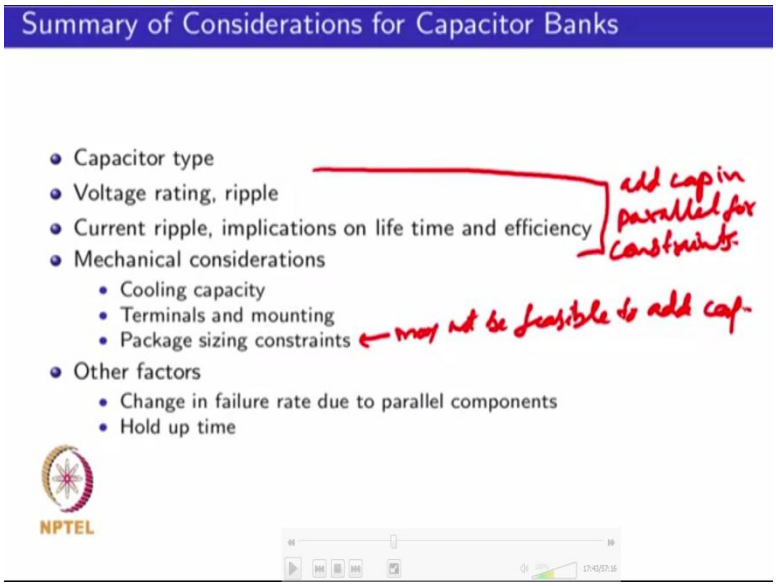

So, if you look at then the overall design of the d c bus capacitor bank. We saw that the first thing that you decide is the type of capacitor. You want to use, so in a voltage d c bus of voltage source inverter an electrolytic capacitor is common, in fact people have started looking at very high reliability inverters where you might actually eliminate electrolytic capacitors in the d c bus. You might actually use polypropylene type of capacitors, but its value is quite small and if you want a large value of capacitance to hold a d c bus constant you will need a large bank.

So, the capacitor type is important the voltage rating from both d c and ripple perspective is important the current ripple has implications on life and efficiency. If you feel that you are tight on these 2 factors: one might consider say, the considering more capacitors in parallel. However, you also have mechanical considerations which you need to consider from the cooling perspective, also if you put more capacitors in parallel. You have more surface area for your capacitor bank.

So, effect effectively help reduce your thermal capacitance as long as you keep your packaging space between capacitors constant, but you also have the mechanical constraint of a volume and size etcetera .Which mean that you cannot go on increasing the number of devices that you could add in parallel. You end up now taking lot of spaces.

So, from your packaging constraints you might have mechanical constraints means, you might have sizing requirement which might prevent you from adding more capacitors. You also have factors like a if you add more and more capacitors in parallel in the system. You are considering components that are increasing. We know from your reliability studies that if you put more and more components into a physical system the chances of failure, especially at connections terminations breakage of term some problem at connections can increase.

So, putting very large number of components in parallel is also not realistic solution from the perspective of component reliability. So, people have looked at what is a reasonable trade of in terms of the voltage ripple current ripple perspective, but at the same time not having too many components overly large number of components also from a cost perspective. If you put too many in parallel your cost might actually go up quite sharply.

Now, will actually look at a the one of the analysis that we did for evaluating the current in the capacitor and the life of the capacitor was actually the switching models. What are the way forms in the capacitor due to the operation of the single phase inverter? So, will now take a closer look at the switching model of the power converter?

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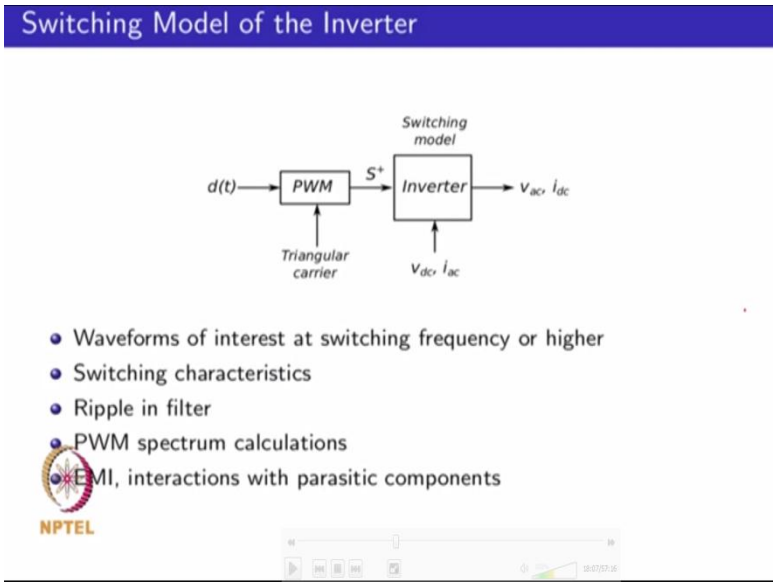

So, if you look at the leg of the power converter. We have we looked at the earlier the leg of the power converters modelled as a single polled double code switch and if you look

at overall invertors structure. You have duty cycle coming at to your P W M block where you are doing a comparison between your duty cycle and a triangular carry carrier. So, we were considering these cycles in 0 and 1 and the triangular carrier is begin going as a in a symmetric manner from 0 to 1 and back down to 0.

The output of the comparison is the command to the top switch of your inverter which is S plus and we also know that this model were we are considering exchange of power between into sources essentially exchange of power between you are a c and d c side. The variables that we consider as input to the input the switching model is the way are the 2 variables that are essentially varying slowly in such a model. The one variable varying slowly is the d c bus voltage.

It does not change rapidly because of the fact that we have a large capacitor typically connected to the d c bus. Another slowly varying quantity is you are a c current again the reason, why we consider a c current to be slowly varying, because we have a output filter which is typically inductive filter. The inductor prevents sudden changes in currents. So, we consider the a c quantity to be also slowly varying. So, the inputs to this particular inverter model are your d c voltage and you are a c current and v in and your i out i a c. We have labelled in some of the diagrams i a c as i out vocalized voice output of the switching model is actually the quantities that are varying quite rapidly, which is your output a c voltage? Which is a V o n? We have labelled it as V o n in our diagrams means, output voltage with respect to neutral or it can be voltage output voltage with respect to negative bus, also mething that can be very output of switching model is your d c bus current which can be a positive bus current negative bus current etcetera.

If you look at switching model of the of such power converter, the question you could ask is, when would such model be required? When could be useful to use and definitely it is going to be useful to us. If the item of interest it is actually close to the switching frequency or may be something even which is a higher than the switching frequency, because of the rapid transaction that can occur, because of the switching action of the inverter.

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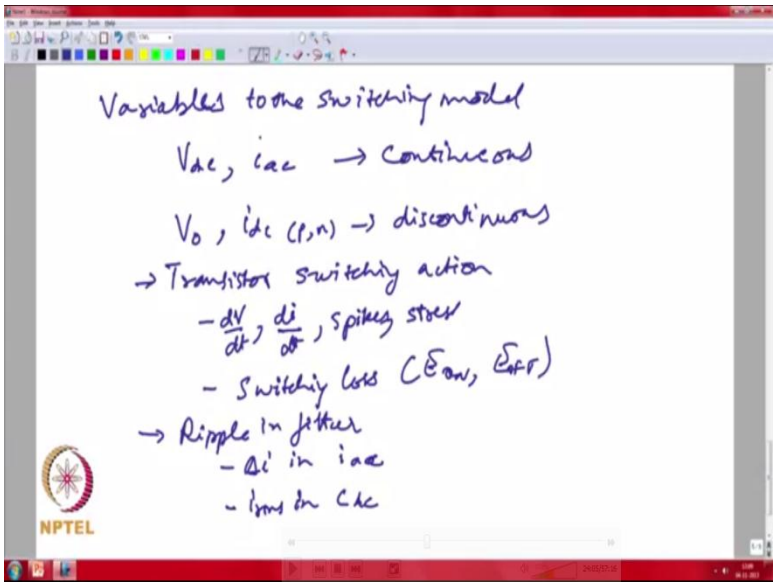

So, if you look at the items of interest. So, you're input the variables are V d c and comma i a c, which we consider to be smooth, to be continuous your outputs are 0, which can be V o n or i d c is can be positive or negative, d c bus which are discontinuous. So, if you need to switching model considering to say. For example, the switching action of the devices a the diagonal operation. For example, if you have d v d t spikes d i d t spikes.

You might have stress on the inverters stress on the component s on the transistors etcetera. You definitely need to look at the a switching action. You may also be looking at the switching loss. So, if you consider it e one off etcetera these are switching characteristics related a. So, if you are looking at detailed V form bases that defiantly would it need a switching model you may also need to consider ripple effects.

For example, ripple in the filter for filter design. So, you might consider delta i in i a c. We consider i a c to be continuous, but it might have some underlined ripple because of the switching action of the inverter and you want to decide how big in that would you want to put in the circuit. You also saw that we could calculate ripple i r m s current c d c noise. So, factor such as that such factors can be calculated from the switching model of the inverter and you might also be interested in P W M spectrum calculation.

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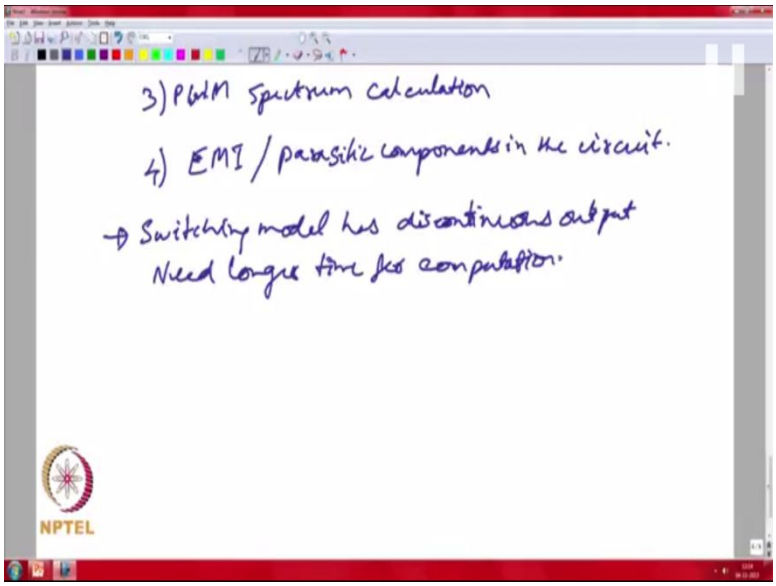

So, if you look at the exact expressions for the P W M spectrum a of say, a sin triangular P W M you get the cell functions etcetera. You have components not just at the switching frequency, but also at the side bands. So, more sophisticate P W M modulation methods, if you want to study it close closely you want to definitely look at the switching functions.

The switching model of the inverter another aspect which when you study closely it becomes a important a aspect of all power converter design is, how to handle electromagnetic interference e. This interferences effects are actually closely guide to the switching effects the d i d t d v d t in the power converter and also another part of the aspect of inverter itself which is the parasitic components in the circuit.

So, a parasitic component that we recently studied the E S R of the capacitor what we want to be purchased just on the capacitor. We got resistance along with a capacitor, which is causing problems. Similar, when you go to purchase a transistor, you do not just get switch you have lead inductances. You have capacitance not just from your collector to emitter of your transistor switch.

What you can have capacitor between your silicon chip to your heat sink and these capacitances can actually carry currents. Those currents can actually lead to significant E M I concerns in your power converter and these components preliminarily. You might

assumed to be ideal in the sense that you would assume that those parasitic or not there, but in the actually realisation in the power converter, if these effects are con ignored.

Then, E M I becomes problem which addressing at a later stage becomes issue. It is always good to look at what parasitic components are there in your circuits. You have stray capacitance between your magnetic windings and your body frame of your inductors transformers etcetera. So, these parasitic components, if it can be included up front can actually be included with the switching model of the power converter to see what would bed i d t? Now coming with inductive parasitic.

What would be in induce voltage or d v d t? Now, with parasitic capacitance what would be the search spiky current that go in to such a capacitor? So, these are these analysis this type of switching model analysis can give you a feel for what is the worst component in your layout which gives you maximum headache from a E M I prospect. It is, but actually drawbacks of the switching model 2 and one of the drawback of the switching model is related to the fact that output of the model is discontinuous.

So, if whenever you have discontinuous functions, you need more data points to actually describe it which more points means, you all have longer computation and you need more memory requirement. So, you always would like actually see, where you could get way something simpler and the something simpler is the average model. So, one can look at the average model and the mean benefits of the average model is when we are looking at longer time frames.

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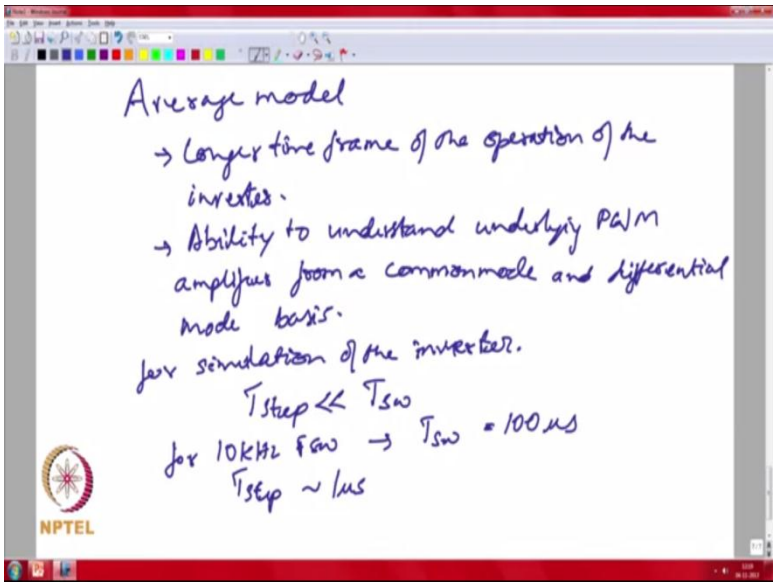

One important area you looked at longer time frame of the operation of the inverter is when you are actually at how to control inverter. So, whenever you are looking at from control design perspective you might say I want to look at how do how does a m p p t act over minute duration rather than over micro, seconds generation where the switching frequency effects occur.

So, if you are now wanting to do longer terms relations over multiple fundamental cycles may be when you are looking at much longer at duration like missions cyclic, mission life times days of the simulations, where you are looking at the temperature effects which cabinet temperatures can actually take hours to settle. So, you might want to look at then the model which can be required less lesser number of computations, which can actually be solved in shorter time frame and in a simplified manner, but can capture most of the effects of what the switching model can do.

So, another aspect that can be covered by the average model is ability to understand underlying p w m amplifier. For example, you might have low frequency's spectrum of your p w m amplifier in many advanced p w m modulation methods likes space vector discontinuous modulations etcetera. One might consider adding a third harmonics. So, you want to look at path for the third harmonist's in the overall system to the filters etcetera. You also have low frequency non ideal ties like distortions death bands etcetera and you may want to look at the model of your inverter from a low frequency

perspective to study these effects on a closer manner, if you look at the time steps that are used for the current computation for the inverter.

So, if you consider say a switching frequency of 10 kilo hertz considering a switching period of 100 micro seconds. So, you are talking about your time step to be much lesser than your T s w, your switching period. So, if you are talking about for 10 kilo hertz f s w you are talking about time step T s w of a 100 micro second. You might take t step of a may be 1 micro second. If you are looking at something on fine grain bases you might even take it lower if you are taking at d i d t's d v d t's, etcetera, during switching action, etcetera.

You can see that you have constraint of your computation time to yours witching frequency where as if you now look at a on an average bases you might actually just do one computation per switching period. So, you are talking about benefits advantages of a 100 to 2000 times increase speed in your computation. So, mething which may take hours on a switching model can be done may in a few minutes or may be just a minute in your average model. So, to look at the average model will start off with again with switching model of the power converter, and we are familiar with the switching model which is the single pole double pole through switch.

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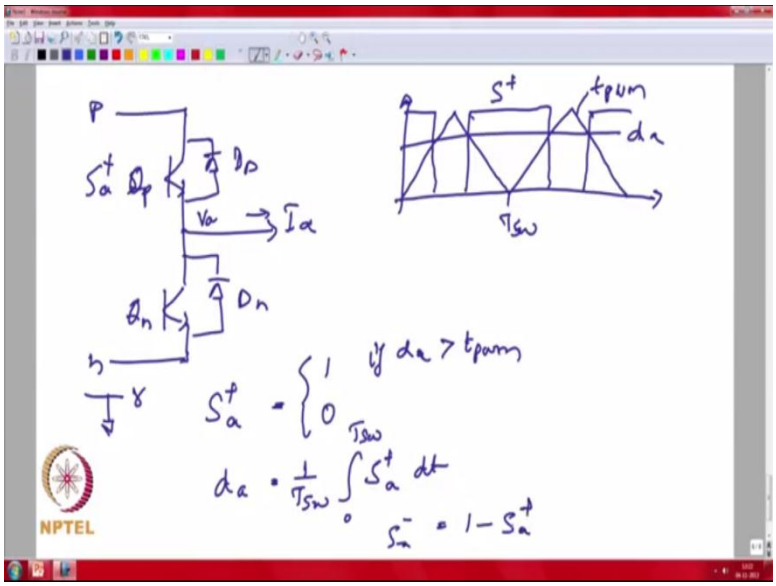

So, we considered switch in parallel with the diode this is transistor Q p and Q n and switching is S plus for say, if you have consider this as a and this is i a current flowing

out p and n and p w m action is generated by sin triangular comparison. So, we have to a triangle going between 0 and 1 and we consider it with respect to reference say, some reference r. So, we have v, v a here if this is a V a. So, in top of midpoint of topology that we can consider as a single phases base, we had considered the neutral to be the centre point to which was the reference.

So, we haves plus for switching function of leg a is 1. If d a is greater than for triangular say, p w m or 0, otherwise we also know, how to relate the duty cycle back is 1 T s w integral 0 to T s w S plus a d t and the switching of the bottom switch is S a minus is 1 minus S a plus. So, we can actually write an expression for V a r.

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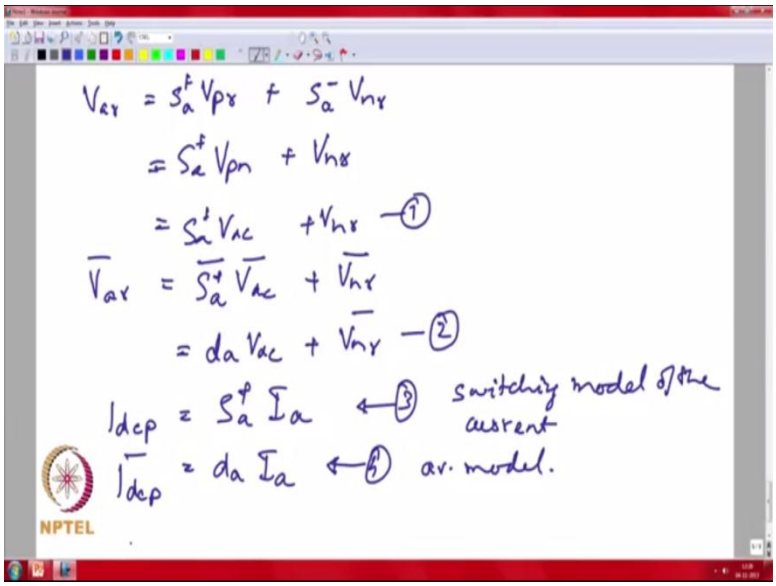

The voltage a with respective to r is S plus V of p with respective r plus say S minus V n with respect to r and we can make you of say S a minus 1 minus S a plus. We gets it's be equal to S a plus V p n or V p n or V d c plus V n r. So, we have simplified model ford c output voltage S. You have considered it as 1, so this is switching function description of our leg a. Ok? And if we then average this particular expression over one switching period will put a bar to indicate average V a r.

So, if you now consider the average of S a plus V c will make a additional assumption that V d c significantly over once switching period. So, you get the average of the S a plus V d c and it is the V d c average plus V n r average and we know that the S a plus average is d a and d c is not changing significantly. So, we have V r is d a V d c plus V n

r. So, this is a the one is switching function model and the 2 represent essentially the average model and the you can actually drop this bars without large change in any significant ambiguity in what type of model. You are writing because you know that the switching function represents the discontinuous function whereas, d a represents something that is smooth function which is continuous.

So, similarly, one can actually write the switching function relation between your d c bus positive current i d c piss a plustimes i a which is the switching model of a the current and if you then hit the average here, taking the average of S a plus i a. We are again going to make the function that i a does not change significantly over one switching period. This might be looser on the assumption compared to assuming to d c bus voltage staying constant o t does have pre implifications. For example, this type of model you might have cannot be able to have average when you are i a put frequency is getting very close to your switching frequency, but for sufficiently large difference between your fundamental frequency and switching frequency.

We could go head and take the average and we have i d coverage is equal to a times i a. Similarly, you could take the model for the negative d c bus current i d c for the negative bus is S a minus i a, which is S a plus S will get 1 minus d a 2 times i a to be a negative d c bus current. So, if you now draw the model of the average group model.

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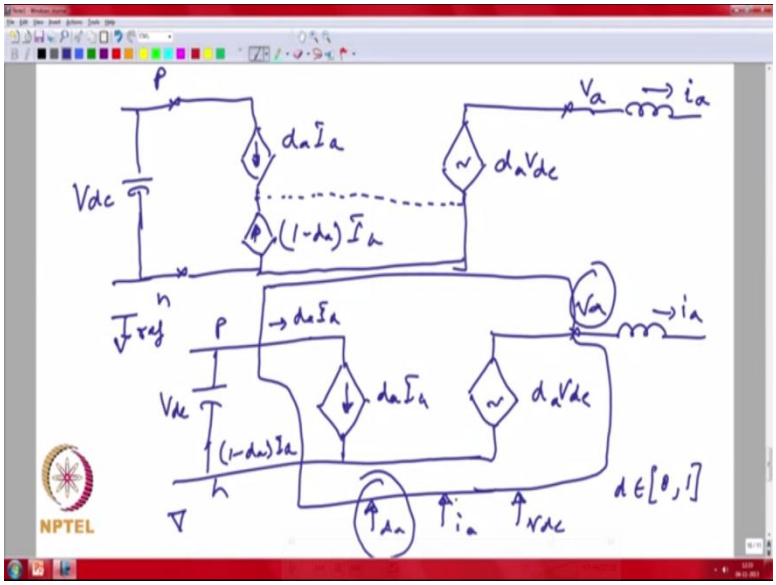

You have essentially a positive bus, negative bus, your d c bus capacitor bank supporting your V d c. You have d a I a time coming in from your positive d c bus, you have one minus d a I a respective n p. If you look at here, output voltage you have d z 10ds V d c generating your output voltage V a, which is going out through your filter.

So, it is your continuous current which is your i out your i c. If you at the voltage d a is actually with respective n and here you what you end up within this model is that this particular point is also link to the same reference. So, the bottom part of the model you have a current source which is going into a short circuit. You find at this particular part is redundant then you can actually simplify it and you can make the model to be a something simpler. You have essentially d a I a, so this current is now automatically d a I a and because this current is d a I a. This current that is going through negatively d c bus is actually one minus d a I a.

So, it is satisfy is a constraint is your as what is their shown away here a and the inputs to this particular model or essentially a duty cycle. Your i a your V d c and your V d c and typically in control application you will have measurement of your d c bus voltage. You have your a c current measurements, your controller is actually outputting your to the duty cycle and then you could actually in cooperate models such as this for the one leg of the power converter, so instead of using the average value.

Now, the value of V a with respect to reference, now continuous quantity rather than a discontinuous quantity and similarly, the currents that are coming in. Now, continuous quantities rather than discontinuous quantities also the assumption that we have made in this model is that the duty cycle belong to the range 0, 1.

If you duty cycle goes out of the range and find that your energy conservation equations may not be satisfied, your amplifier cannot be generate more voltage, then what is available? So, you need to ensure that you're respecting your duty cycle constraints you also have other non ideal ties that you have ignored in this model. You have ignored non ideal ties such as dead time switch voltage drops etcetera, which might effectively reduce the actual voltage that would be obtained that the output of this average model.

So, you can ask a question now in this average model can we, can we take this particular inverter to be amplifier again? So, if you consider this particular amplifier as having a very stiff d c voltage. You can see that the relationship between in your duty cycle input

and your output voltage V a is essentially just a V d c. So, if we consider V d c to be constant.

So, essentially gain times your input to be your output so many times, we might further simplify from your output voltage perspective your inverter to be considered as a ideal amplifier. So, you can, but if you look at it from reverse perspective where you are looking at the currents that are coming into your d c bus. Your duty cycle might be a sinusoidal quantity your input current would be a sinusoidal quantity. So, you might you may not be able to take a simple gain model as the relationship between your currents at the input and output one current might be 50 hertz and then your ripple.

Now on your d c bus is, now starting to a current at a 100 hertz etcetera, however between your duty cycle and your output voltage you have the same frequency effects. So, you could consider it to be just a linear amplifier with simplifying assumptions regarding the d c bus.

Another factor to be consider when you are the modelling inverter especially considering the when you are looking at a one leg, is a in this particular case. If you had this is for one leg of the power converter if you have 2 legs, you could consider 2 such models in parallel. If you have poly phase you could consider multiple such legs in parallel. So, this particular average model can be generalized. So, another factor to consider when you are modelling the converter is the effect of P W M delay.

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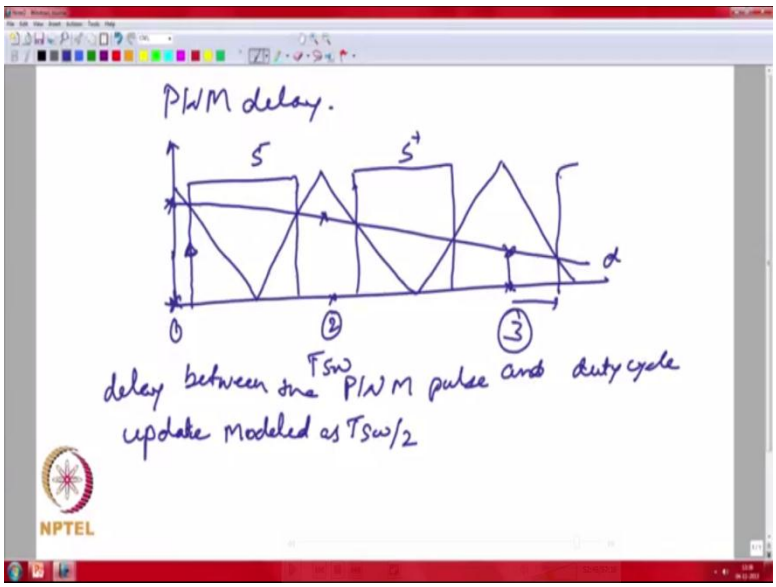

So, this is especially important when you are considering the bandwidth of the converter to be a close to the switching frequency in engineering of 10 when we consider something to be close or far we consider number such as factor of 10. So, if you are switching frequency is 10 kilo hertz and if you are considering the control bandwidths below 1 kilo hertz. Then, you might say, you could may be ignore the delay effects, but for designs where you want to actually consider switching frequencies which are much closer to your bandwidth.

So, you may want to have a bandwidth close to 1 kilo hertz, but your switching frequency may be just 2.5 kilo hertz. The reason why you do not want to take your switching frequency is high you know that your switching losses would go up with frequency. So, you do not want to take it to be much higher than what is really just required. Then you will have to may be now look at what are the delay effects that are there because of the P W M also many times in modern power converters.

The P W M delay gets added on to the computational delay in your digital controller and the overall delay becomes a important factor. So, if you consider the P W M operation and say, duty cycle coming down. So, we in a digital controller your actual point at which updating your duty cycle might be at regularly sample points. If you are having a analogue type of implementation might be able to have the fact intersection of your sine wave and your duty cycle wave.

Your triangle people looked at the difference between regularly sampled a naturally sampled P W M and the performance is actually quite similar. There are some pulse position changes because of the sampling, but people have found that you get similar performance in the 2 methods, but you can see that in case when your duty cycle is close to 1, a update over here will give you a fast response for the operation. Your output voltage goes up to a high value very close to when your actuation, your actual computation is updated whereas say, if you look at the .3 you're updating over here.

Now, you have a delay between when your actual witching action is taking place and when the computation is being provided from your controller and this depends on what is the value of the pulse that you are trying to get etcetera. It is a varying effect, but it is modelled as a, as a equivalent delay model of T s w by 2. So, another way of looking at

why whether one can justify such a model for the delay, one can look at the expression for the average output voltage and the volt second match at the output of the inverter.

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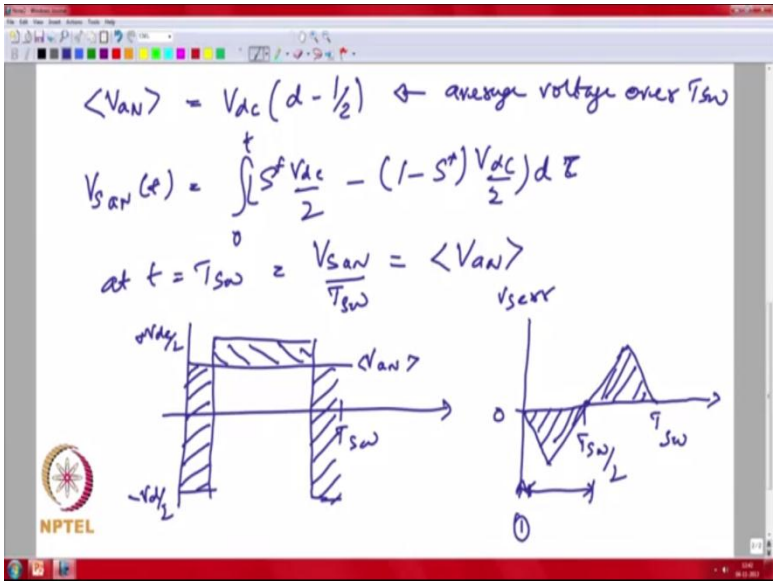

So, if you look at the average output voltage say V a with respect to say, the neutral in our inverter model is V d c into d minus half. So, this was the average model over T s w. So, if you look at the volt second on a to n bases, you can describe it as integral of with respect to time T s plus V d c by 2 minus 1 minus s plus V d c by 2 d tau where tau is the time with respect to a doing your volt second integration. So, at T is equal to T s w.

We have volt, second a n divided by T s w by definition this is what your average is V a n average. So, if you look at, what this means if you look at your p w m switching cycle? You might have the output of the inverter going between 0 plus V d c and minus V d c by 2. You might have an average value and by definition the average cancels out the positive and negative volt second error and if you look at then the volt second error that you are built building again assuming that your error is 0 to start with. So, volt second error you are starting off with 0, you are having some negative volt second error. Then, you are volt second error is going to the other side and coming back.

So, if this was instant one and which you are updating your p w m operation the point at which your error comes back to 0 is at T s w by 2 and at T s w and subsequent points. So, if you look at a control action, the time to take for the error to go back to 0 is T s w by 2 and many times the delay between when you give a command. The output to go

back to 0 and all the subsequent ripple would be such that the positive and the negative volt seconds balance out.

So, one could model, the delay effect of the p w m leg to be T s w by 2 from also from a volt second perspective volt second error perspective. So, this of10 in power converter is used along with the model of your output filter, people when they model the inverter for digital control might a model the inverter as a 0 order hold. So, if you look at the phase delay of a 0 order hold the where the 0 0 order hold is being updated at a rate of T s w is actually. The delay is T s w by 2, so many times people use a 0 order hold model for the inverter with the subsequent analogue filter, etcetera. In case there is subsequent sufficient separation between switching frequency and your control frequency, then people might be even justified in ignoring such delay effects.

Thank you.