Power Electronics and Distributed Generation
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Lecture - 34
AC filters for grid connected inverters

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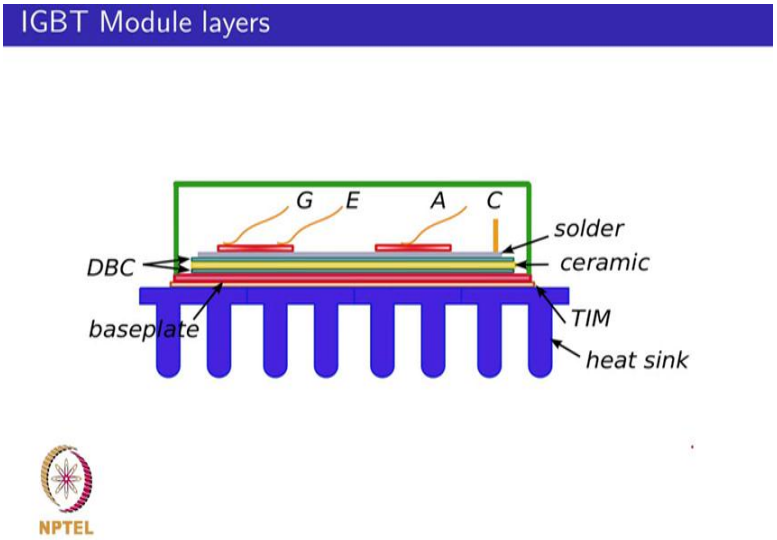

Welcome to class 34 in topics in power electronics and distributed generation. We have been looking at the structure of the an IGBT module, and we have seen that it consists of multiple layers, and each layer made up of different material. And during operation of the power module, this layers heat up and cool down, they expand and contract because of the terminal variations. And they can expand and contract to different extents, resulting in stress between adjacent layers. And the stress can actually lead to strain or plastic deformations which can actually cause damage.

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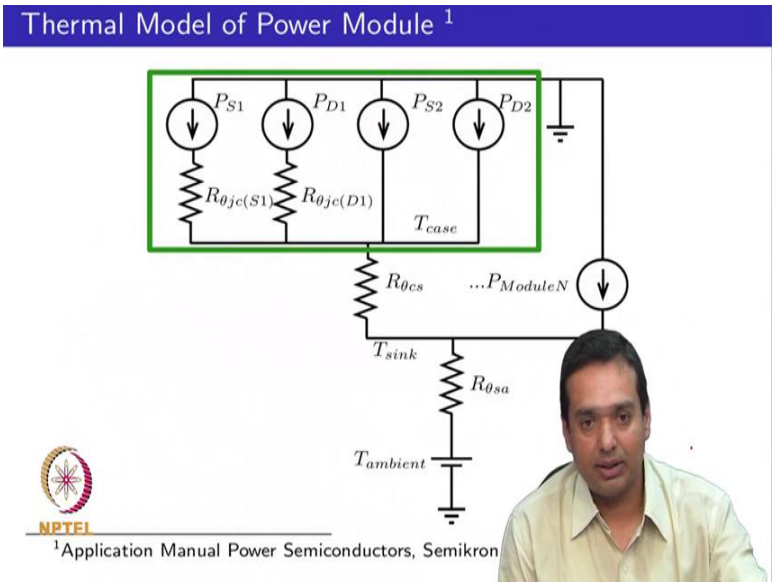

And we also saw that different parts of the module will operate at different temperatures, your junction temperature would be one, your top surface temperature totally would be different, bottom surface temperature of the chip would be different. Coming all the way to the case where, we should be another value. So, there is a thermal gradients within the power module and because of these variety of reasons you have the buildup of stress occurring within power module within, when it is in operation. Good reference to look at for the terminal modules and terminal evaluation of the parts in the conductor is a applications manual of manufactures such as a semikron, A B B, oil peg, ((Refer Time: 02:05)) wide range of manufactures. They provide good information on how you could actually do a accurate characterization of the power of semiconductor.

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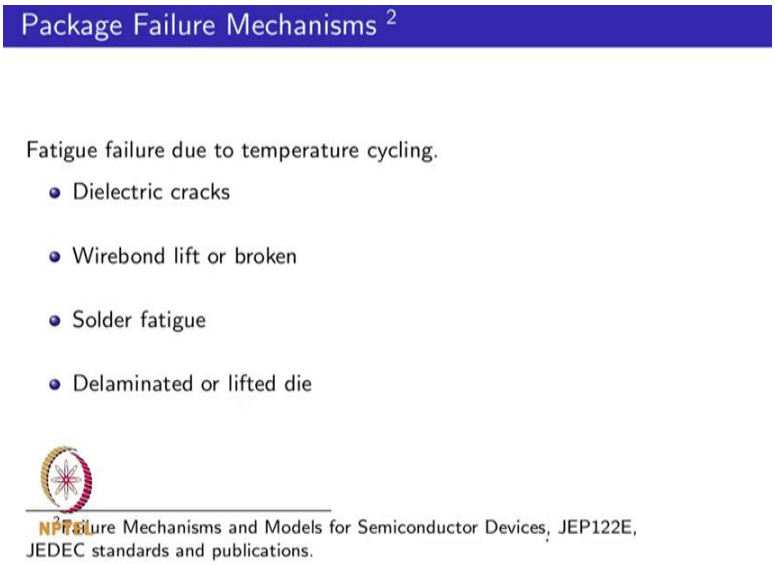

And because of a the heating up and cooling down the temperature cycling, the fatigue can cause cracks in the dielectric ceramic layers, isolation layers. Or it can cause a wire bonds to break form cracks eventually break and lift off from the chips surface, it can cause fatigue in solder joints, the chip can delaminate from the sub straight and the lift off, again loosing electric connection, impacting the power distribution within the chip and the power handling capability of the power module, eventually leading to failure. These mechanisms are actually described in the reference by jedec standards and publications, so these good standards to take look at.

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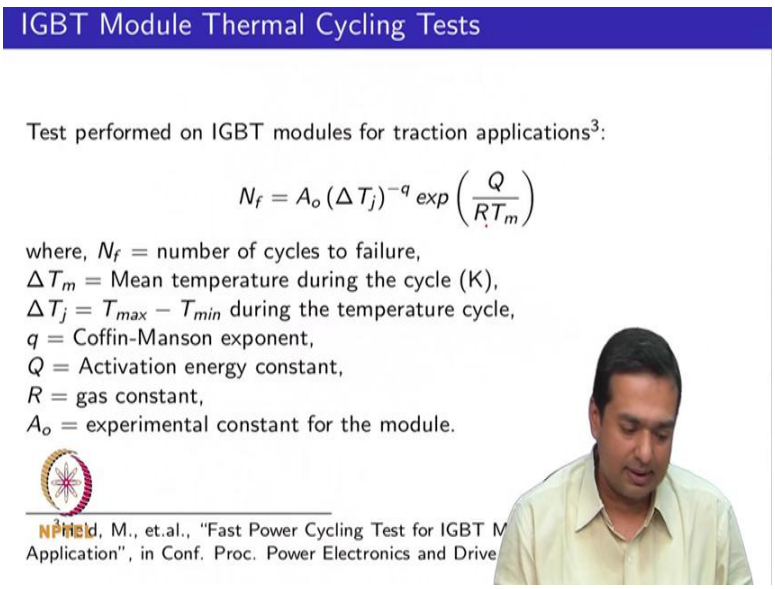

We have seen that the thermal, the cyclic, a life to failure due to the thermal cycling can be model by the Coffin-Manson equations, and the version of that was used by this group early in the mid 90's to evaluate the life and the impact of thermal cycling on power modules. And they came up with an expression, showing that your junction temperature variations delta T j and your mean junction temperature could be factors, which can actually affect the number cycles to failure.

So, with that, we then looked at what could be the impact of looking at different junction temperatures, T j max for your design. So, we could design with a T j max of a 125 degree centigrade or 135, 150, what would be the impact of doing that on your number of cycles to failure and the service life of your power module. And we saw that we could use that as designed guideline based on your application requirement. And in this particular case, we are looking at system where it is going to a full on full off condition. So, it was essentially between, cycling between two temperatures, but in a practical application, we know that…

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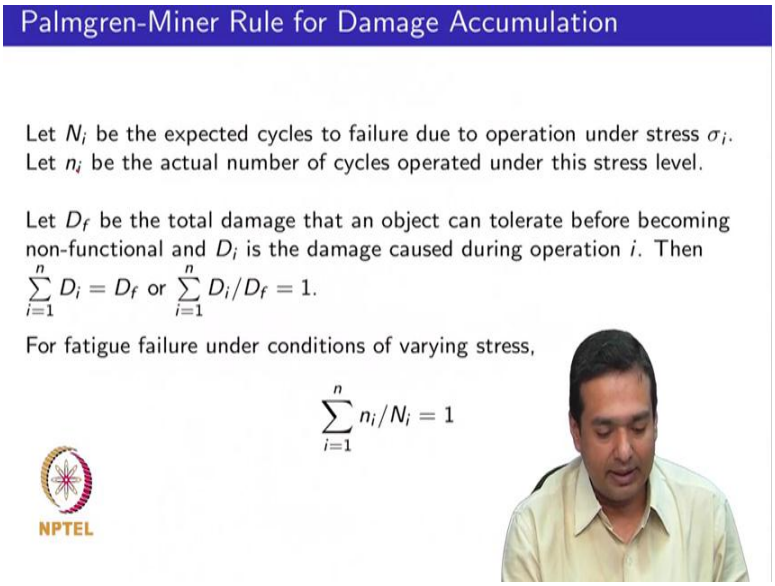

You will be operating at multiple temperatures, and not just at two temperatures. So, you have different cycles to failures depending on between two temperatures your, which temperature you are cycling, so you are how you might be operating under different stress levels sigma I, and if you have N i be then number of cycles to failure for the stress condition sigma i.

And small n i be the actual number of cycles that are experienced in your actual applications, then we looked that how you could evaluate the overall life, based on the concept of accumulation of damage. And this is essentially the miner law Palmgren-Miner rule for accumulation of damage and a evaluating fatigue failure under conditions of varying stress.

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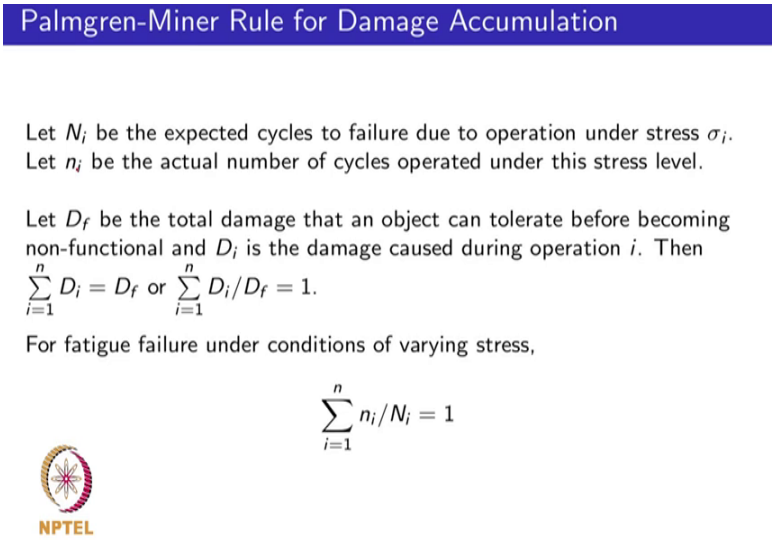

So, will, before we go to the example, we will looked at how one could then consider conditions of varying stress, essentially what you are doing as you are looking at longer periods of time, over which your semiconductor would be exposed to similar conditions of a loading. For example, you might have daily loadings, routines in a industrial environment, you might have weekly loading a types and transportation or house hold environment, and renewable energy systems, winter burns might see similar level of wind patterns, whether patterns on over many months or annual bases.

So, you have periodic loading conditions and then you are splitting it up into smaller cycles over the period, and you are identifying the cycles to failure for each small sub period. And then you accumulate the damage over the entire period and see how many such longer periods would be required for the damage, normalized damage to actually become one.

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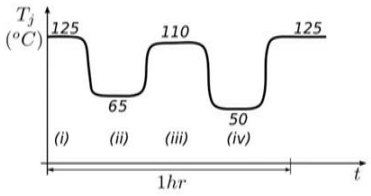
Periodic Loading of the Power Converter



	ΔT (^oC)	T_m (^oK)	N_{fi} (cycles)	D_i/D_f
(i)	60	368	9.61×10^4	5.2×10^{-6}
(ii)	45	361	6.88×10^5	7.27×10^{-7}
(iii)	60	353	2.84×10^5	1.76×10^{-6}
(iv)	75	361	5.35×10^4	9.35×10^{-6}
Total normalized damage per hour				1.7×10^{-5}

So, now we will look at an example, where we are looking at a case where your maximum junction temperature is 125, but you are varying between multiple temperatures. So, overall you are first going from 125 degree centigrade to 65, then going back to 110 coming down to 50, then going back up to 125. So, to evaluate the numbers of cycles to failure, you then look at this 1 hour duration, and you have, you could consider one cycle has going back in forth between valley to peak back to the valley or. So, if you are going from only in one direction, you could considered that to be half a cycle.

So, in the first transition from 1 to 2, you are having a delta T of 60 degree centigrade and the mean temperature is 125 plus 65 plus 273.15. So, that mean temperature is 368 degree centigrade, and then you seeing the expression for cycles to failure. And the parameters that we are given in the previous example that we considered last time, we have the number cycles to failure to be 9.61 into 10 the power of 4 cycles to failure.

And in the second case, when you are going from 65 to 110, your delta T j is 45, the mean temperature is 361 Kelvin, the 110 to 50, the delta T j is again 60, but now your mean temperature is lower 353. And the final translation 50 to 125, your delta T is 75, and your mean is 361 and for each of these conditions, we are using this expression to obtain the cycles to failure.

And then if you look at the number of the, the number of actual operational cycles under each conditions in a period of 1 hour you are you are having half a cycle in condition 1, you are having another half in condition 2. And so each of this is actually, each of the value of the N i is 0.5 and you are D i by your normalized damage would be 0.5 divided by the N fi. So, you are 5.2 into 10 power of minus 6 is 0.5 divided by 9.61 into 10 power of 4.

So, you have the normalized damage for each of those sub durations. And essentially what you do is, you accumulate the total normalized damage and on, in one period which is essentially 1 hour, your accumulated normalized damage is 1.7 into 10 power of 5. So, the question is how long would this particular semiconductor equipment last, it would be your T rep divided by your total normalized damage during the T rep, which is 1.7 into 10 to the power of 5, and this is 5.87 into 10 to the power of 4 hours. So, converting from hour to the years, this is about 6.7 years.

So, you can get an estimate for what the expected life would be in a mode complex operating cycle of your equipment. You could also then consider in your, look at an actual loading situations for example, in a ((Refer Time: 11:34)), you might not have a clean transitions, which you could identify it could be a much more complex nature of your way form of your junction temperature as a function of time.

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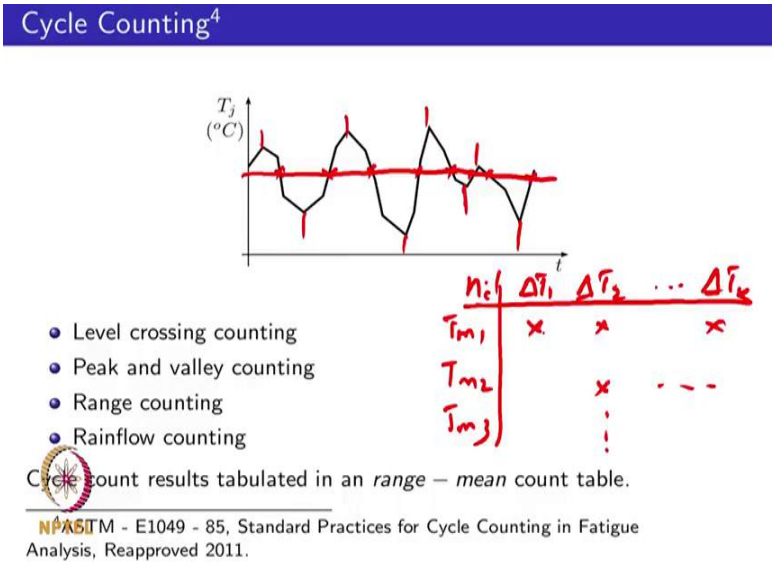

Also you would have a large durations of time, might be many months of data which you are actually trying to analyze. So, one need to find exquisite methods, so actually count the number of cycles, and you are looking at multiple information one is what is the delta T, and also what is the average temperature or may be the minimum temperature. You are also looking at what would be the net result cause by such a variation and its impact on the expected life. And one way to do such counting of cycles, is a the standards for is, one is the ASTM standards, practices for cycle counting for fatigue analysis. One way to do a cycle counting would be to actually may be a draw a line through the cycle.

And in fact, it will not be just one line, you will have multiple lines because you are also interested in the range. And so when you talk about a range, it is essentially the difference from the peak to the valley, and not just the level at which the number of cycles have been counted.

So if you could count the number of positive going and the negative going points in your level, and you can see that you could for example, just count to the positive going levels and for a sufficiently long sequence of data, that would be just twice the number of counts if you are doing both positive and negative level crossing. And you could use that information to actually look at how many cycles were there. Another way of looking at it would be at look at where you have points of reflection in the way form where your d by dt is going through 0.

So, identifying your peaks and the valleys. Often you may want to ignore extremely small cycles because we have seen that extremely small cycles, very narrow cycles, will not cause temperature change in there or the temperature change would be in the plastic range of deformation. Also we saw that because of the thermal capacitance, it is not just the instantaneous loading it is filtered through the thermal time constants of your module and your heat sink.

So, the wave forms would actually be much smoother then looking at it as a instantaneous power dissipation times your thermal impedance, thermal resistance of your thermal module of your system. So, you could calculate your peak in the valleys and use that to actually do this cycle counting. Another way is to look at the range counting.

So, you look at the number of values where your delta T is going from one particular level to the next particular level, and keep counting the number of such changes all along the way form starting with the largest to the small. Rain flow counting is another range calculation where you are not just looking at say a positive range are also including the negative range.

So, for example, you might look at the highest peak, the next highest peak and the valley in between, and you would count that as a cycle and then reduce the way form and continue with the counts. So, the variety of ways of doing the counting, your statics that you get would be slightly different because depending on the number of the way in which you are counting, but the net result can be then used for your thermal evolution of how many cycles to failure, you could expect within such a module.

So, the net results would be in the form of a table, essentially a table would have the number of cycles your n I, small n i which is what you are trying to count, and you are looking at delta T 1, delta T 2, upto delta T k. So, delta T 1 might be cycles which are 20 degrees from peak to valley, delta T 2 might be cycles which are 40 degrees from peak to valley, delta T k might be cycles which are 120 degrees from peak to valley.

So, essentially you are looking at the range over which the cycle is occurring, and the other column is your, will be the mean temperature. This particular variation whether it is occurring at a mean temperature of 50 degrees or 40 degrees, or whether it such a 60, 70.

So, you might have T m1, T m2, T m3, so at the end of the cycle counting, essentially you will have values that are populated all along this table. And then you could evaluate the number of cycles to failure for each of the this conditions, then use the Miner's law to accumulate damage to look at what would be your actual expected life time of the equipment given that particular design.

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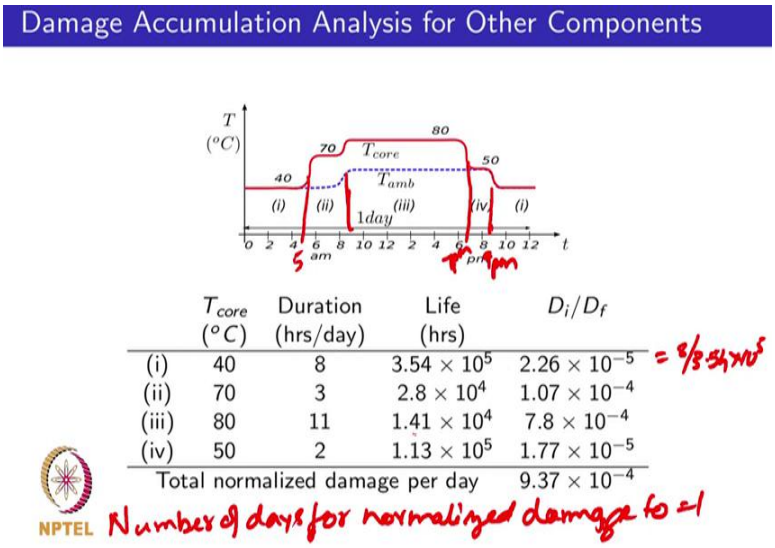

So, we have looked at how to look at the concept of accumulation of damage for parse semiconductors device like IGBT module, we could also use the concept of accumulation of damage to other components say for example, we could think of how it could be applied to the case of a, in case you are making use of the capacitor because we are not operating the converter always at its maximum power level. You might be operating under a mix condition were your core temperature might be going over difference cycles depending on the loading, the ambient, etcetera.

So, here we have an example, where you have converter, where you are making use of capacitors, where you expect a life time of 5000 hours at a core temperature of a 95 degree centigrade. And your power converter essentially operation say in industrial environment, and say your ambient temperature which is increasing from 40 degree centigrade to 50 at 9'o clock in the morning, and it is reducing 12 hour level at 9 pm. And your converter is operating from 5 am to 7 pm.

So, you might have a more complex operation like this and you want to see what could be the expected life time, when you are having conditions of varying temperature. Then you could use the same concept of a accumulation of damage to see how you could look at the life of the capacitor in such a more, in a varying operating condition. So, you could then look at each duration.

So, look at the duration when it is operating at night, at may be at no load, at when the ambient temperature is low at 40 degree, as core would be the same as the ambient temperature. So, when it starts operating, the temperature gets hotter by, the core gets hotter by 30 degrees.

And at once the ambient temperature also start getting heated up around 9, then it goes from 70 to 80. When the power converter is shut down, it comes back to say 50 and then at night it goes back to 40. So, you might have operation such as this. So, you could then look at the number of due hours a day, it would be operating under each of this condition and what would be the corresponding core temperature under this different conditions.

So you are then looking at what is life of the particular device, the capacitor in this case in hours. So, we saw how you could make use of the expression, that you have linking the core temperature to life of the capacitor. So, based on such an expression you could evaluate the number of hours at 40 degrees, the minimum life would at the hottest temperature, so it is going to just 1.41 into 10 to the power of 4, at 80 degrees where as when it at 40 degrees, it is 3.54 into 10 to the power of 5, then you could look at then what is the damage under each of these durations.

So, for your duration D i is essentially 8 hours, 3 hours, 11 and 2 hours under these different conditions, So, your D by D f which is the life of. Under each of this condition would be your normalized damage corresponding to 1 day over all period.

So, you have 2.26 into the 10 to the power of 5, which is essentially 8 divided by 3.54 into the 10 to the power of 5. Similarly, the other entries in this particular last column. Then you could accumulate the damage occurring over the entire duration and that is 9.34 into 10 to the power of minus 4, then you could look at what is a normalized, this is the normalized damage that is happening on a daily bases. And then you could look at what would be a number of days for this normalized damage to reach a value of 1.

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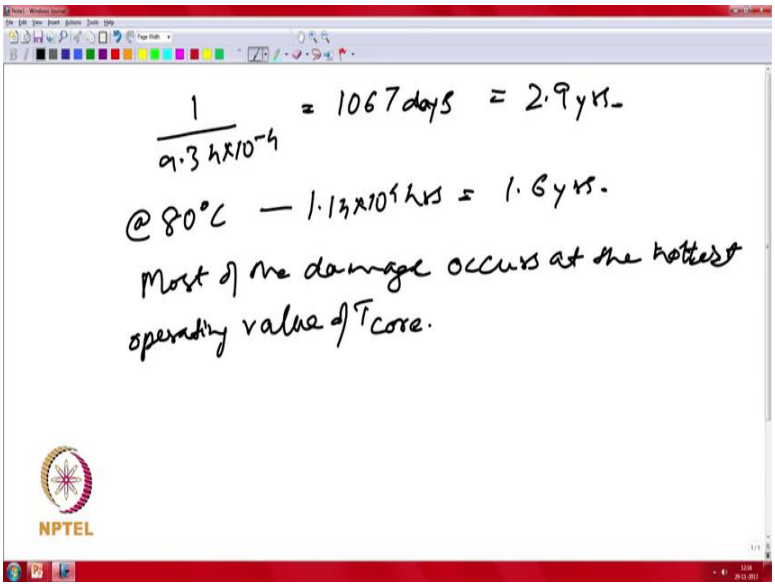

So, this would be 1 day divided by 9.34 into 10 to the power of minus 4. So, this is 1067 days, this is 2.9 years. So, if you look at the table, if you look at the number of hours at 80 degree centigrade, that corresponds to 1.4 into 10 to the power of 4 hours. So, if you look at 1.4 into 10 to the power of 4 hours, this corresponds to 1.6 years, and that is just 11 hours a day.

So, if you multiply that by the percentage of time that is getting operated, you can see that most of the life time is getting consumed that the hottest temperature, which is what one would expect in such operation of the equipment.

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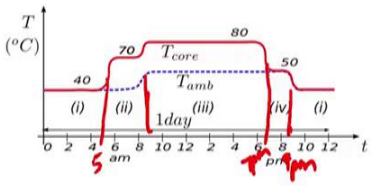
Damage Accumulation Analysis for Other Components



	T_{core} (°C)	Duration (hrs/day)	Life (hrs)	D_i/D_f
(i)	40	8	3.54×10^5	2.26×10^{-5}
(ii)	70	3	2.8×10^4	1.07×10^{-4}
(iii)	80	11	1.41×10^4	7.8×10^{-4}
(iv)	50	2	1.13×10^5	1.77×10^{-5}
Total normalized damage per day				9.37×10^{-4}

= 8/3.54x10^5

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Number of days for normalized damage to =1

So, we can see that what we have seen so far is that between say for example, you have in a power converter, between your device.

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Design of Power Converter Components

- Trade-off between component cost and power loss
- Thermal analysis for design reliability evaluation

EIC

- Design based on effective initial cost include factors for cost, efficiency and reliability

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And your cause that is actually a trade of say for example, if you want to reduce the power loss in semiconductor device, you could use higher current rated say device which would typically have a lower R on, the on state resistance would actually be lower. So, as to reduce your power loss in the device, but then you would have to pay more money for essentially the higher cost of the higher current rated device. The other thing we saw in

our example of a capacitor selection, we could actually reduce your power loss in the capacitor bank at least initially by adding more capacitors in parallel, when you are looking at the loss in the ESR.

But adding more capacitors would involve more cost. So, there is actually a trade of between the cost and the power loss, and we also, I have now seen that there is actually trade of between the thermal analysis for a liability and essentially the power loss, which is actually a function of the cost of the component.

So, the reliability power loss and cost is actually trade of that you can actually apply in the design of the power converter, and we have seen in our analysis of effective initial cost that, we could actually. Now include factors of cost efficiency and reliability in fairly straight forward manner to come up with something, which balances between the cost of the component, the power loss over its operation, and what is the reliability that you could actually expects for the component. It is also possible to in cooperate factors, such as weights, size, power density in such effective initial cost calculation, and do a overall analysis such that your design is actually cost effective design.

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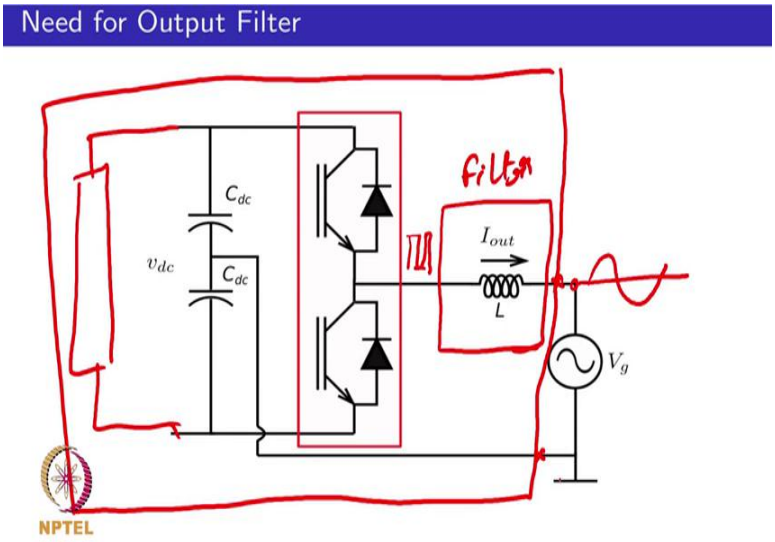

So, at this point we can, we have seen that in a power converter we have taken look at two of the components, one is essentially your DC bus capacitor, and the power semiconductor device the switch, the transistor, and the diode. The next major component in the power converter is essentially the output filter and will take a closer

look at how one could go about the design of the output filter, and if you, if you look at the filter, it is typically inductive filter. And we have seen in analysis that in power converter you would like to switch between a voltage source and a current source. In the power converter, that the DC bus capacitor bank is actually emulating a voltage source.

So, it is trying to keep the voltage constant and stiff on the DC side. On the other side you would expect a current source and essentially the inductor plays the role of the current source. We know that the inductor does not want to change the current level, current flowing through it on a instantaneous basis. So, essentially inductor can actually be used to emulate a current source.

If you are also looking at the analysis that we have done for the current, that is flowing through the DC bus capacitor etcetera. We assumed that the current flowing out of the i out is actually a pure sinusoidal current, but we know practically it is not exactly going to be sinusoidal, it is going to have ripple on it, there will be some variation above the nominal sinusoidal shape. Ideally if you want to have a ideal current source, the inductance would end up being very large, practical designs would need finite values the, of the inductance, which is actually quite small and that would now add constraints on how large you can make the inductor or how small you would like to keep it in terms of the design.

So, the first thing that one need to keep in mind is, why have a filter at all? One thing that you have is your grid is actually a sinusoidal voltage coming at the ((Refer Time: 30:40)) and we know that the output of the power converter essentially has pulsed wave forms. If you just directly connect it, essentially the current would not resemble in anything to a sinusoid, so it might have very large spurned spikes which would not even work your inverter would not be functional.

So, you definitely need a filter in a practical power converter. And to see why one needs a filter and what is the level of filtering that is required, we have to look at, what are the relevant relations on connecting a DG to the grid, and the standards that are associated with it.

If you look at the previous case, if you are having DG system, say a solar system, solar panel and a inverter. The panel and the inverter would essentially be within something that is being provided by the equipment manufacturer. The point at which it gets

connected to the external word is at the AC terminal. So, what happens within the box is up to the designer, but what comes out of the box can actually be regulated because that effects the customer that effects the all the people. So, you have regulations on how you can actually connect DG equipment out into the grid.

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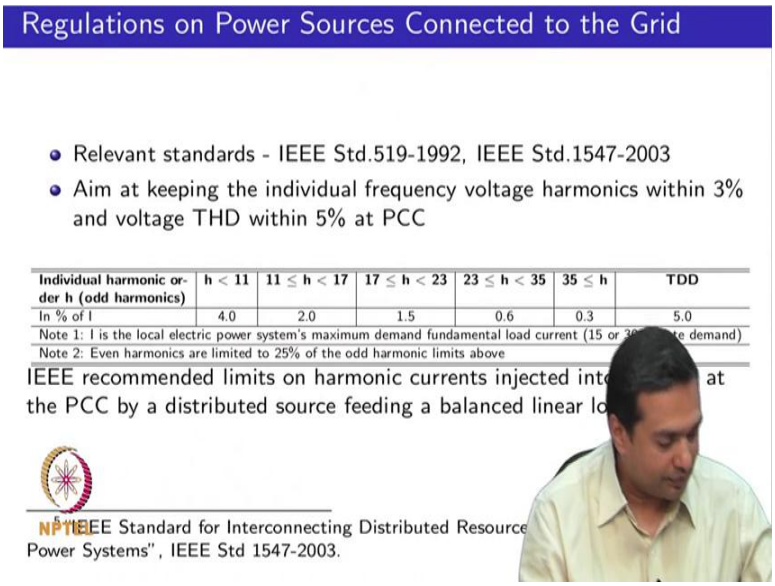

And two of the relevant standards are IEEE 519 and IEEE 1547, IEEE 519 is a about harmonics in power systems and 1547 is about connecting distributed resources with the electric power systems. And the objective of the standards, is to ensure high power quality. So, when you are talking about higher power quality, there are couple of ways of looking at it.

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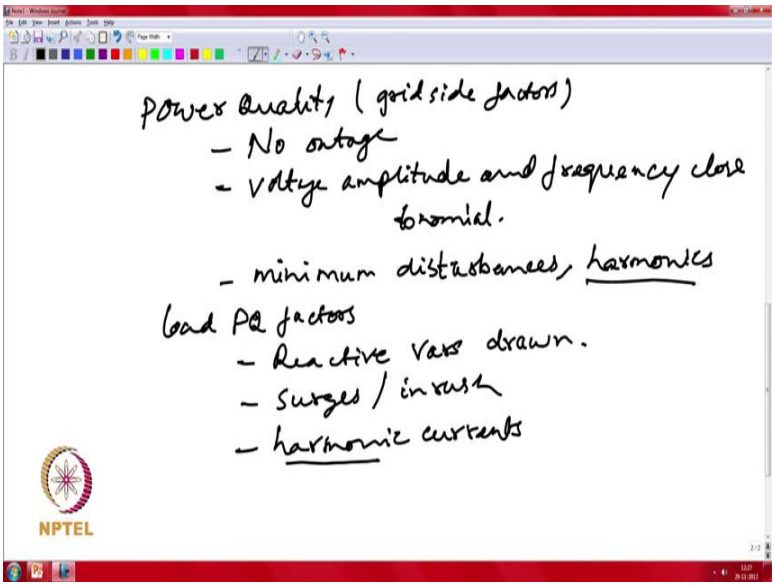

So, you can have power quality in terms of the grid is when you are talking about the grid, we are looking at know outage, we want voltage amplitude and frequency is close to nominal, and you can have small ranges around it, and you want it to be sinusoidal which means that you do not have distortions, you do not have harmonics, you can also have power quality. So, these are grid factors, we can also have load side factors of over the power quality. So, one thing you might want is to ensure that you are not drawing very high reactive watts.

So, you might not want very large surges to be consumed by the load, and you do not want to have in rushes. So, those might be some concerns that you have. You have another factor, you do not want your load to be drawing harmonic currents. And of course, another factor which would be overall requirement would be that, you are not causing EMI problems because of your load, that is being connected. And if you look at your, the IEEE 519 and 1547 and the filtering requirement, we are actually addressing the harmonic issues from the point of your actually both the load and the grid.

Because if a load is drawing distorted power, and we know that the grid has finite impedances, it has finite x by r ratios. So, the harmonic current drawn by a particular load would interact with the impedance to cause harmonic voltages, which would be exposed to other customers which are connected to the same line.

So, you need to ensure that your currents are within a range, such that one particular user will not be able to cause power quality problems to the neighbor.

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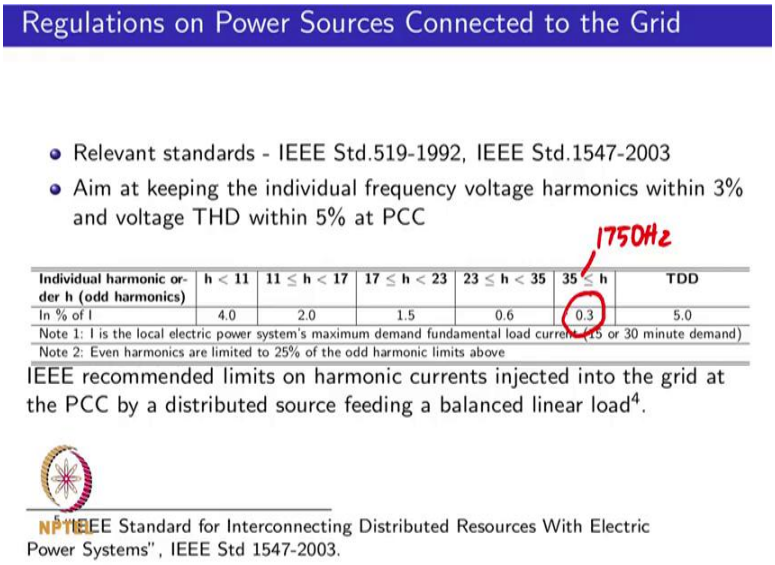

And the level of the harmonic currents that are drawn depends on how stiff the grid is for example, if this if the grid is extremely stiff, you can draw a lot of harmonic current and distort, not to distort the voltage.

So, your allowance for harmonic currents can actually be quite high whereas, if you have a grid which is quite weak, which means that it is short circuit ratio is quite small, then even a small amount of harmonic current can actually cause a large grid voltage distortion. And when you are designing a power converter equipment, you do not know whether it is going on a stiff grid or on a weak grid.

So, you have to design it for the worst case condition, which is the weak grid. And what is shown over here is the regulations for the harmonics, the objective of the overall system is to ensure that, the voltage harmonic distortion at the point of common coupling PCC stands for point of common coupling, and the voltage total harmonic distortion is less than 5 percent and your individual harmonic amplitudes do not exceed 3 percent in the voltage. And the corresponding harmonic currents that can be drawn by the load, would then depend on what is the harmonic number and the overall objective is actually to keep your total demand distortion.

You look at the definition of what PCC is THD, TDD, etcetera is, you want to keep your total demand distortion to be a less than 5 percent. And depending on what is the harmonic number, you have different levels of allowed currents that can actually be able to injected by your DG system.

So, if you look at the highest harmonic which is given in the standard, which correspond to the 100 and the 35 th harmonic, this would correspond to about 1750 hertz, for a 50 hertz system. So, what is being asked is when you are having harmonics at this particular frequency or higher, you can inject less than 0.3 percent of your current demand at the PCC as the harmonic currents.

Often, in a power converter your switching frequencies would be 2 kilo hertz or higher which means that you need to attenuate your harmonic distortion to less than 3 percent by your filtering action. So, this is actually a important number which comes up when you are looking at filter designs for DG systems.

Another thing to keep in mind is when you are looking at the demand distortion, you are looking at what is the demand over some time frame. Another thing is that if your harmonic is a even harmonic, it is one-fourth of what is given in this particular table, even harmonics cause a loss of half a way symmetry, so you would like to actually keep it to a smaller extent.

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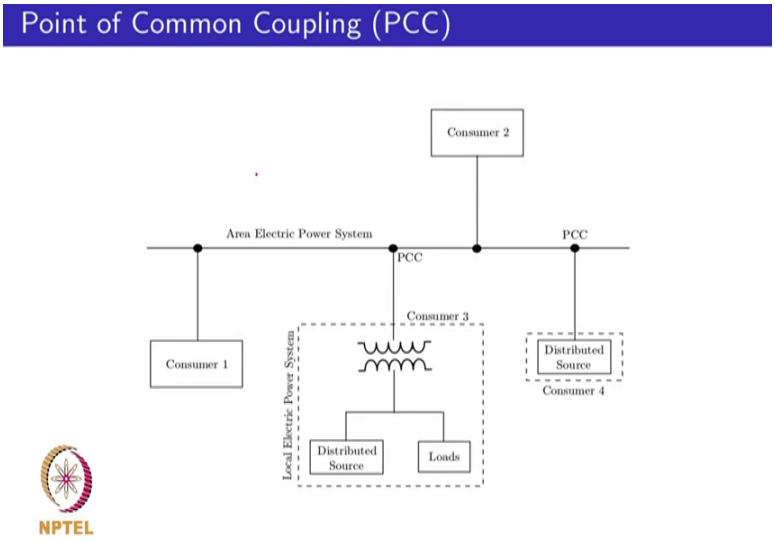

So, the first thing is to look at what the concept of a point of common coupling is. If you look at your typical household scenario, the point of common coupling is the place where the public service stops and where your private consumption starts. This would be in a house, the power meter might be considered as a equipment belonging to the distribution company whereas, the circuit breaker which is downstream of the power meter is equipment that belongs to the owner of the particular enterprise.

So, you are not allowed to tamper with the power meter and the distribution company would expect you to ensure that whatever is connected downstream of that to be protected by the owner at the owners expense. So, the point of PCC, you can think of a analogy between the electrical system, and say your physical, say home and the road that come to your home.

So, interface between your home and the road would be your gate. So, beyond the gate is the public road, inside the gate is your private home and essentially the objective is in that particular case is might be, you might have, you might be coming in and out of your house, but you might also be generating some garbage in your house, which you have to dispose off. So, you can think of harmonics as pollution, which you do not want ideally it should be 0.

But you know that if you want to have a complete garbage disposal facility in each and every house, it might be too expensive. So, you are allowed to dispose of some amount of garbage, but if it is too large, instead of maybe a bucket full of garbage, you are disposing a truck full of a garbage, that is not acceptable, but whether the garbage is being generated by your elder brother or whether it is someone else in your family does not matter, the total should not be too large.

So, that is essentially what is being at the PCC, and the concern is if you too much garbage, your neighbors would not like it, you might cause health problems in the neighborhoods. So, you want to ensure that the power the quality of life overall is good. So, essentially you can think about harmonics in power systems as a societal requirement is important that you meet the standards that ensure that the power system operates in a clean manner.

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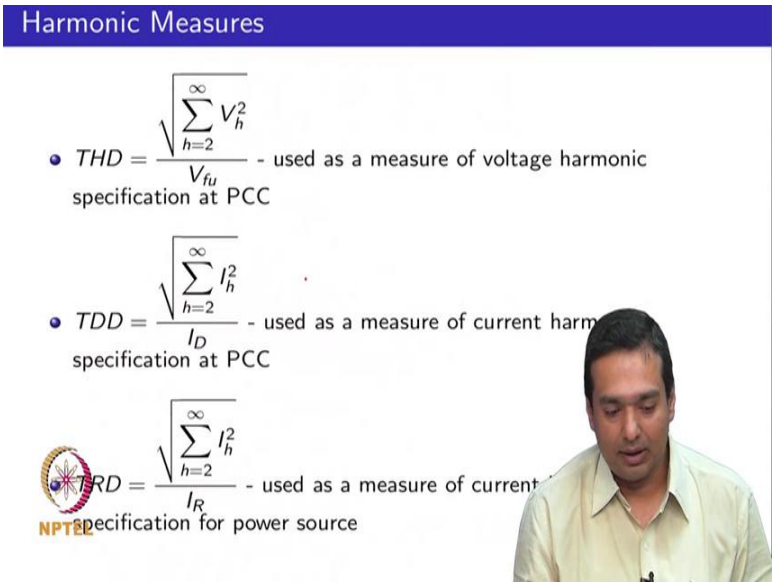

So, we the other concept that we had mentioned is about THD, THD is essentially the ratio of your RMS of your harmonic components, from the second to the largest value that you would have or could consider in your particular application divided by the RMS of your fundamental. And commonly in the IEEE finite in context, we will look at the voltage specification of the PCC in terms of VTHD, because the VTHD at the PCC is going to be similar, same as the VTHD with order loads within that particular facility because your IR drops in the conductors within your particular establishments is not going to be very large. So, irrespective of whether it is a load the PCC, you would see similar levels of THD in your system whereas, that is not the case of your current.

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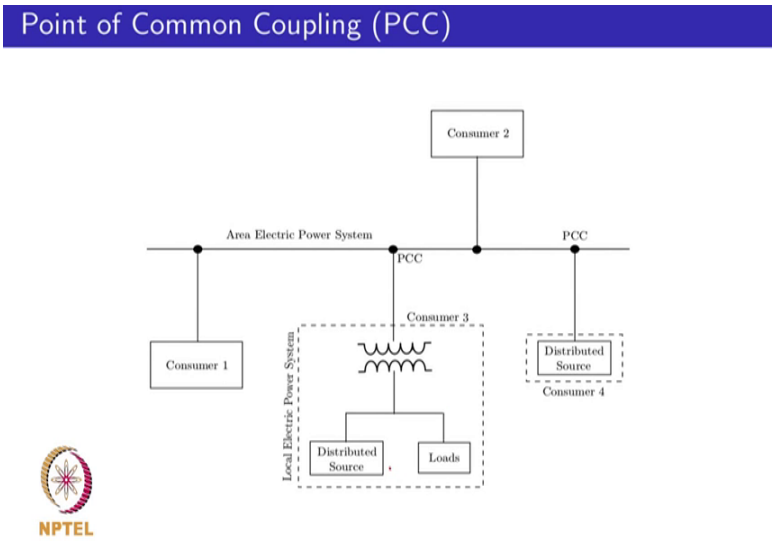

Say for example, you might have a current, which is a highly distorted from one equipment, but your current drawn by other equipment might be clean and sinusoidal. So, when you are looking at the PCC, overall you might not have much distortion just because you have other loads within the particular facility.

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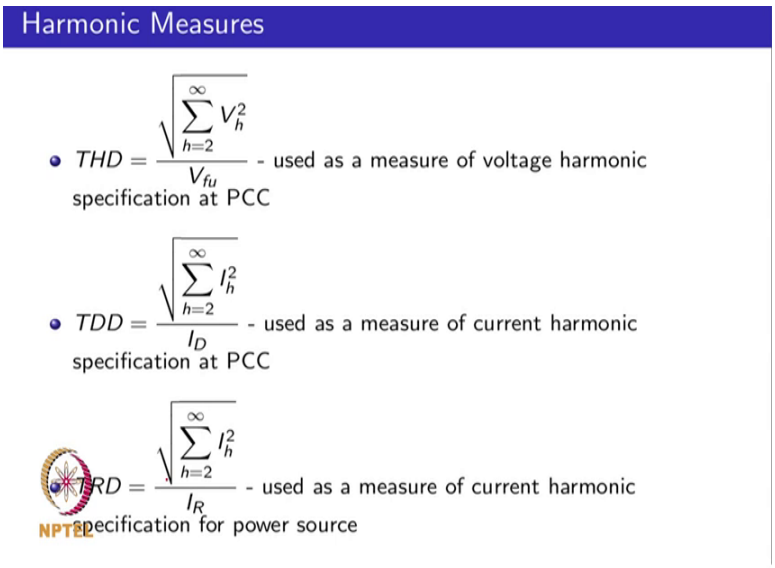

So, what is being asked is that the overall demand, based on the demands seen at the PCC, your value of the distortion, the ratio of your current harmonics from the second to the highest that is being considered divided by the RMS value of your demand is not

exceeding a value, and the demand might be considered over a 15 minute or a half an hour duration, and you want to ensure that it meets the particular standard.

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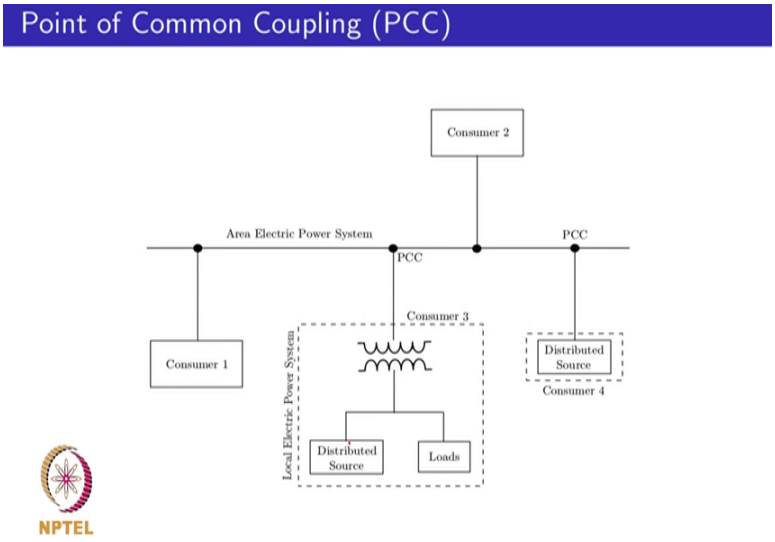

In a DG application, it may not just be, your actual demand might actually go up and down depending on what other loads are there in the system. A worst case might be to consider your DG source as the only source, in which case you are looking at, what is the distortion divided by what is the fundamental being output from a DG source and because one might be interested in what is the maximum operating point of this particular equipment, you might also be looking at what is the rating, rated conditions under which such a system might operate.

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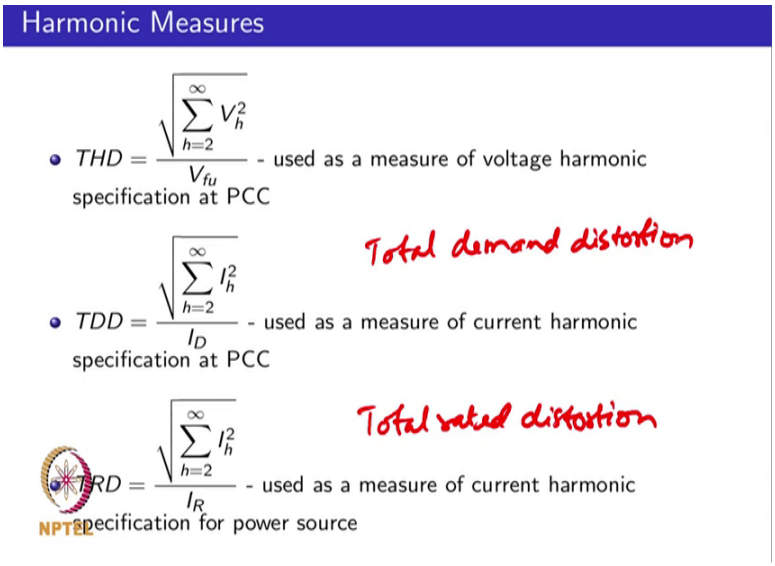

And that is where you have your TRD, your total rated distortion. Rather than looking at the demanded, the demand distortion over 15 minute or 30 minute intervals. So, what we have done is so far, we have looked at the AC side current to be a smooth sinusoidal.

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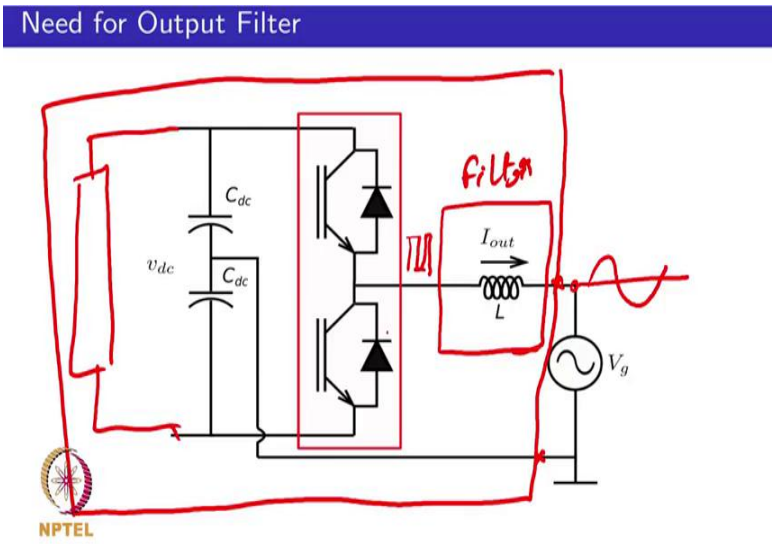

So, the next thing that we could do is maybe look at what would be ripple, that would be coming out of say a power converter connected to the grid with a DC bus voltage and the grid side voltage, in case of a simple topology such as the single phase central tap

topology. So, for that what we will look at is, look at the modulating wave form and look at what is a ripple current, depending on what the duty cycle is.

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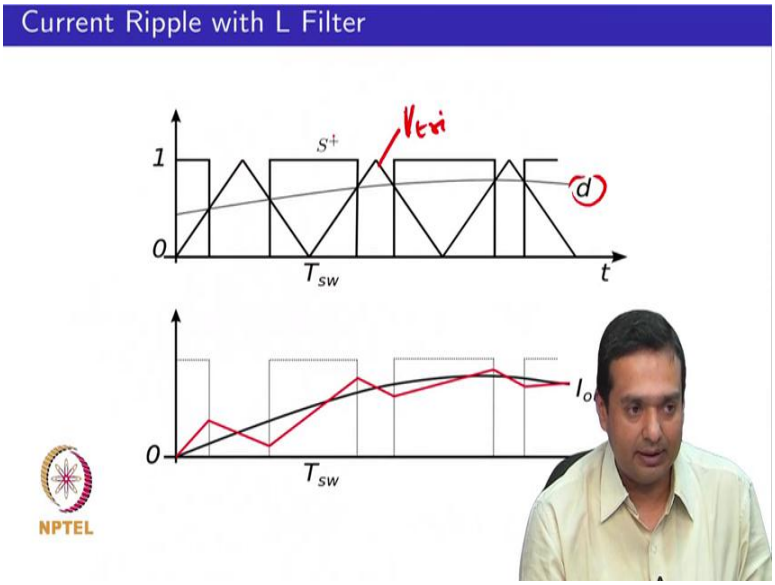

So, if you look at your actual current your modulation signal, that is being provided to the switch, that is shown as d over here and your, you have your triangle, triangles which is your carrier and to compare your d modulation, your duty cycle command with your carrier to actually look at what your modulation signals to the gates are. So, when S plus is on your top switch is on, you are applying plus V dc by 2 across at the output of your converter leg and on the grid side you have V grid, one thing that we will assume is that grid voltage is close to your output voltage of your leg.

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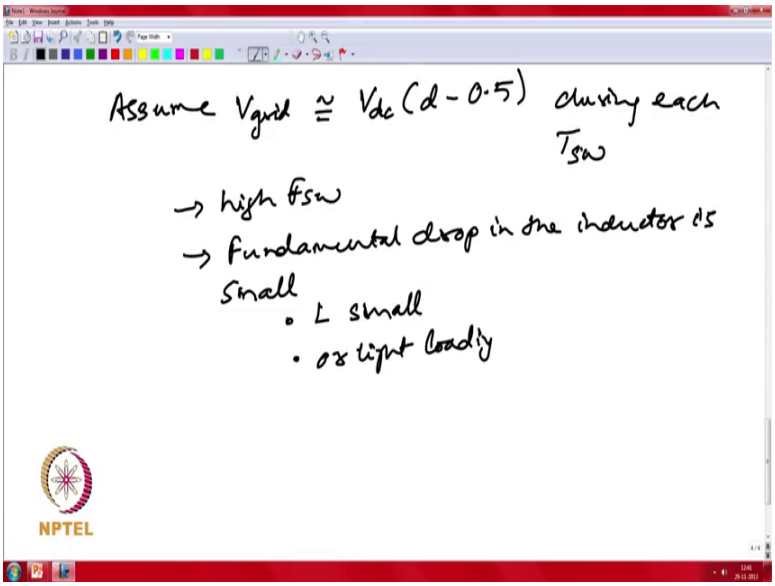

So, we will assume, if your, another thing that we would assume is that your duty cycle is not changing much, so it is whatever you are commanding is close to being constant over a duty cycle. So, you are assuming that your switching frequency is high, you are also assuming if your grid voltage is close to the voltage that you are commanding, it means that the voltage drop across the filter inductor is quite small.

So, this would be a, the fundamental voltage drop and the inductor would be small if L is small, if the filter inductor itself is small, or if your loading condition of your power converter is light, or it could be a condition of both. So, we could write an expression then for what is the current that is flowing through the filter inductor during your on duration and off duration.

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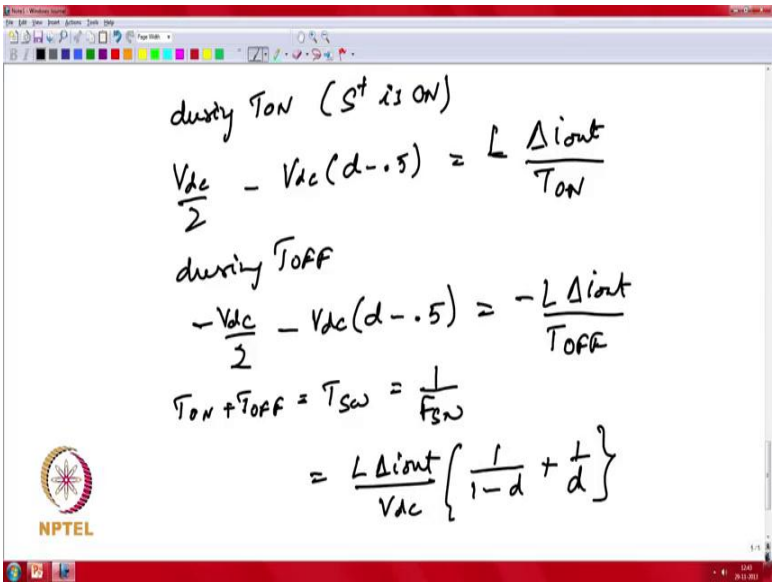

So, during T on essentially your S plus is on, we have V dc by 2 minus your grid voltage, which is taken as V dc into d minus 0.5 is L into delta i out, change in the value of your output current divided by T on. Similarly, during the off duration, we have minus V dc by 2, being applied at the output and your grid voltage is, and the ripple is now going down, so you have L minus delta i out by T off. Also we know that T on by T off is your switching duration, which is essentially reciprocal of your switching frequency. So, you can write an expression for T on plus T off in terms of these two, expressions over here you have 1 by F sw to be equal to L delta i out by V dc. So, you could then write an expression for what your current ripple is.

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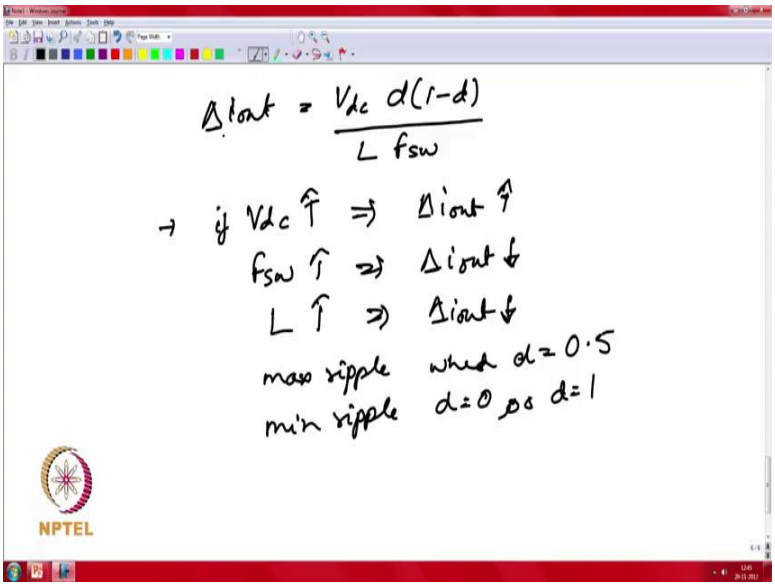

You have delta i out is V dc into d into 1 minus d. So, one can see from this expression that you have, if you have a higher V dc, one is if V dc is high, then essentially your delta i out could be high. So, you do not want to keep your DC bus voltage to be too high for multiple reasons, one is you do not want to stress out your components, other thing is you want to keep your rippled to be not too large.

If your F sw is high, then your ripple would come down, but with a higher switching frequency, you end up with higher frequency losses in your semiconductor components. The third thing would be if your value of inductance is high, then your delta i out would be low, which is natural to expect. The other thing to see is that if you look at this particular expression, it is d into 1 minus d, you can look at when you have minimum or maximum conditions of your ripple, you will get a maximum ripple. For this single phase inverter, it occurs when d is equal to 0.5.

So, essentially this is when your output voltage is 0 you will end up with higher ripple, you are going to have minimum ripple, when d is equal to 0 or 1. So, when d is equal to 0 or 1, this turns out to be 0. So, you will not have ripple. So, under the close to the peak or value of your voltage reference, we will end up with smaller ripple in the single phase power inverter. We will look at some of the constrains, when you look at your selection of the inverter.

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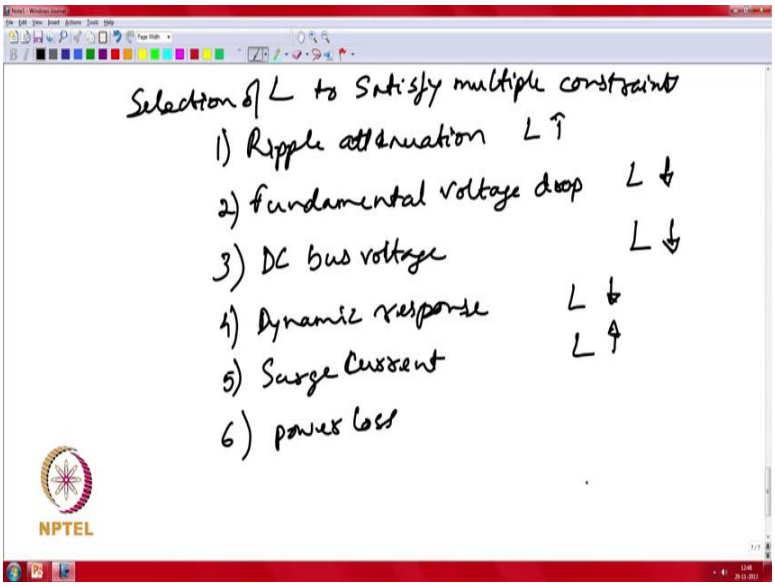

The selection of the inverter selection of the L. So, one thing you would like to do is, you want to attenuate it to selection of L to satisfy, one is ripple attenuation for which you need L to be large. You would also like to keep your fundamental voltage drop across the filter low for which you would like to keep your inductance low to keep the DC bus voltage low, you would like your inductance again to be low.

If you look at it from a dynamic response prospective, you would like a larger inductor has more. you can think of it as having more inertia, so you like to keep your value of your inductance low from your dynamic response prospective whereas, if you are looking at it from search transient. So, you turn on the converter and you want to limit your search current, you would like then have a higher impedance, so you would like your inductance to be high.

If you look at the power loss, it has to be, if it is too low then the ripple current would cause lot of losses, if it is too high your fundamental current loss would be too high. You are looking at some optimum value of L, which is lying in between. So, you have multiple constrains that come up when you are looking at selection of the inductor. So, we will look at starting point of how you could start with a design of a simple inductive filter in the next class.