

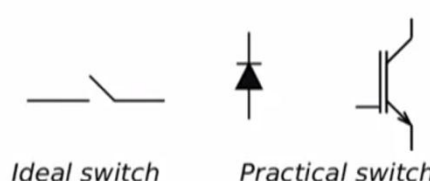
**Power Electronics and Distributed Generation**  
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**Module - 03**  
**Lecture - 31**  
**Switch Selection in Two Level Voltage Source Inverters**  
**and Loss Evaluation**

Welcome to class 31 on topics in power electronics and distributed generation. In the last class, we have been looking... previously, we have been looking at the selection of DC bus capacitors in an inverter. So, today we will look at selection of the power semiconductor devices in an inverter.


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**Switches in Power Converters**



*Ideal switch*      *Practical switch*

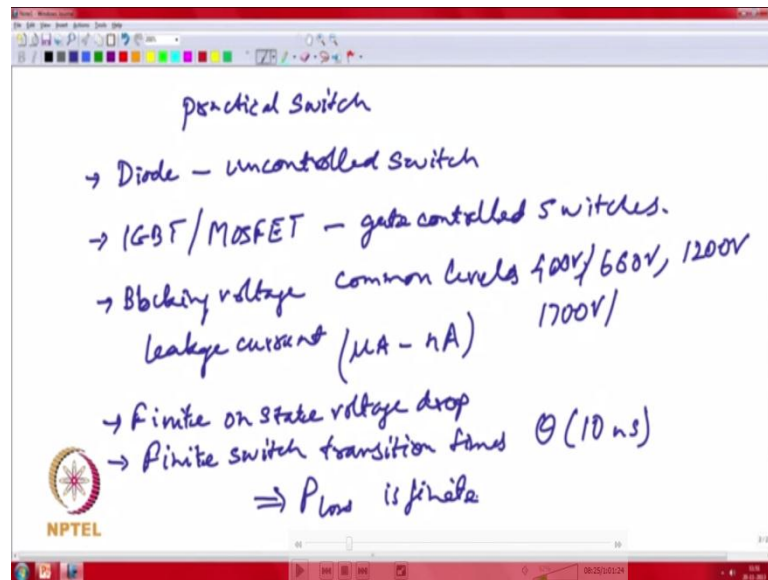
- Voltage and current ratings
- Switch transition times
- Power loss in the switch

  
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So, if you look at the what we had been studying so far in our switching models, we have been considering an ideal switch. If you look at an ideal switch, an ideal switch, ideal switch will block infinite voltage in and it will not have any leakage current when it is blocking the voltage. The ideal switch can actually carry an infinite amount of current without having a substantial on-state drop. So, there is no on-state drop in the ideal switch whereas, in a practical switch you are going to have a finite voltage drop and there will be a conduction losses because of the on-state drop in the semiconductor device.

If you look at the switching transition times in the ideal switch we are considering it going from on to off and off to on, on an instantaneous basis in the ideal switch. Whereas, in a practical switch you have finite transition times between your on-state and the off-state, so if you look at a practical switch.

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So, practical switches are the most basic as a diode you have thyristor you have mosfets IGBT's GTU's etcetera. For many applications in the distributed generation range, we could consider the power levels of a few Hun few tens to hundred of watts to a few tens to hundreds of kilo watts. You have commonly devices such as diodes IGBT's mosfets etcetera.

So, we will consider IGBT in a diode as a standard practical switch, when we look at the semi conductor device. So, if you look at a diode, it is an uncontrolled switch. So, when the external voltage from anode to cathode is positive, it would conduct current when we reverse the voltage. If you apply a negative voltage across the terminals it would block conduction, it would not conduct current.

If you look at a controlled switch you have an IGBT or a diode. IGBT stands for Insulated Gilt Bipolar Transistor or you have a mosfet metal oxide a field effect transistor, these are gate controlled devices. So, depending on the voltage that you externally apply at the gate, you can control the switch to be in an on-state or in an off-state.

If you look at the breakdown voltage of these devices, you have a finite breakdown voltage we are looking at examples where we have DC bus of the order of 600 to 800 volts or 400 volts. So, you might have common semiconductor blocking voltages, or 600 volts rated semiconductors or 1200 or 1700 volts rated semiconductors. These are common blocking voltages.

You have 400 volts, you also have medium voltage GVT, which convert to 3.3 KV 6.6 KV etcetera, but commonly for DG applications you would be using a IGBT's that can be used in a low voltage applications. And you are looking at the leakage current. The leakage current is actually a function of temperature, you heat a semiconductor device, the leakage current typically would increase. You are talking of currents in the range of macro amps to nano amps depending on the rated current of the semiconductor.

So, a higher rated current semiconductor would have higher leakage current compared to one at the lower rated current. Because physically the cross-section area of the ((Refer Time: 06:11)) would be lesser for a lower rated current device and it is also dependent on temperature. If you look at the finite on-state voltage drop. So, we are talking about 1 to 1.5 volts or typically for diodes, you are talking about again 1.5 volts to 2 volts for IGBT's.

So, for mosfets, depending on your on-state resistance you might have voltages in the range of the order of 1 volt, depending on the current level and the on-state resistance. If you look at your switching transition times, today switches are able to turn on and turn off in the range of tens of nano seconds. So, of the order of tens of nano seconds. So, again depending on the rating of the device a larger rating device might be slower. You have a finite switch transition times so you are able to switch at tens to even hundreds of kilo hertz with the semiconductor devices that are available to be.

So, if you compare an ideal switch because you had no leakage current no zero on-state drop, you had zero switch in time the switching. The power loss in this the ideal switch is zero. Whereas, because of all these reasons in the practical switch, you would have finite power loss. So, the implication of all these factors is p loss in the same conductor is finite and that has important implications on how you operate the power converter. So, if you look at the on-state loss this is commonly referred to as the conduction loss.


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**Loss Model for Switches**

- ON state power loss *Conduction Loss*
- OFF state power loss *due to leakage current (neglected for low voltage)*
- Loss during transition from OFF to ON
- Loss during transition from ON to OFF

*Switching Loss*

Accurate power loss in the semiconductors is used to evaluate maximum junction temperature of the semiconductor switch.



And depending on the on-state voltage and the current that is being carried by the semiconductor, you would have participation in the device which can be a significant factor, especially if you look at the overall loss in a device. So, ideally you would like to have a device with low on-state voltage to actually minimize conduction loss. If you look at the off-state power loss this corresponds due to leakage current.

So, in the conduction loss if you have a on-state voltage drop of the order of 1 volt, and if you are carrying currents of the order of 10 amps 100 amps etcetera. You are talking about an order of tens of watts of participation in the case of leakage current you are talking about off-state voltages of the order of 800 volts may be 1000 volts, and if you are talking about micro amps or a of leakage current or nano amps, so you are talking about participations of milli volts.

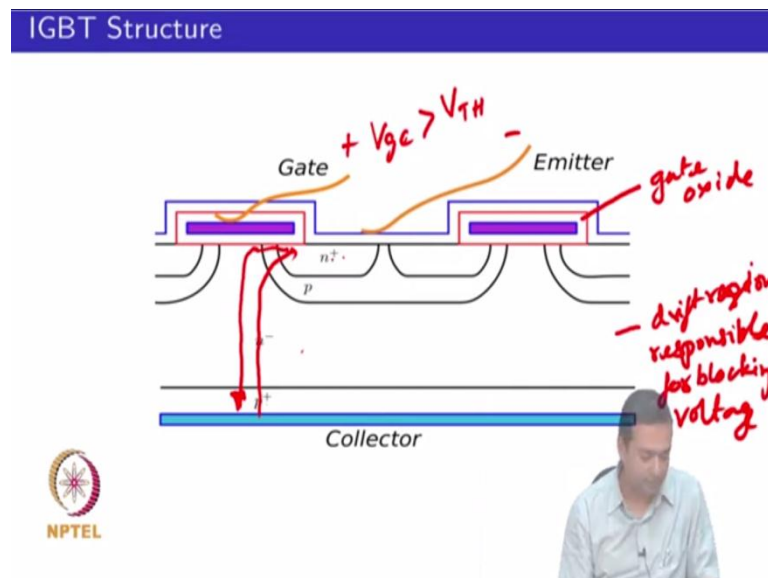
So, compared to the conduction drop, the off-state per loss may be neglected especially when you are looking at low voltage applications. And typically when you are referring to low voltage in from a power systems prospective, you are talking about voltage is less than 1000 volts.

If you look at your switching loss you have switching transition from off to on turn on and on to off. So, this would correspond to the switching loss, and because of the finite loss that occurs in a device at each switching event. If you now operate a higher switching frequency, your switching loss will scale with your switching frequency. So,

one limitation of how fast you could switch a device, is that your power loss due to the switching loss factor would increase to such an extent, which might limit how fast you can switch a device.

And you could say what is the final a big concern for doing a detailed valuation of a power loss in a semiconductor device in a power converter. The primary implication is to ensure that your maximum temperature within your semiconductor does not exceed critical values, and to ensure that your semiconductor devices stay cool during the operation of your power converter. And your overall losses have to sum through all these factors to when you are actually evaluating your overall loss to look at your junction temperatures.

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So, if you look at an example of a structure of a semiconductor device. So, here what is shown is a schematic of cross-section of an IGBT semiconductor chip. This is actually a vertical double diffuse because you have diffusion for n plus and p layers within the semiconductor. You have the n plus would be connected to the emitter, so you have metallization which is shown on the upper blue curve, and what is shown within the red curve is the gate oxide. So, the gate metallization is what is shown in the magenta color. So, you have connections to the gate out within the gate oxide you have the gate.

So, you have the aluminum which is used as a gate connection to the IGBT. So, you could apply a gate voltage with respect to the emitter. If you look at the region where the

gate is located, it is located between the emitter and the n minus region. So, you have a channel that can be where you can use charges by applying appropriate voltage. For example, if you apply positive voltage between the gate and the emitter, you get positive charges in the gate metallization, which would induce negative charges just below in the p region of the semiconductor.

So, this n minus region is called a drift region, which is primarily responsible for the blocking voltage. So, if you need a larger blocking voltage the drift region would be wider, and the junction which actually blocks the voltage is this particular p n junction. So, if you apply a positive voltage at the collector you do not have gate voltage. So, you apply positive to the n minus region and negative to the p, so it is a reversed bias junction. So, you have depletion regions that are formed across this n minus p region, because this is likely doped the depletion x region extends well down into the structure

So, essentially this particular dimension and the doping level of this region determines what the rated voltage, the breakdown voltage of the devices. The p plus region at the bottom is what is connected to the collector of the device, so the collect if you when you are passing current, positive current from your collector to the emitter, it essentially flows from the p plus to the n plus in and out through the emitter.

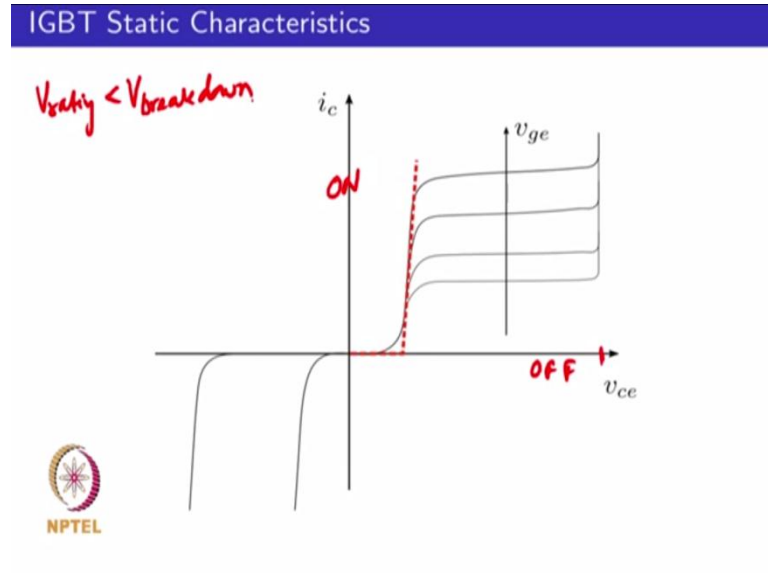
So, if you apply a voltage, if you apply a positive voltage  $V_{ge}$ , it means your gate and the emitter essentially you will induce charges in this particular region and you can get essentially electrons to flow in this particular direction, and holds to flow back. You also have a p and p transistor over here, which would give you a enhancements in terms of the conductivity, the p n junction would inject a minority carriers into the n minus region to give you conductivity modulation which reduces the on-state voltage drop.

So, if  $V_{ge}$  is greater than the threshold voltage of the particular gate, gate oxide and the semiconductor, so if it is greater than the threshold voltage, essentially your device would start conducting current and if your gate voltage is below the threshold voltage, it would essentially block conduction.

If you, if you look at the structure of the IGBT, you have a PNP transistor, you also have a NPN transistor. In early IGBT's people used to worry about the problem of latching of IGBT's, because you have essentially a PNPN thyristor structure. If you look at IGBT's

that are available today this is no longer a problem. We have IGBT's with a rugged square safe operating area which can be used without problems of latching.

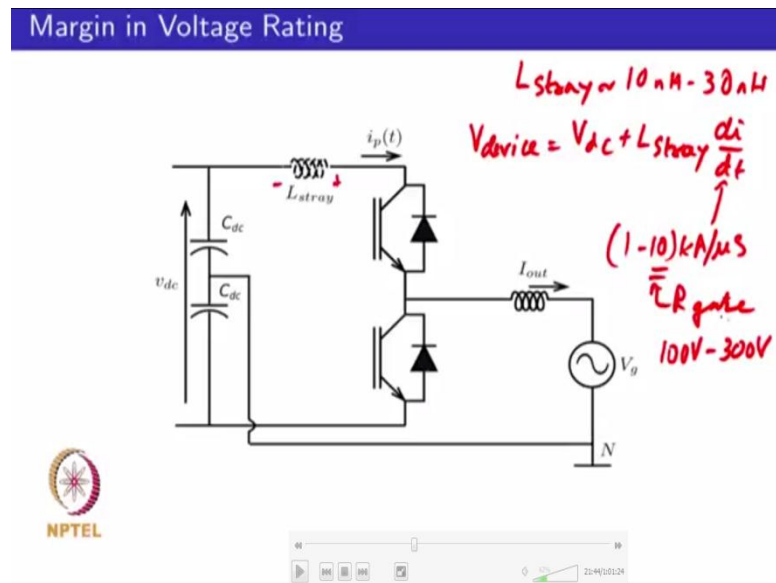
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If you look at the IGBT's the operating region in a power converter you are either going to be using it off-state. So, this would correspond to applying a voltage and blocking current or you will be using it in the on-state, so your switching between the on and off conditions. If you, if you look at so you are in the off-state as long as you ensure that your voltage does not exceed the breakdown voltage. If you, if your voltage exceeds the breakdown voltage then essentially you would have uncontrolled conduction.

So, your voltage rating is less than the breakdown of the junction. So, the breakdown of the junction depends on the geometry, the temperature of the of the your device etcetera. And for a 800 volts DC bus, we would commonly use a 1200 volt IGBT.

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So, if you look at why you need a the margin of 400 volts going from 800 to 1200 volt device, you can look at typical IGBT module. You would always have interconnection inductance. So, if you have a  $L_{stray}$  of the order of say 10 henries is to 30 nano henries. So, this you can get 30 nano henries even in few within less than 10 centimeters of interconnection. You have your actual device voltage, would be is  $V_{dc}$  plus  $L_{stray}$  into  $\frac{di}{dt}$ . So, for example, when you are switching off the device you will end up with a  $\frac{di}{dt}$  which applies a voltage across the  $L_{stray}$ .

So, if you look at your  $\frac{di}{dt}$  is that are of a present day switches, you are talking about 1 to 10 kilo amps per micro second. So, if you look at 10 kilo amps micro second, you will end up with a fair amount of voltage drop. So, voltage that is being applied across the device so whether it is 1 or whether it is 10, it is also a function of what type of gate resistances you would use if you use a smaller value of gate resistance is your  $\frac{di}{dt}$ 's can be larger if you use a large value of gate resistance your  $\frac{di}{dt}$ 's would be smaller, but then your switching losses would also increase.

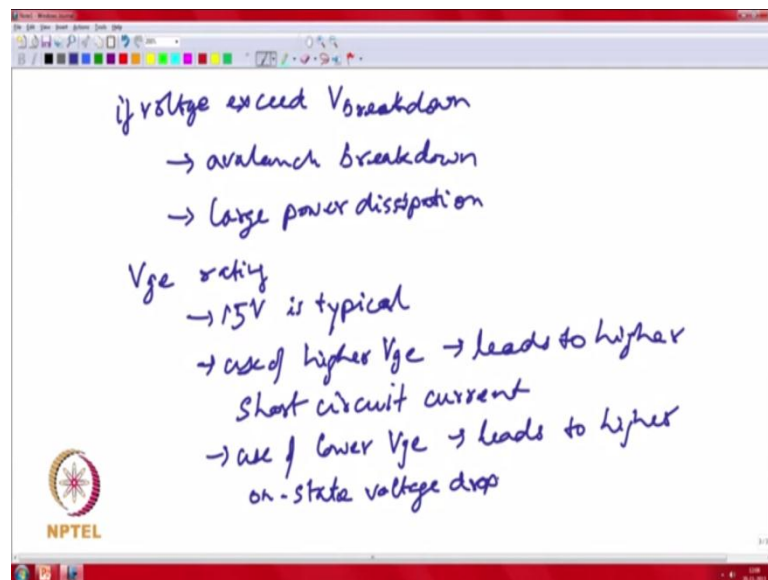
So, it depends on your  $R_{gate}$ . If you are then talking about say something like 10 kilo amps per micro second and say you are talking about  $L_{stray}$  of 10 nano henries, you are talking about 100 volts to 300 volts even with 30 nano henries you would get 300 volts drop across your stray inductance which can then apply a substantial voltage across your



semiconductor device. So, you defiantly need a margin above what is available under DC bus.

So, it is critical for a designer to ensure that the inductance of your loop, which includes your switching module is extremely small. So, people will look at parallel plate structures. If you are using capacitors, you need to ensure that you have a low ESL pass available in parallel to take up a fast switching transitions, even a physical module might have internal inductance of the order of 10 nano henries. So, to ensure that your devices stay safe without breaking down, you need to co-ordinate your gate resistance selection with tight geometric design of your DC bus. So, if your voltage exceeds your rated breakdown voltage.

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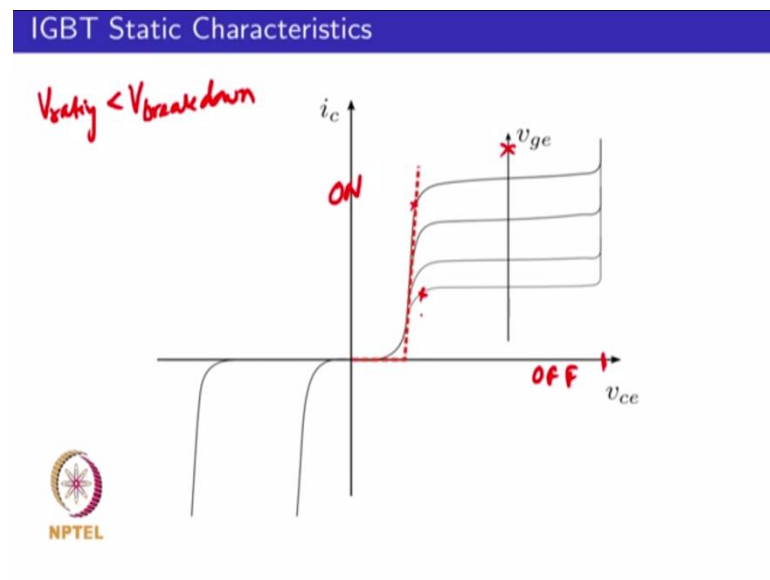


Then you have avalanche breakdown. So, essentially the electric field has become large enough, that between two collisions of the carriers it splits up sufficiently to actually generate additional carriers, so you lose control of the gate and you end up with a large amount of current that can actually flow through the device in an uncontrolled manner. So, implication is now you can end up with a large participation and eventually leading to device failure. So, it is important to ensure that you are always operating your semiconductor below it is rated voltage.

If you look at the other aspect of voltage rating. So, if you look at we have looked at the voltage that can be applied say from the collector to the emitter, the other voltage rating

is related to how much voltage you can apply between the gate and the emitter. So, if you typical voltages that are used at the gate emitter junction is of the order of 15 volts, 15 volts is a common voltage. If you apply excessive voltage you can actually damage the oxide.

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Also if you apply higher level of gate voltage essentially with increasing gate voltage your saturation current within your device is going up. So, at a higher voltage you will end up with higher saturation currents which is what would show in case there is a short circuit in the particular device, so your device can get rapidly damaged if you apply excessive gate voltage. If you apply gate voltage which is low instead of having a on-state voltage over here, you might end up with a on-state voltage over here. So, you might end up with a higher conduction losses if the gate voltage is low common, commonly used gate voltage is 15 volts.

So, 15 volts is a typical number, also if you apply a excessive  $V_{ge}$ , you can end up damaging a gate oxide which would then damage your device. And so, if you then look at what could be the next rating factor which people would typically consider is the current rating of the semiconductor.

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Current rating  
→ Indicative value

$$I_{\text{rated}} \times V_{\text{ce-on}} = (T_{j\text{max}} - T_{\text{case}}) R_{\theta jc}$$

$P_{\text{cond.}}$        $150^{\circ}/125^{\circ}$        $\text{Specified. } 25^{\circ}/70^{\circ}$

⇒ Switching action would lead to actual current level that is lower  
→ indicates capacity of leads/connectors/wire bonds.

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So, when you look at the current rating of the semiconductor, which is actually provided prominently in the data sheet. We need to remember that current rating is only a indicative number, it does not specify the actual application in which your semiconductor is going to be used.

So, if you look at what your current rating is, it is determined as a  $I_{\text{rated}}$  and your on-state voltage when your device is on  $V_{\text{ce-on}}$  and essentially the product of this is your conduction loss. The conduction loss power and essentially if you look at what your  $T_{j\text{max}}$  junction maximum temperature is, you might have semiconductors which are rated for 150 degrees some might be rated for 125 degrees. So, you look at your  $T_{j\text{max}}$  and you look at your  $T_{\text{case}}$  temperature which is specified.

So, people might specify your current rating at 25 degrees or 70 degrees or some particular indicated temperature. So, this is essentially at room temperature or some particular operating temperature times your thermal resistance of your device, your thermal resistance from junction to case, we will talk more about the junction temperature shortly.

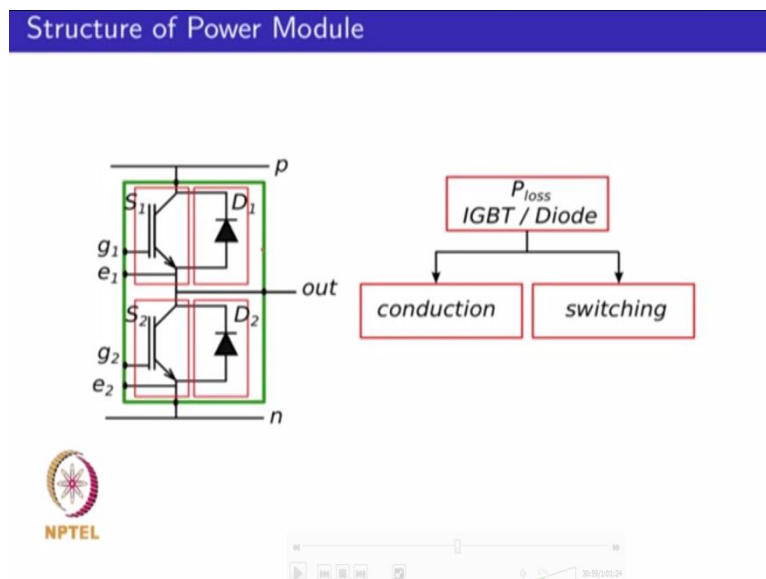
So, essentially if you look at your rated current, it is essentially having factors only of the conduction drop under specified measurement conditions. So, it is only a indicative number if you look at your actual operating current rating with your switching action and

the associated switching losses, your actual current capability of your semiconductor would be less than your rated current.

So, however you need to also keep in mind that the current rating is also indicative not just of the semiconductor, it is also indicative of the current carrying capability of your connectors, your terminals, your wire bonds, etcetera within your device. So, it is not just of the semiconductors, it is actually of your entire package. And if you operate above your current rating then it has to be for extremely short durations. For examples, when you have a short circuit, you if you operate for just a few less than 10 micro seconds you might be able to see your device, but if you continuously operate above the rated current, you can actually damage a sub-confidence within your semiconductor package.

So, the implications of operating above your current ratings, is that your devices would heat up, you can immediately see from this expression for how the rating is being defined, that is actually linked to your temperature.

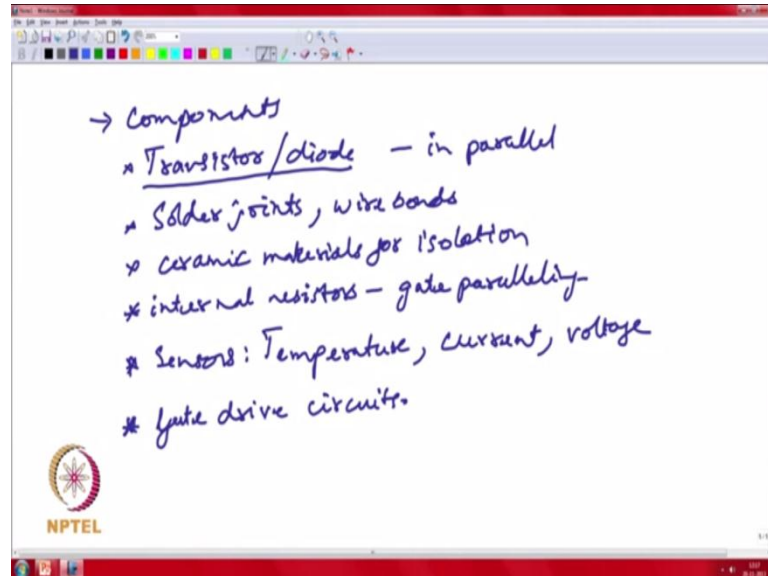
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So, if you look at typical power module, you would have what is shown in this green box, you would have multiple chips corresponding to switches diodes. Here what is shown is a leg you would have a switch for the upper switch in the leg and lower switch in the leg diodes D 1 and D 2. In turn if you have higher current rated modules each of these red squares might actually contain multiple chips which are operated in parallel. So, you might have dozens of semiconductor chips which are packaged within a

semiconductor module. So, if you look at the to evaluate the thermal rating of the semiconductor module one have to look at all your components.

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Your transistor, diode in parallel which maybe in parallel. If you would have a solder joints or bracing joints, wire bonds. You would have a ceramic materials for isolation, typically the chips are soldered onto a ceramic and the ceramic is then soldered onto a base plate and is the base plate which conducts heat out of the module. You have, you might have internal resistors, say you might have resistors for gate paralleling, you might have sensors especially if you have a newer modules come integrated with multiple functions people call them intelligent power modules might have sensors.

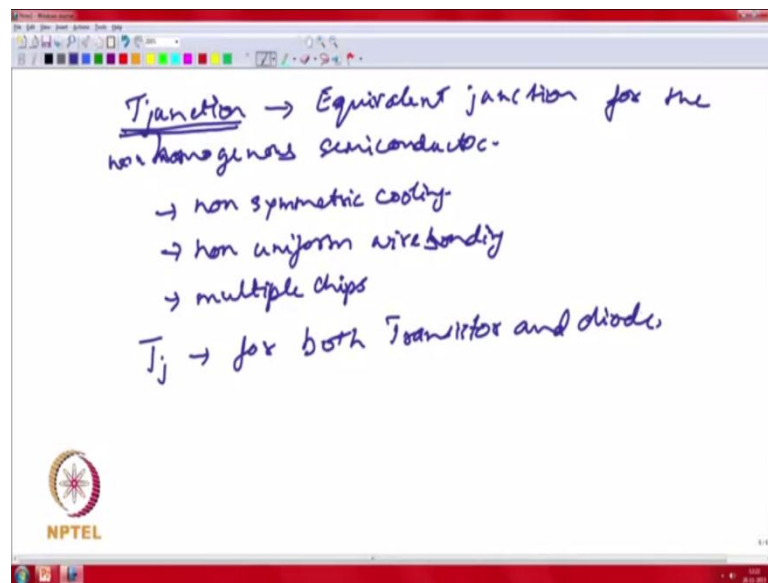
You might have temperature sensor, you might have current sensors, you might have Dc bus voltage sensing, also the IPM intelligent power modules, might also have integrated gate drive circuits. So, one has to look at the limitations of all the components within the particular package, and if you look at a critical aspect is to look at how much participation is happening in the transistor, and the diode which is actually carrying the largest level of power within the overall module structure.

So, again what is the issue of the higher temperature is that, at higher temperature your semiconductor the carriers, the carriers within the semiconductor becomes excessive and if once the excess carriers the value goes beyond what is there for your background

doping and the of your semiconductor then essentially the capability of your junctions to block goes away and you would have uncontrolled conduction.

So, typically if you look at the temperatures is at which your semiconductor material would have such large amount of excess carriers, would be of the order of say 300 to say 400 degree centigrade. If you look at the actual semiconductor chips there are highly homogenous, so people define essentially a virtual temperature which is what people commonly refer to junction temperature

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So, and you have number of non-homogenous you are talking about a non-symmetric cooling. So, the upper layers of the semiconductors would have lower cooling than the lower cooling levels of the semiconductor. If you look at the wire bonding connections to the semiconductors which is not uniform across the surface they are at discrete points. So, if you look at the actual chip, the edges might be at a much cooler than center of the chip, so you have connections for the gate which introduces non homogeneity in the participation across the chip you have multiple chips.

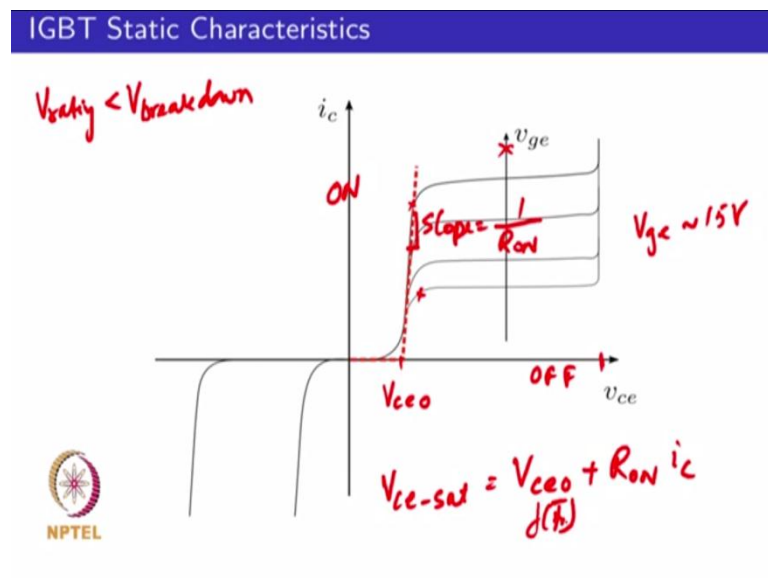
So, the chips that are at the edge would get better cooling than chips that are surrounded by any other chips which are themselves dissipating power. You also have passivation materials around the chip, which makes the participation within the chip are non uniform. So, when you are talking about temperature there is a significant difference

between your actual junction temperatures, to what people refer to as virtual junction temperature, which would one like to keep below 125 or 150 degree centigrade.

So, you can see that clearly you are have a factor of to factor of safety between your actual junction temperatures, which might which might actually be very difficult to measure to measurements on the surface of the chips, which might be lower than what is actually happening at the junction to a evaluated junction temperature virtual junction temperature, which is kept of the order of 125 to 150. The assumption is that if you keep your virtual junction temperature to less than 150, then the overall system does not go into a condition where your excess carrier background carriers levels become too high that you are going to uncontrolled conduction and excessive leakage currents.

So, the junction temperature  $T_j$  need to be evaluated not just for your transistor, but also for your diode. So, one would evaluate what losses are happening in your IGBT switches and what losses are happening in your diode. You look at it separately from your conduction prospective conduction loss prospective and your switching loss prospective.

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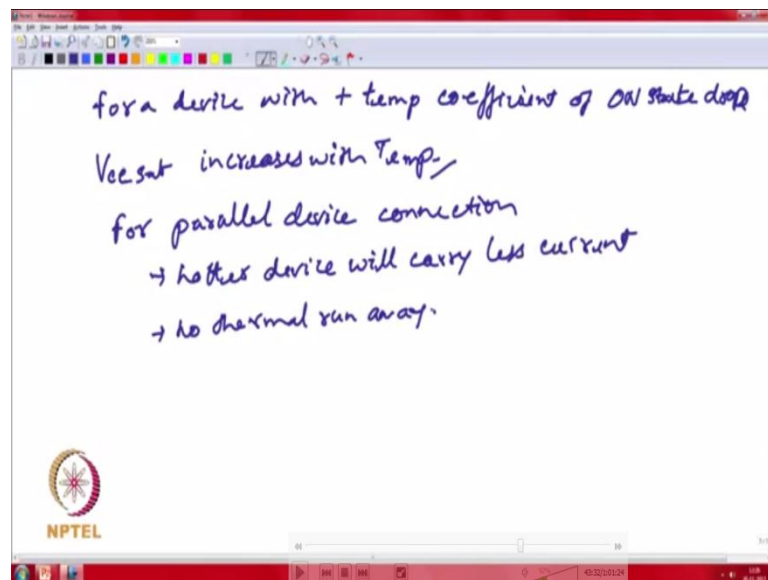


So, to look at your conduction loss, essentially a model for your conduction loss might involve the detail physics of your junctions, which would give you the exact expression for what your voltage drop would be at given level of current when a device is on or it can be simplified as shown in this figure to a voltage  $V_{ce0}$  on-state plus what is shown

over here is the reciprocal, which is whether reciprocal of  $R$  on on-state voltage of your on-state resistance of your semiconductor device

So, if you look at your  $V_{ce-sat}$  your on-state saturation voltage and if you look at essentially what your  $I_C$  is whatever current is going out through the output AC of your inverter leg is essentially going to flow as the collector current, and essentially your expression for your on-state voltage is can be modeled as constant voltage plus a  $I R$  term a drop term. Both these values  $V_{ce-sat}$  and  $R_{on}$  are a function of temperature. So, if you change your temperature, your on-state voltage would actually change. If you look at a positive conductor device with a positive temperature coefficient of an on-state drop your  $V_{ce-sat}$  would increase with temperature.

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So, if you essentially what implies is that a hotter device would actually carry lesser current because, especially when two devices are put in parallel, a hotter device would have a larger drop which means that the other device which is in parallel would be forced to take up the current. So, and essentially what this implies is that you will not have a situation of terminal run away where if you had a hotter device, which whose drop would reduce, then it would actually draw more current and eventually that particular device which is hottest would end up carrying all the current and have the maximum power dissipation. So, if you look at the power dissipation during the conduction



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Conduction power loss

$$P_{\text{cond-Q}} = V_{\text{ce-sat}} \times i_c$$
$$= \underbrace{V_{\text{ce}} i_c}_{\substack{\text{Average current} \\ \text{loss effect}}} + \underbrace{R_{\text{on}} i_c^2}_{\substack{\text{RMS current} \\ \text{loss effect}}}$$
  
$$P_{\text{cond-D}} = V_{\text{D-sat}} \times i_D$$
$$= V_{\text{D0}} \times i_{\text{out}} + R_{\text{D-on}} \times i_{\text{out}}^2$$

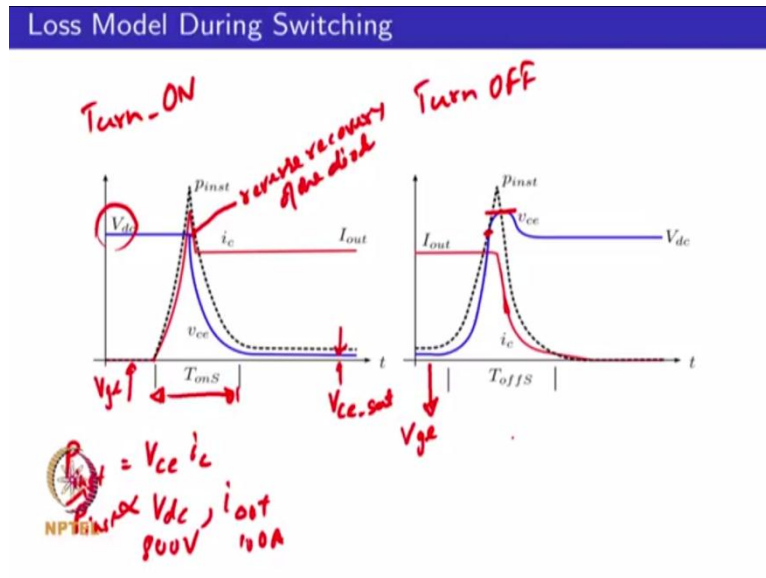
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We have P conduction in a transistor is essentially  $V_{\text{ce-sat}}$  into  $i_c$  and this is equal to  $V_{\text{ce0}}$  times  $I_c$  plus  $R_{\text{on}}$  into  $i_c$  square. So, if you look at the terms corresponding to the power conduction loss, this term corresponds the first term with  $V_{\text{ce0}}$  corresponds to the power loss due to the average current that is flowing during say a switching duration. And the second term correspond to a  $i$  square  $r$  type of situation which would correspond to a RMS heating effect.

You could write a similar expression for your diode your P conduction of a diode is  $V_{\text{diode saturation voltage}}$  times  $i_D$  again can be modeled as  $V_{\text{D0}}$  into  $i_c$  which would essentially be your  $i_{\text{out}}$  plus  $R_{\text{D on}}$  to  $i_{\text{out}}$  square. So, if you look at the switching action between your in your power converter, which is all happening your transferring power from a voltage source side. You might have some stray inductance, but essentially you have a voltage source on one side and you have a filter which are would represent a filter inductor, which would correspond to a current source.

So, essentially this switching action of this layer corresponds to power transfer between a voltage source and a current source. So, you could look at then the next component of the power loss, which is essentially your switching loss.

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And if you look at your switching action you have essentially a turn on and you have a turn off. So, if you look at the sequence of events in a typical switching transition, first you would have a your gate which would actually be a triggered high which essentially gate voltage would be a commanded to go to plus 15 volts, once your gate voltage reaches threshold voltage then essentially your current starts raising and once the current raises above your actual output current, you have essentially your recovery of your reversed your freewheeling diode.

So, essentially if you look at a situation where your current is positive and you are trying to say turn on switch is 1. So, originally your diode D 2 was conducting this positive current, so during turn on your current starts raising, once the current raises above your  $i_{out}$  then essentially your excess carriers which are stored within your diode is what is swept out by this particular current, which leads to a spike in this red we formed over here. So, this corresponds to your reverse recovery.

So, once the reverse recovery phenomenon of the diode is completed, when the essentially your voltage starts dropping down your original voltage which was your DC voltage, which the switch was blocking would now turn come down to your on-state saturation voltage. So, this level over here is your  $V_{ce,sat}$  which is modeled when you look at your conduction drop.

So, if you look at the period of your switching action this is starting from when your current starts raising to your voltage charge reaching quite close to your saturation voltage. So, this particular duration is when there can be a significant amount of participation within your device. So, if you look at your instantaneous participation, your  $p$  instantaneous essentially it is a product of  $V_{ce}$  times  $i_c$ .

So, you can see at the peak point over here essentially you are multiplying  $V_{dc}$  times the current which is essentially your  $i_{out}$  plus your reverse recovery current. So, if you are talking about, so this is proportional your peak value of your participation is proportional to your DC voltage and is proportional to your  $i_{out}$ . So, if you are talking about say DC bus voltage or say 800 volts and say you are talking about current levels of the order of say 100 amps then you are talking about participations of the order of 80 kilo watts.

So, you can see that there can be a significant participation during the switching action, and your ideal switch had a participation of 0 and you can see that during a inductive turn on and the same case for the turn off you can have fairly significant participation and the way to ensure that this participation leads to lesser overall participation is by ensuring that this duration during which this occurs is extremely small.

So, this is what we want to do by keeping gate resistances to be quite small and ensuring that even there is large participation it is occurring over a very small interval. So, as to ensure that your energy that is dissipated is extremely small.

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$$E_{ON} = \int_0^{T_{on-s}} V_{CE} i_C dt \quad \ln(T_j, R_{g_{on}}, V_{g_{e-on}})$$

Data sheet  $E_{ON}$  @  $I_{satd}$ ,  $V_{dc-nom}$ ,  $T_j$  specified ambient/mount  $T_j$

$$E_{ON}(V_{dc}, i_{out}) = E_{ON-std} \times \left(\frac{V_{dc}}{V_{dc-nom}}\right)^{k_v} \times \left(\frac{i_{out}}{I_{satd}}\right)^{k_i}$$

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So, if you look at your  $E_{on}$  on energy during the switching action that would be your integral from 0 to T on and your actual energy dissipation is a function of your junction temperature, your gate resistance and your gate voltage that is being applied. And essentially manufacturers provide data sheets, which contain your turn on losses at different current levels for typical gate resistance that are suggested by the manufacturers.

So, also your data sheet would contain your  $E_{on}$  at I rated and at some nominal DC plus voltage and you might have again at a couple of temperatures you might have it at your room temperatures or your maximum junction temperatures. So, one could actually go by the explicit curves that are provided by the manufacturers or one could actually look at your actual operating condition might not be just at your rated condition at the specified DC nominal that is being used by the manufacturer.

For example, the manufacturer might have specified a DC voltage at 700 volts you might be using it at 600 volts or maybe 800 volts, your rated current might be hundred amps, but you might be operating your converter inwards between 0 amps to may be 50 amps. So, it is important to evaluate your switching energy loss under conditions which are different from what might be specified in the data sheets

So, one way to do it is by actually having curves which interpolate what the switching loss would be at your actual  $V_{dc}$  and your actual collector current or your output current would be  $E_{on}$  under rated conditions times  $V_{dc}$  actual divided by  $V_{dc}$  nom raise to power k v and your actual output current divided by I rated the power of k i of all people take k i is to be equal to 1 and you could actually then derive expressions for your switching turn on loss over a fundamental cycle or a switching loss over a fundamental cycle.

If you look at a your turn off transient similar to the turn on in this particular case you would have your gate voltage being commanded to go off and sometime later your collector voltage would start raising and once your collector voltage reaches your DC bus voltage then your output current starts falling and because your output current is falling with some large fairly significant  $di/dt$  you end up with a  $l_{di}$  by  $d_t L_{stray}$  by  $d_t$  which applies a low voltage on the device and your current fault might be followed by a

tail current, the tail current could correspond to sweep out a carrier from within the IGBT.

So, you can then again find a turn off duration the switching device and if you look at the instantaneous participation in the device during turn off, could write expressions similar to what we did for turn on. And look at what the losses would be during the turn on of transient to. So, if you look at your turn off, and this is a function again of a junction temperature, your  $R_{g-off}$  and your  $V_{ge-off}$ .

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$$E_{off} = \int_0^{t_{off}} V_{ce} i_c dt \quad f_n(T_j, R_{g-off}, V_{ge-off})$$

$$E_{off-s}(V_{dc}, i_{out}) = E_{off-rated} \left( \frac{V_{dc}}{V_{dc,nom}} \right)^{k_v} \left( \frac{i_{out}}{I_{rated}} \right)^{k_i}$$

Sw: loss in diode during reverse recovery

$$E_{off-rr}(V_{dc}, i_c) = E_{off-rr-rated} \left( \frac{V_{dc}}{V_{dc,nom}} \right)^{k_v} \left( \frac{i_{out}}{I_{rated}} \right)^{k_i}$$

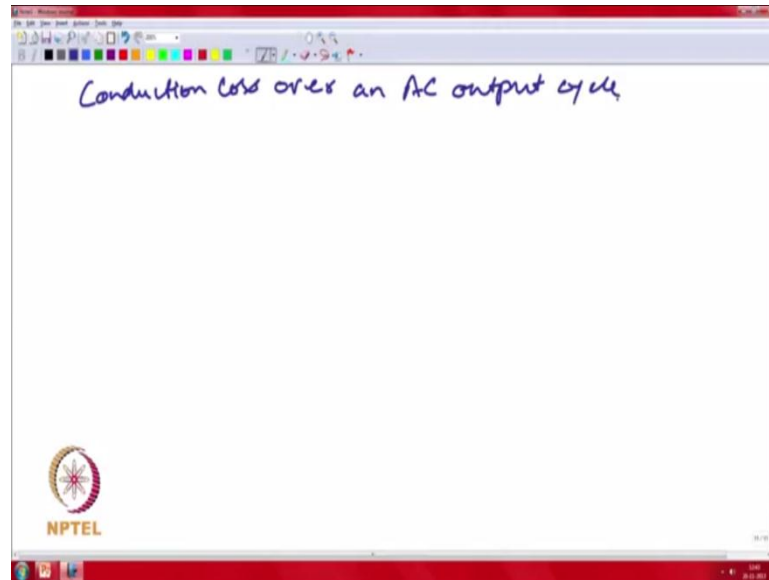
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You could write expressions for to interpolate your off-state your switching loss for a transistor at beside DC bus voltage and your current. So, these expressions are actually given for the switch you could similarly, write an expression for your loss, your switching loss of a diode and if you look at a switching loss of a diode, the most important in a switching loss is the reverse recovery loss in the diode.

Often, the fact is  $k_i$  is taken as 1, so that you could get a linear relationship between your output current and your loss to help obtain simplified expressions for the, for the for your power loss and in case of reverse recovery, it is typically not that linear because you can have significant reverse recovery even when your output current is close to 0. And your reverse recovery current may not change that much with loading as much as what your transistor switching loss terms know.

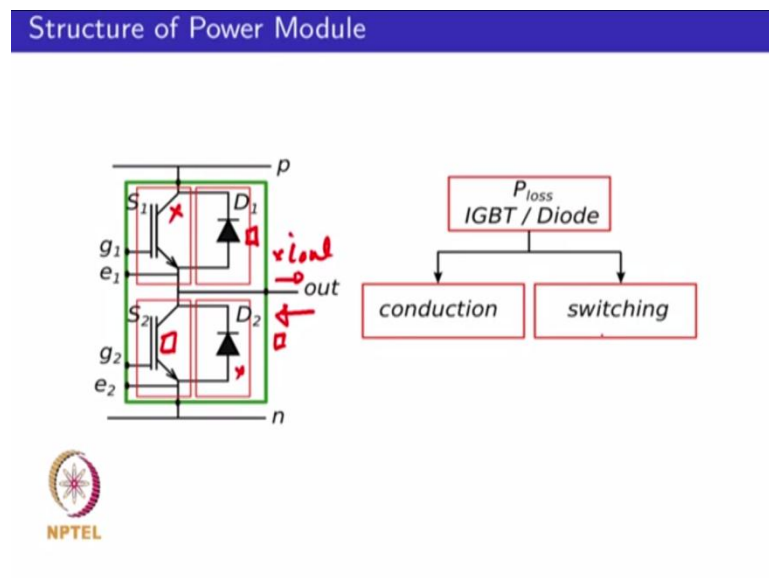
So, once you have your switching loss, you could then try to actually look at what is your overall loss within your switch and the diode, you can write expressions for power loss in the switch and the diode and we will start with the particular exercise.

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So, if you look at the devices that would conduct.

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When  $i_{out}$  is positive essentially that the devices that would conduct is a switch  $S_1$  and diode  $D_2$ , if it was negative, if you had current flowing in say the opposite direction then switch  $S_2$  and diode  $D_1$  would be the devices that would conduct. So, depending on the

polarity of the current we will have to actually look at what would be the device, what would be the particular chip that would have switching loss and conduction loss. So, you would can write an expression for when switching loss is happening in particular switch or a diode and total that over a fundamental cycle to actually look at what happens over the AC cycle which would be used in typical DG systems.

Thank you.