

# An Introduction to Electronics Systems Packaging

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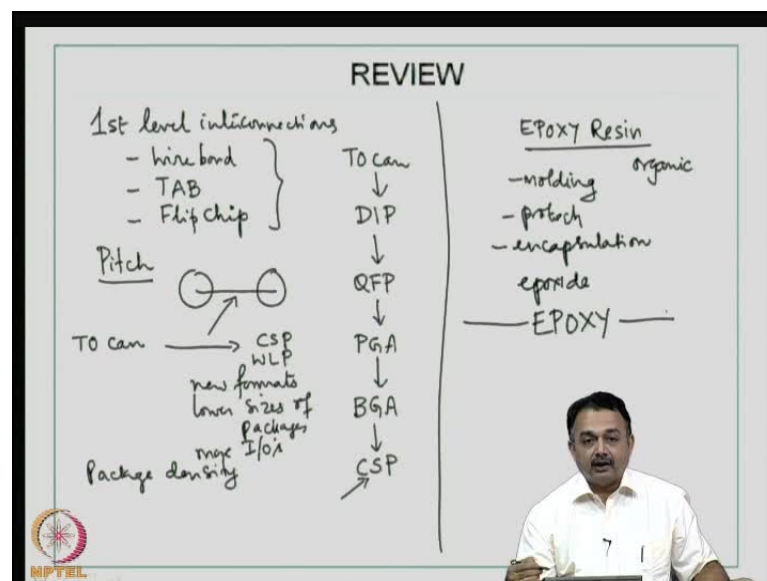
Module No. # 02

Lecture No. # 09

## Wire bonding, TAB and flip chip-1

We will begin with the review of the last class topics.

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If you can recollect, we looked at first level interconnections. What are those first level interconnections? Basically, it is wire bonding or wire bond. The second one is Tape Automated Bonding or TAB and the third one is Flip chip. So, these are the three basic chip connection choices and they form the first level interconnections. Before that, we also had a look at what is the definition for pitch. So, if you have two IO points, the midpoint of these two adjacent pins or pads is referred to as the pitch.

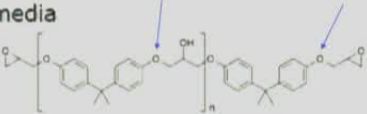
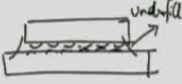
As the decades went by, starting with the TO Can and today we are in the CSP or wafer level package. We have seen that the pitch has decreased tremendously and that is one of the reasons, why we are able to get new formats and lower sizes of packages and more IO pins that are being packed into these packages. So, these talks about package density and it can also get reflected in the assembly process that we are talking about. If you can recollect, we talked about TO Can, then the development came into what is known as DIP packages or Dual Inline Packages, then came the QFP packages called Quad Flat Pack packages, then came PGA or Pin Grid Array packages that are used in lot of microprocessors, then came the migration to Ball Grid Array or BGA packages and finally, today, we have what is known as the CSP class of packages. This is called as Chip Size or Chip Scale package. So, this is what we saw in last class.

We also briefly mentioned about the term called Epoxy Resin. I have shown you different samples of single chip packages in which, I have shown a molding compound that is being used to protect the first level interconnections. It means, you use an organic resin to cover up and protect the first level interconnections like your wire bond or your TAB or the flip chip; so that they are protected from the environment and this is some sort of a protection, you can call it as encapsulation. So, organic chemicals are used, Organic resins are used and one of the most common resins to be used today is epoxide that is the chemical name, which is known very commonly as epoxy. So, I will be using this term called 'EPOXY' quite a few times. I will also explain why this is necessary for protecting your packages.

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EPOXIES *Epoxy Resin*

- Molding Compound; Potting samples
- Package encapsulation ✓
- Underfill media ✓
- Photoimageable solder mask media
- PWB substrate (resin)
- Conformal coating
- COB glob top media- WB and TAB
- Conductive adhesive media
- Solder paste media
  - ◆ And so on...
- Epoxy or Polyepoxide
- Thermosetting polymer (curing with hardener)
- Typical epoxy resin is from Bisphenol A and Epichlorohydrin
- Ciba, DuPont, Shell etc..



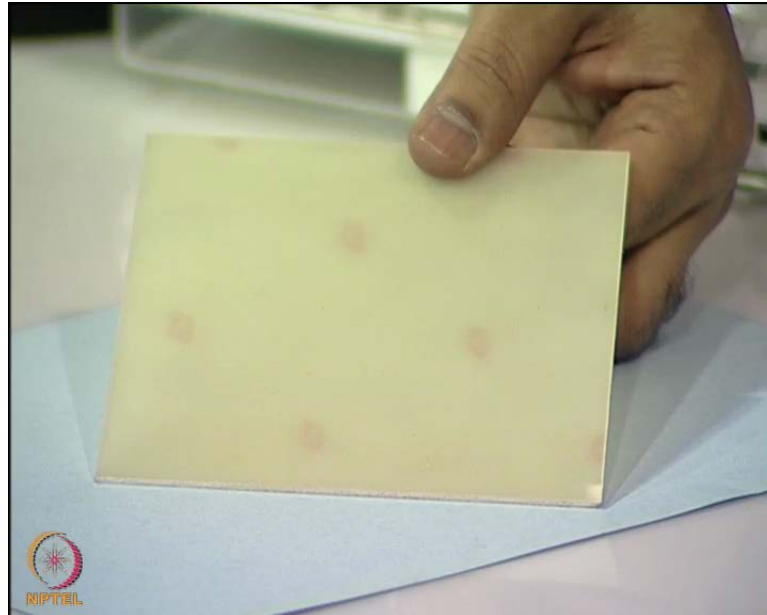
The slide contains a list of applications for epoxy resins, a diagram of a flip chip package with underfill, and a chemical structure of a typical epoxy resin. The chemical structure shows a bisphenol A core with epichlorohydrin groups, forming a polyepoxide chain.

I will first start by telling you the different application areas for using Epoxy Resin. If you look at the slide, there are various application areas in this packaging industry, which can utilize epoxy resin. It is not that epoxy is the only material that needs to be used for these purposes. There are other materials also, but they can be expensive and each of these exhibit different physical and chemical properties. So, in the industry where large volumes are used, obviously you will look at economics, you look at low cost and ease of handling. So, that is probably one of the reasons, why the most common material used is epoxy resin. So, epoxy can be used for molding purposes, encapsulation purposes. The term Potting sample also refers to a methodology, where you can use epoxy material to mold certain compounds for analysis- to look into various aspects of surface topography, inner layers of a buildup substrate and so on. So, it can be used for package encapsulation and it is also used as a material for underfill media.

As I briefly mentioned, when you use a flip chip material; a flip chip is a die, which has got bumps underneath and when you mount it on a substrate- organic substrate or a ceramic substrate, there are bond pads on the substrate, which you will register with the flip chip. The area between the die and the substrate is protected with underfill. So, this underfill material is also an epoxy material, which is very commonly used. We will see, why underfill? What if you do not use an underfill, in the coming lectures.

This particular slide is basically to tell you the different application areas for epoxy. It can also be used as a photoimageable solder mask material in the printed circuit board industry. It is also used as a key ingredient in the manufacture of printed wiring board substrate.

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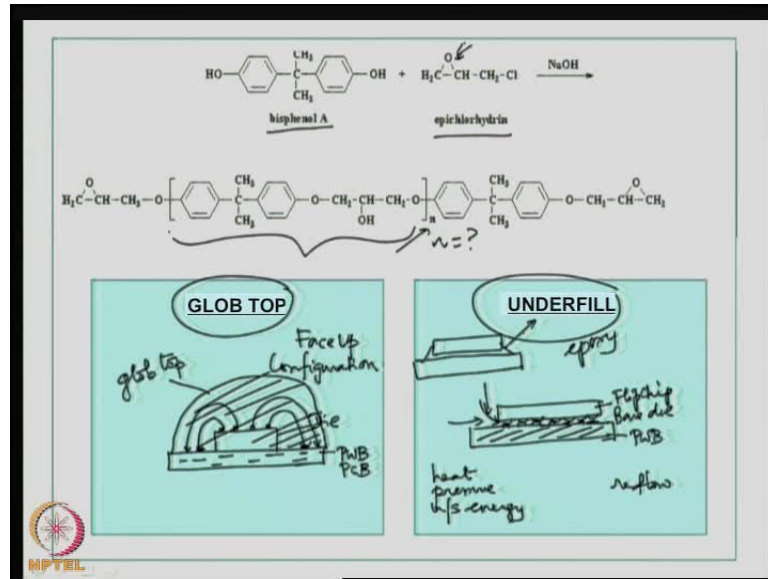


I want to show you a sample of a blank printed wiring board substrate. This is a substrate without copper on both sides. So, this is basically an epoxy material, this is a very rigid material, very hard material and you can also get flex epoxy materials. As I mentioned before, there are different classes of substrates used in the PCB industry. So, I am giving you the best example in terms of low cost and ease of operation. So, it can be used as a substrate for printed wiring board and it can also be used as a conformal coating for finished printed wiring board assemblies. It is also used in chip on board technology; COB is known as Chip On Board technology, where it is used as a glob top.



I will show, what is the actual reaction taking place. There are different manufacturers for epoxy material, I have just listed a couple of companies here. There are many companies manufacturing epoxy resins for the packaging industry. Epoxy is not only used for electronics industry, it is also used for other industries as a binding material, curing material, ceiling material.

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If you look at this reaction here, the laminate structure, which I showed you as a sample here, involves basically formation from a reaction between bisphenol A and epichlorohydrin, which contains the epoxy ring epoxy group in the presence of sodium hydroxide. Therefore, you get a long chain polymer here. The number of elements, the n depends on what kind of molecular weight you require. So, this can be established by defining the weight of the materials that you have taken, that is the starting materials, the time, the temperature, the conditions and what kind of molecular weight you require as an end product to define your application. So, this is a repeated unit that will be defined by the conditions of the reaction. So, once again I want to emphasize and tell you at this point, you should be able to very clearly distinguish between what is a Glob Top and what is an Underfill? Because, these are the two things that we are going to use in this industry. So, I will basically show by a quick diagram on how to use a glob top. Although, I have explained it more than once, I think it is better to do it again.

So, assume this is a PWB or a printed wiring board printed circuit board (Refer Slide Time: 11:50). So, this will be a multi-layer structure and here you are going to place a die; a known good die, on top of which your bond pads are established or the IO's are established. Now, peripherally you do a wire bonding and so you require bond pads on the substrate. Now, you check your wire bonds for electrical contacts and for this particular bare die, where it is a face up configuration. Similarly, for other wire bonds you will be doing the connections. You apply this epoxy resin using a syringe or some other dispenser and cover the entire wire bond structure that you have generated. So, this is a protected area and this is known as glob top. I hope you are clear with this explanation about when to use a glob top configuration of epoxy resin.

In the case of underfill, you have a flip chip. What is a flip chip? It is a chip that is flipped over, which means when you flip it down or flip it over; you have the bumps. This is the flip chip and it is a bare die. Now, you have a substrate on which this is mounted, this can be a printed wiring board. The bumps will touch the bond pads on the substrate by using heat, using pressure, using ultrasonic energy or simply by using a reflow process- reflow is basically remelting the solder material that is there in the bump of the flip chip. Now, a connection is established between the bump of the flip chip and this bond pad on the printed wiring board. There is a small gap between the die and the PCB. So, you need to cover up this area and so that the die is protected and the established new connections are protected. So, what we do is- we use this epoxy material and apply in between the area of the die and the substrate. So, it will take a shape like this (Refer Slide Time: 15:05). So, the underfill will be dispensed in the area between the die and the substrate. So, this is known as underfill and for this also we use epoxy material.



(Refer Slide Time: 15:18)

**TAB (Tape Automated Bonding)**

- Interconnect Patterned On Tape
- Stronger Lead Bonding Strength
- Supports Smaller On-chip Pin Size and Pitch
- Supports upto 850 pins
- Better Electrical Performance than Wire bonds

TAB is an approach to fine the pitch interconnection of a chip to a lead frame. The interconnections are patterned on a multi layer polymer tape. The tape is positioned above the 'bare' die that the metal tracks (on the polymer tape) correspond to the bonding pads on the die. Welding is done using compression bonding.

Handwritten annotations on the diagram: 'Lead frame' with arrows pointing to the four sides of the tape; 'Die' with a circle around the central chip; 'polyimides' with an arrow pointing to the tape.

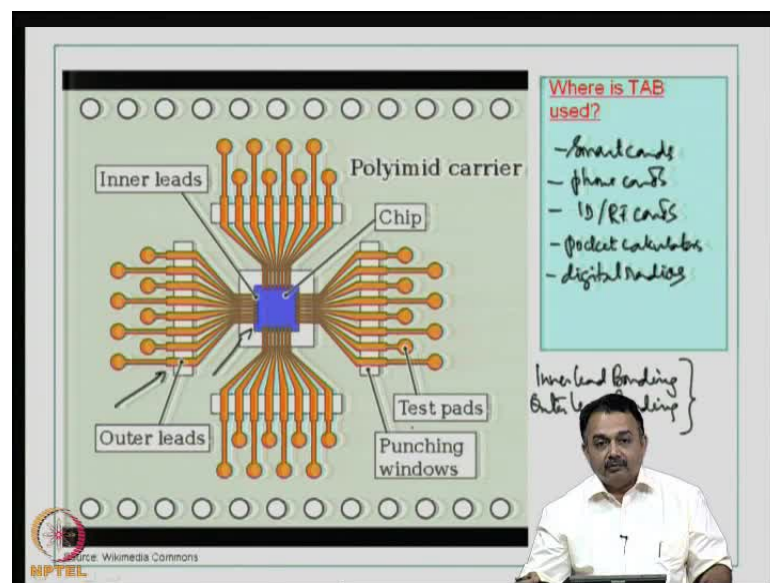
NPTEL logo is visible in the bottom left corner of the slide.

Having seen wire bond, now we will see- what is TAB or Tape Automated Bonding? Tape Automated Bonding or TAB is basically an interconnect structure patterned on a tape. So, as you can see in this figure here, this is a tape and has got these kind of perforations because this is required for mounting on the equipment. This is basically an equipment based operation; automated process. It has got stronger lead bonding because instead of a wire, we are going to use thicker leads. The lead materials can be different, it can be made out of gold, it can be made out of other materials like - kovar, invar. It can be simply tin lead plated materials and so basically, we are going to use leads. It supports smaller on chip pin size and pitches. It supports up to 850 pins and it has got better electrical performance than wire bonds. Typically, the advantage of using TAB is that you can increase the number of IO's compared to wire bond structure.

Wire bond, today is automated, but at the same time it is a very sequential process. Whereas, here it is somewhat a different assembly process and TAB is an approach to fine line pitch interconnections of a chip to a lead frame. So, you are going to use a lead frame structure like your DIP package, the interconnections you can see in this figure (Refer Slide Time: 17:15) that these are the lead frames on four sides of the tape. This tape is basically a plastic material. Typically, we use polyimides or some other form of plastic material. Now, in the center here, you see the die. So, there are three entities here, one is the die, the other is the plastic material or the tape and the third one is the lead

frame, which houses the leads and which are basically the input output pins connecting to the external world. Then this die is brought into registration or into the exact position that is required and that is defined by the lead frames present. So, you can imagine this tape sitting here, your die is coming from underneath and aligning with the lead frames. Now from the top, you use thermo compression bonding and that means you apply heat, pressure. The lead frames will bond with the bond pads on the die and then a connection will be established. So, this is second chip connection choice that we are discussing after wire bonding.

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I think this picture is much clearer. You can see here at the center, you can see the blue color material is the die that is coming from underneath. You can imagine and this material here is the polyimid tape, which has got perforations because it comes in reel form and it needs to be attached to the TAB equipment. These are the lead frames that you can see here. Now, using thermo compression bonding from the top, you can establish connection between the lead frames and the bond pads on the die. So, this is known as inner leads (Refer Slide Time: 19:40) and here this is known as the outer leads. So, a TAB process will involve two types of bonding: first one is- inner lead bonding and the second one is- outer lead bonding. So, you have inner lead bonding and outer lead bonding and you need to understand, what is inner lead and outer lead bonding. What are the temperatures, methodologies and conditions for establishing this bond?

Now, where is TAB used? Typically, you can use TAB in the manufacture of smart cards and these are used in phone cards, ID cards; which use RF, Pocket calculators, the digital radios and so on. So, you can imagine now, the TAB is used, where the product size is very small. Typically, you have just one die that is required to be connected to a lead frame structure and that will establish connection to the other part of the circuitry. So, TAB will involve first an inner lead bonding process and after that it is checked. The outer lead bonding process is established. The extra material of the polyimide is then removed by cutting or removing it from the equipment and so that is TAB.

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**Flip-Chip (C4) Attachment**

- What is Flip-Chip?
  - A method to electrically connect the die to the package carrier
  - The bond wire is replaced with a conductive "bump" placed directly on the die surface
  - Under-fill epoxy is used to secure the attachment and absorb stress
  - The chip is then "flipped" face down onto the package carrier using a re-flow process
  - Bump sizes range from 90-125 microns in diameter
  - Also known as C4 (Controlled Collapsible Chip Connection)
    - Invented by IBM in 1963

**Wire Bonding** ✓

**Flip Chip Attachment**

Now, we come to the third chip connection choice, which is known as Flip chip process. It is also known as C4 process. C4 mean- Controlled Collapsible Chip Connection. In fact, flip chip or C4 is not a new process. It has been established by IBM way back in 1963, but the developments over the years have brought flip chip to the forefront. Today, as compared to TAB and wire bond, wire bond has been used for a very long time in all your DIP packages and QFP packages, where the profile is very high. Today, with low profile components, you are not able to use wire bond because it occupies more space, more volume. So, compared to wire bonding as you can see in this figure here, I think now you are very familiar with the peripheral bonding of wire. As you can see, the bonding of wire bonding process is at the periphery and here these are the gold or aluminum wires, which are attached to the substrate.

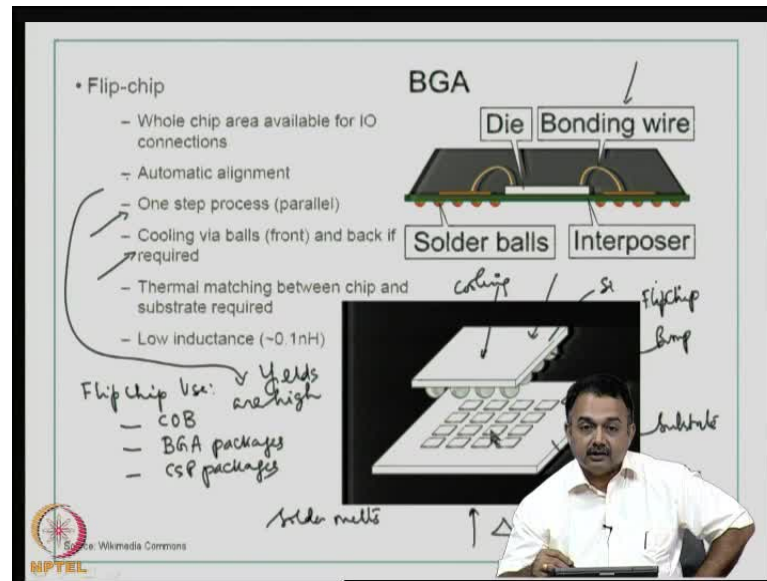
So, the flip chip process, once again is flipping the chip over and these have got bumps. Now, what is the size of these bumps? What is the material of these bumps? The size of these bumps is around 100 to 400 microns. Today, the most common standard is around 125 to 200 micron. Now, the pitch is also very similar and so you can imagine the difficulty in establishing a flip chip bonding, even if it is through sophisticated equipment. You have to have a very good registration procedure in the equipment and so, establish a very good flip chip connection. Now, this is the Die and it is flipped over the material. It is used in flip chip and it is basically tin, lead or other tin based material. If you do not want to use lead, as lead causes a health hazard. So, you can use tin, silver, copper or some other form of material used involving only tin and indium or tin bismuth and so on. We are going to look at these things at the later part of this course and so you require a substrate. So, once you have a flip chip ready to be assembled. Next, what you require is a substrate and the substrate should have bond pad, which is also very small in size matching with the area or the area of the solder bump.

Now, you apply heat, pressure and also apply heat to the board on the substrate. So that using thermo compression bonding, you can establish a connection with the two components and then you apply an underfill material to protect your substrate. So, this is a method to electrically connect the die to the package carrier. The bond wire here is replaced by a conductive bump placed directly on the die surface. So, the bumping process itself is a technique, which we are going to look at very shortly. So, when you use a flip chip, you will have to look at the materials used in the bump because only then you can characterize the reliability. You can understand the reliability of the solder joint established by the flip chip and also you need to characterize different types of materials that are used in flip chip. So, you need to have a very good understanding about the bump material, the substrate material, basic thermal and the Mismatch that can happen between the bare die, which is silicon and your organic substrate, if you are using economic organic substrates. So, you can use underfill epoxy to protect the die and the substrate because there is going to be stress when the board is in operation or when the chip is powered up, there can be heat. That can come from the chip, if it is accumulated, it can crack the die. It can warp the substrate and it can affect the solder joint.

So, the chip is flipped face down. As we have seen here, using a reflow process and so in addition to thermo compression bonding, you can also use a reflow process reflow.

Basically, it means, we are going to melt the solder bump again and establish a new metallurgical bond with the bond pad on the substrate. The bump sizes range from 90 to 150 or 125 microns in diameter. So, you can imagine that this is a very high dense connection and this is not a package. Mind that flip chip is not a package and you need to have a fairly good understanding if you want to use C4 or flip chip.

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Now, where is flip chip used? Flip chip is used in the manufacture of ball grid arrays and CSP's. So, flip chip is used as a chip on board; directly on to your substrate, it can be used in the manufacture of BGA packages, it can be used in the manufacture of CSP packages. So, the whole chip area is available for IO connections and that is how the density increases automatic alignment. It is a one-step process, I want to explain to you, what automatic alignment means. Now, if you look at this figure (Refer Slide Time: 28:30) here, there is a die and this is the bump. This is your substrate, now you are going to align this die with the substrate. Now, this bump is basically a solder material. When you apply heat to the process, assume it is a reflow process. We are going to apply heat, what will happen? The solder will melt because it is a melting process. The flip chip or the chip will try to move away from its position slightly, but the surface tension of the solder material in conjunction with the bond pad area and the bond pad material will pull back the die to its original position. So, there is absolutely no reason why you will have misalignment during the reflow process of a flip chip because of the automatic alignment

provided by the surface tension of the solder material. Pulling back the die to its original position, you will get 100 percent perfect alignment and that is how the yields are very high.

So, the automatic alignment actually provides you a much better yield compared to other processes. It is a one-step process because all the connections are established at one time. During the reflow process, the cooling of the entire die takes place through the solder bump material. and also from the top of the die. So, this area is also utilized for cooling because it is exposed to the atmosphere. There is always a question of thermal mismatch between the silicon and this is a plastic material. So, there is going to be a thermal mismatch. We will see how we can remove or minimize this mismatch. Of course, one important thing that takes care in minimizing the thermal mismatch and protecting the die is- using an underfill material.

So, a BGA or a Ball Grid Array can be fabricated either by using a wire bond structure or by using a flip chip structure. So, there are two methods to create or manufacture or design a BGA material. In this, (Refer Slide Time: 30:18) the first case there is a die here and there is a die here. There is a wire bond that takes place to the bond pad on the substrate and similarly at the periphery. There is a substrate, which is highly dense and which provides the solder balls at the bottom, providing the second level interconnect. In this case, it is a different process all together.

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**Flip Chip**

Flip-Chip is :

- NOT a Specific Substrate material
- NOT a Specific Package like SOIC
- NOT a Specific Package Type like QFP, BGA or PGA
- Can be mounted on organic and ceramic substrates; in other words- at board level too

COB

Where is FC used?

- digital cameras
- Camcorders
- Laptop
- Comm/Handheld products

\*\*Summary of first level connection choices\*\*  
Next up: Description of Wirebonding, TAB and C4 processes

WB  
TAB  
C4

NPTTEL

So, a flip chip is not a specific substrate material, you must be clear about it. This is not a specific package like SOIC- Small Outline Integrated Circuit or QFP or a BGA or a pin grid array and this is basically a chip connection choice. Please do not confuse a flip chip with a package. It is not a package at all, it is a first level interconnection choice. It can be mounted on organic and ceramic substrates. In other words, it can be directly used at the printed circuit board level like your chip on board. When you say board, you can use it as a chip on board activity.

So, where can we use flip chip? What are the application areas for flip chip? Flip chip can be used on boards. Let us say, it is used in digital cameras or camcorders. It can be used in laptop motherboards, it can be used in communication handheld products. So, flip chip combined with a BGA or a flip chip in a CSP format are the most favored package choices today, for application areas in various segments like cameras, camcorders, laptop, various handheld products.

So, what we have seen now is the summary of all of the first level connection choices. We have seen exclusively, what is a wire bond? What is a TAB and what is a flip chip or a C4 process? Now, what I am going to do is- give some more inputs to you on each of these first level connection choices and so that you can understand the process sequence.

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**Wire Bonding**  
Used in interconnecting the Die to various substrates

...the most popular interconnection method

Wire bonding is a **SOLID phase welding process** where the two metallic materials, a **thin wire** and the metallization on **pad surface** are brought in intimate contact under a combination of **heat, pressure and/or ultrasonic energy**.

Ultrasonic  
Die  
Package

NPTEL

The slide features a diagram of a wire bonding process where a thin wire is being connected to a die on a package using ultrasonic energy. A speaker is visible in the bottom right corner of the slide frame, gesturing while presenting.



How do you do wire bonding? Wire bonding is used in interconnecting the die to various substrates. It is the most popular interconnection method. So, it is a solid phase welding process, where the two metallic materials are going to use a thin wire. A thin wire can be gold or aluminum. Today, copper is also used and a metallization on the pad surface is also ready for this bonding process. So, on one side, you have a thin wire and the other side you have a pad surface that is ready to take up the wire. These are brought together in intimate contact by the wire bonding process using a combination of heat, pressure or ultrasonic energy. So, you can decide what combination you want to make the process simple without providing too much heat that can damage the substrate. So, if you are using gold, you can use a thermo compression bonding. If you are using aluminum, you can lower the temperatures and so on.

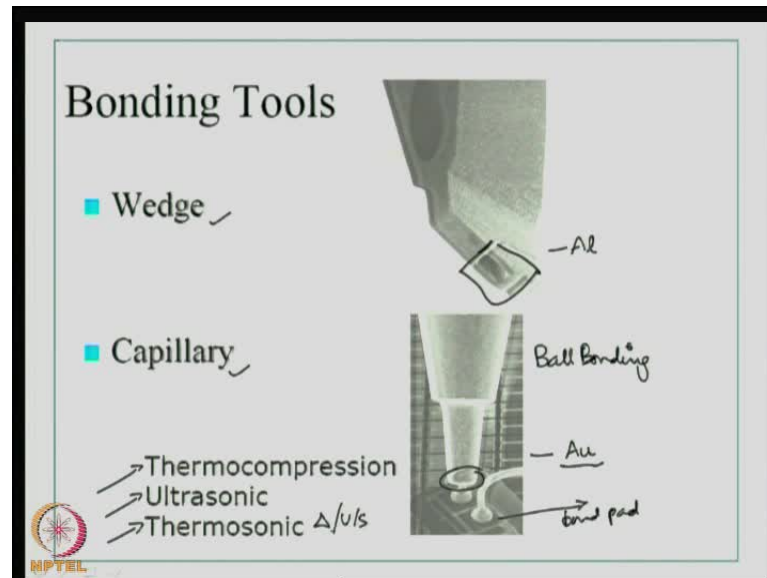
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The slide is titled "Wire bonding - Types" in a red box. Below the title, it states "Wire bonding is made using two types of tools:". A list of tools is provided in a box: "a. Wedge - Called **wedge bonding**" and "b. Capillary - Called **ball bonding**". A handwritten word "Tool" with an arrow points to this list. Below the list, it says "Very inexpensive- A penny per pin!". At the bottom, a box contains the text "Progress in IC packaging is essentially due to technology improvements in WIRE BONDING", with an arrow pointing to the underlined term. The NPTEL logo is in the bottom left corner.

So, wire bonding is of two types: one is known as wedge bonding and the other is known as ball bonding process. The wedge bonding uses a wedge tool and here the tool is a Wedge tool. In the ball bonding process, you use a capillary, where you can draw thin wires. The wire diameter depends on the space availability. If you are using a chip on board directly on board, probably you can have more area to utilize, but if it is in a package on a lead frame, then you have to be very critical in choosing the diameter.

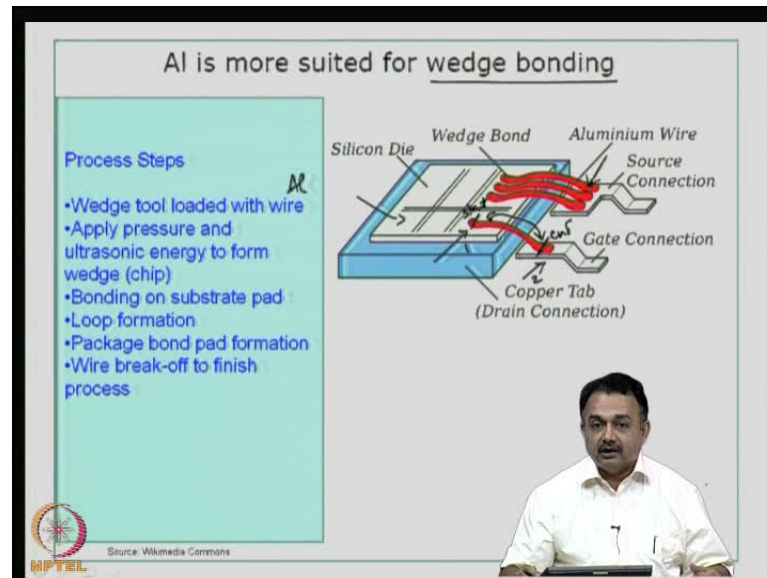


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So, the improvements over the years have been due to the increase in Wire Bonding equipments that are available because the speed of wire bonding is very much essential to increase the volume output in a commercial manufacturing set up. Today, every wire bond is almost highly inexpensive. It is about a cent or less than cent per pin. So, the bonding tools are of two types: wedge and capillary tool and that is used for bonding. Wedge tool utilizes aluminum. You can see the shape of the wedge tool, which is flat, large and capillary. It comes out in different sizes depending up on the diameter of the wire that you want to draw. Typically, gold is used for capillary ball bonding and here you will use ball bonding process. The classification of the entire bonding can be thermo compression ultrasonic or thermosonic. If it is a combination of heat and ultrasonic energy, then it is known as thermosonic bonding.

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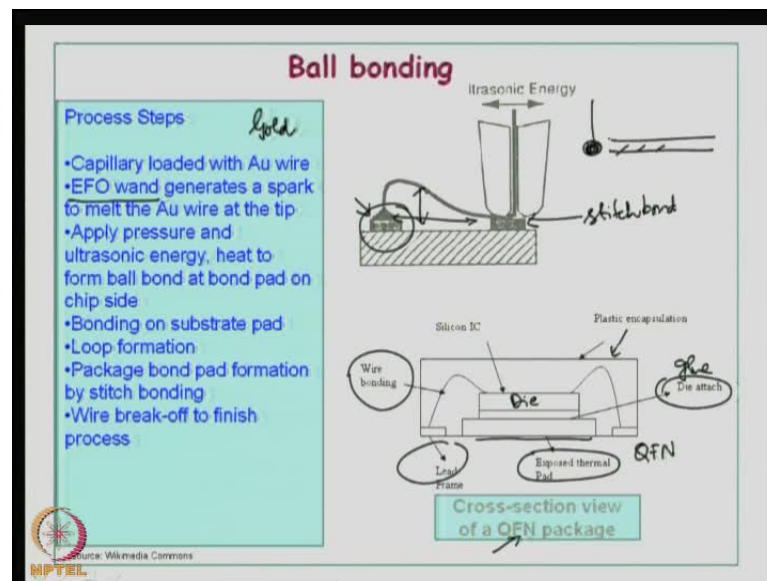


Now, aluminum is more suited for wedge bonding. The reason is- aluminum is easy to work with, mechanically compared to gold. If you can look at this figure (Refer Slide Time: 38:08) here, what I am basically trying to show you is a wedge bond that has been formed using aluminum wires. Now, this is the silicon die and as you can see it is labeled. Then this is the wedge bond from the bond pad on the silicon die to the lead frame. Let us say or the leads of the package... Now, you see a wedge has been formed and at this area you can see the connections are barely large. It requires larger area and size. Basically, you cannot expect too much of high density using wedge bonding process.

What are the process steps for a wedge bonding process? The wedge tool, which you saw earlier is loaded with the wire, typically aluminum. Now, you apply pressure and ultrasonic energy, the reason for using ultrasonic energy is you can reduce the temperature of operation because the ultrasonic energy will require a minimum amount of energy in the form of heat. Otherwise, the actual operation for wedge bonding will require much larger temperatures and it can affect your substrate. So, you apply required pressure and ultrasonic energy to form a wedge. So, bonding is done first on the substrate pad, then a loop is formed. This is basically the loop and now as a experienced person, you will decide how much loop and height you require for forming a wedge bond. After the loop is formed, then the package to bond formation will be done. So, this will be the

first sight, (Refer Slide Time: 40:04) where the wedge bond will be formed and this is the second site, where the wedge bond will be formed. Finally, the wire is broken off here. This is the start point and this is the end point. So, that completes the wedge bonding process. Now, this has to be faster in the industry, if you want to have more through put from the wedge bonding process.

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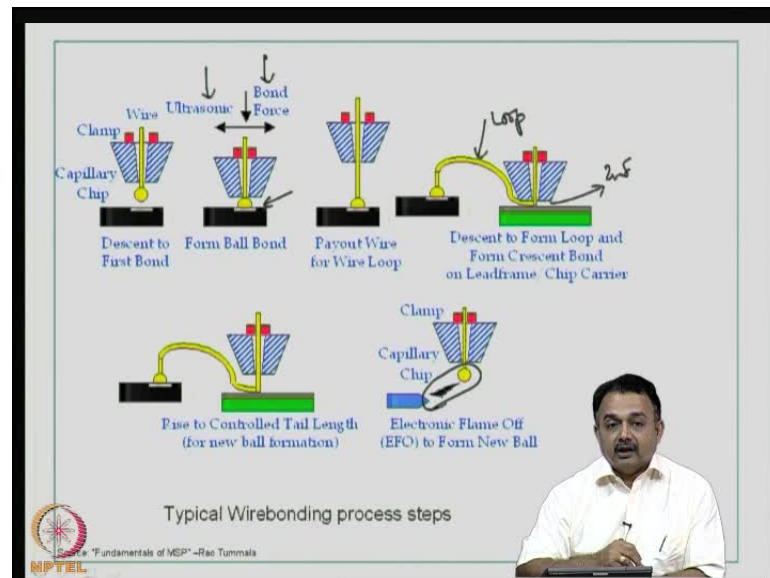
Let us see, what is a ball bonding process? Obviously, as the name indicates, you have to form a ball of the gold wire. The most popular material for ball bonding is gold. The capillary is loaded with the gold wire depending upon the thickness that you want. It can be ranging from 50 microns to 300 microns depending upon the bond pad area available and the peripheral number of connections that you have.

Now, you can create an electronic spark. Electronic flame of wand will generate a high voltage spark that will melt at the tip of the gold wire to form a bond. Basically, I will show you a video clip, which you can understand. Basically, there will be a wand, wire and this will melt the wire to form a ball. This molten ball will now be utilized here. So, you can imagine that this molten ball is at the first bond site on the die. Then using appropriate pressure, ultrasonic energy or a combination of heat and pressure, ultrasonic energy and the ball formed, you form the first bond here. Now, you take a loop and this loop height is very important. There are various calculations that are required to determine or fix, what loop height you want and what loop length is actually... this is

determined by the two bond pads. This distance is fixed and so according to this, what loop height you require is dependent on the thickness of your gold wire. Then after the loop is formed, the package bond pad formation is done here at this point and this is known as a stitch bond. This is not a ball bond; this is more like a stitch formation. So, that completes the two ends of the wire bonding. The first one is- ball bond and the end one is a stitch bond and then here the wire is broken off to complete the process.

So, this is the cross-section of a single chip package (Refer Slide Time: 43:16); this is a QFN package or Quad Flat No lead package. As you can see here, it is a cross-section. You can see the lead frame at this point. You can see this is the area, where the heat will be dissipated to the substrate. So, this is an exposed thermal pad and there is a die attached material here. Glue that bonds the chip to the substrate, then you have the wire bond here. Wire bonding is done on both sides of the peripheral; this is the die (Refer Slide Time: 43:49) and then this is the encapsulation. This part is the encapsulation and so you must be able to now draw such cross-sections for a wire bond BGA, for a wire bond QFP, for a flip chip BGA and so on, as we go along.

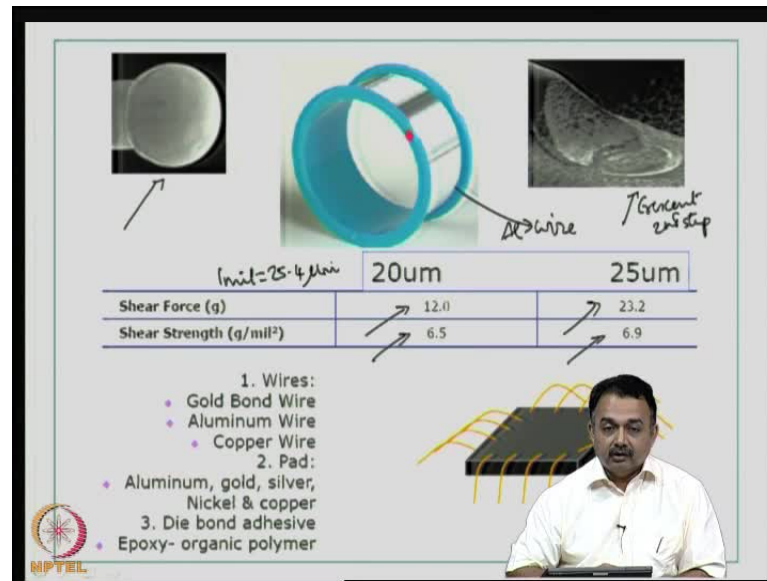
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So, this is a pictorial depiction of the wire bonding process. You can see here, there is a clamp, there is a capillary and then comes the ball formation. The ball now touches the pad surface. The formation of the ball there is an ultrasonic energy; there is a pressure and that reduces the temperature. The ball bond is established and now the clamp is

pulled over the loop is formed. This is the loop (Refer Slide Time: 44:48) and the loop formed is taken to the next site. This is the lead frame or the package. So, this is the second landing site for the wire. So, a crescent bond or a stitch bond is formed and then it is cut off. So, this is a picture (Refer Slide Time: 45:08) showing you, how a high voltage spark will create a ball and that is now utilized to form the first bond.

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So, the wires for wire bonding can be gold, it can be aluminum or copper. The pad that is required for leading the wires to form the attachment can be made out of aluminum, gold, silver, nickel and copper. Die bond adhesive is used to bond the die to the substrate and that adhesive is basically a epoxy organic polymer. So, this picture (Refer Slide Time: 42:50) shows you micrograph of a ball that is created. This is the commercially available wire, which you can utilize for wire bonding. So, this is typically aluminum, but you can also get gold of different sizes and diameters. This is the crescent or the stitch bond that you can see, which is used in the second step of the wire bonding process. So, the loop height is determined by the diameter of the wires. The normal test after wire bonding is done basically to pull the loop and look at the loop strength. So, there are certain standards that you can look at in the hand book. You can determine the quality of the wire bond and so typical guidelines are given here. For 20 microns and 25 micron wires, the shear force is around 12 grams and the shear strength is about 6.5 grams per mil squared and 1 mil is 25.4 microns.

So, like that, if you can look at for different materials and different thicknesses. If you are doing wire bonding at your laboratory, you can do quality test in your own lab.

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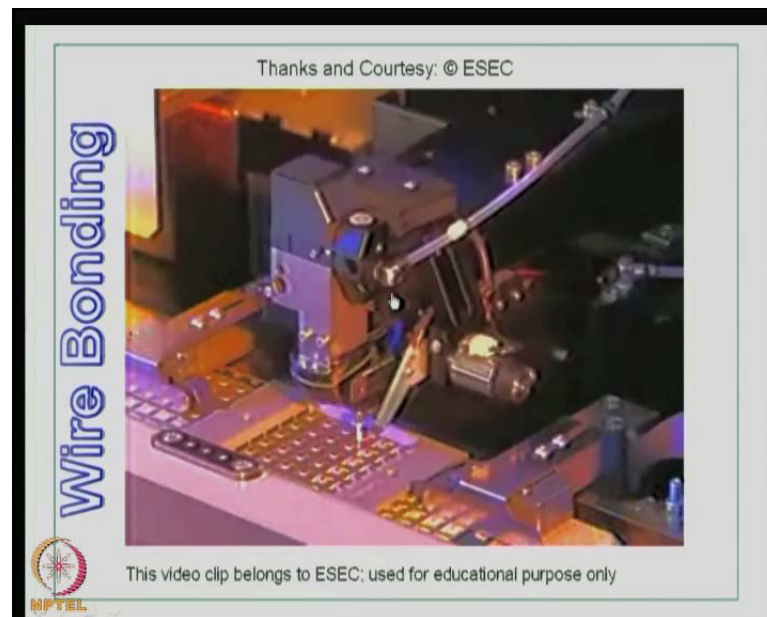


Now, I would like to show you a video clip of a wire bonding process. This is die bonding, which I am going to show. As you can recollect, die bonding is basically attaching a die a known good die, that is, a silicon die to a substrate.

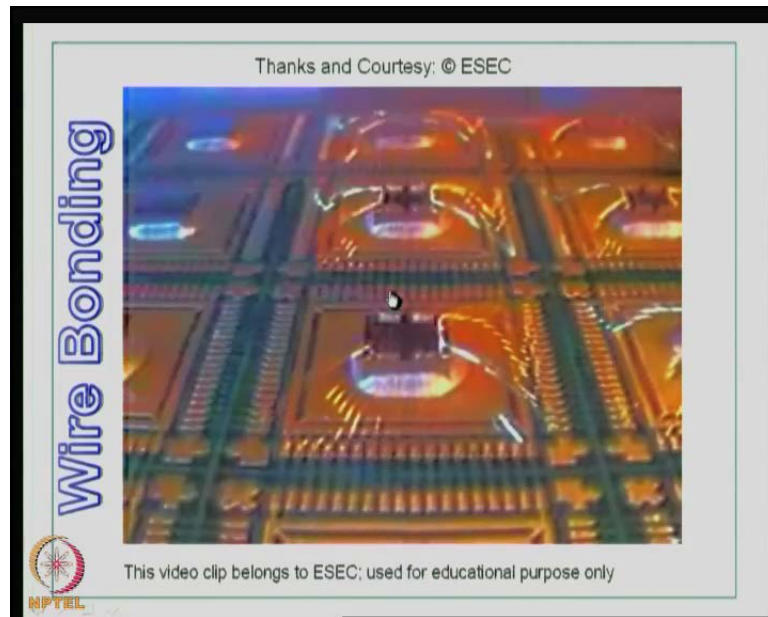


So, what you have seen in this video is a glue an epoxy material is dispensed using syringes. It can be done by other methods also on to the area or the substrate, where the die is going to be placed. This is a nonconductive adhesive and it is used for all the first level connection process like wire bonding. Before wire bonding, you have to do an adhesive bonding. Except, in the case of a flip chip, where you do not require an adhesive bonding because your solder bump is going to be flip down and that will establish the connection with the substrate.

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Now, what I am going to show you is a video clip of a wire bonding process. So, you can see the wire bonding process in the industry is highly automated. The throughput is very high. The number of hits or number of wire bonds established per minute is very high and that is how your yields in forming the packages, first level interconnections has a very high bench mark and that is set by the industry today. So, this also possess a very big challenge for the equipment manufacturers because they also work in close tandem with the package assembly people.



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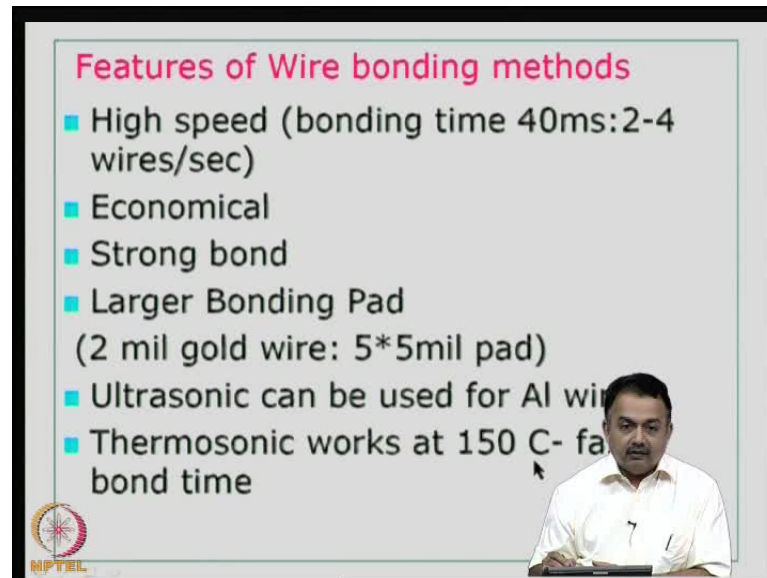


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Now, I will show you what we have seen earlier. Clip is basically a high throughput wire bonding process. Here, we will see the individual bond that is ball bond, wedge bond and another type known as ribbon bonding. Ball Bonding is a technique for interconnecting silicon chips. Here, we see ball bonding on 200 micron diameter. An aluminum wire arc is used to produce a ball on the end of the wire. The ball end allows a multi angle upon the placement approach. It is pushed down and ultrasonically welded to the chip. The wire can be led to a lead frame or the substrate and wedge bonded. The process is normally used with gold wires. Wedge bonding is used mostly on aluminum wire and is a reliable method of joining silicon devices to substrates and lead frames. Both process can be automated to achieve speeds over three to ten loops per second. Here, we see ribbon bonding, which is used primarily in high frequency devices.

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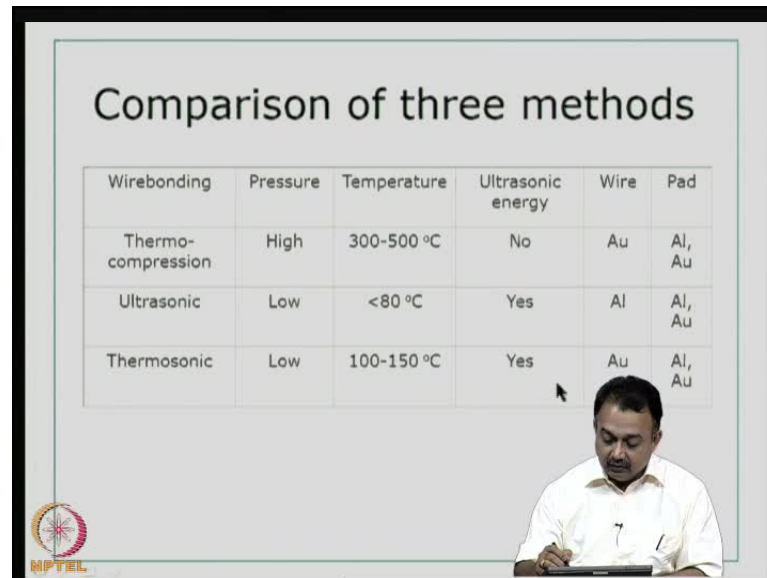


**Features of Wire bonding methods**

- High speed (bonding time 40ms:2-4 wires/sec)
- Economical
- Strong bond
- Larger Bonding Pad  
(2 mil gold wire: 5\*5mil pad)
- Ultrasonic can be used for Al wire
- Thermosonic works at 150 C- faster bond time

So, you can see that wire bonding process in the industry depends on a high throughput. Typically, we are looking at something like 60 to 70 hits or wires per minute. So, it has to be very fast and has to be accurate. All the processes are to be in tandem, if it is a ball bonding process, the formation of the ball, the formation of the loop and then the stitch bond should occur in perfect tandem without any misalignment. So, the features of wire bonding is- it should be high speed, economical, strong bond and quality reliable bond. So, obviously, you have to do some post wire bonding quality checks continuously. The bonding pad area depends on what type of materials you are using. If it is a wedge bond, you require more area and if it is a ball and stitch bond, you do not require that much area. For example, if it is a 2 mil gold wire, as I said, 1 mil is 25 microns. If it is 2 mil then, you have to use about 5 by 5 mil pad to establish a reliable connection. Ultrasonic bonding can be used for aluminum wires and thermosonic works at 150 degree centigrade, faster bonding time.

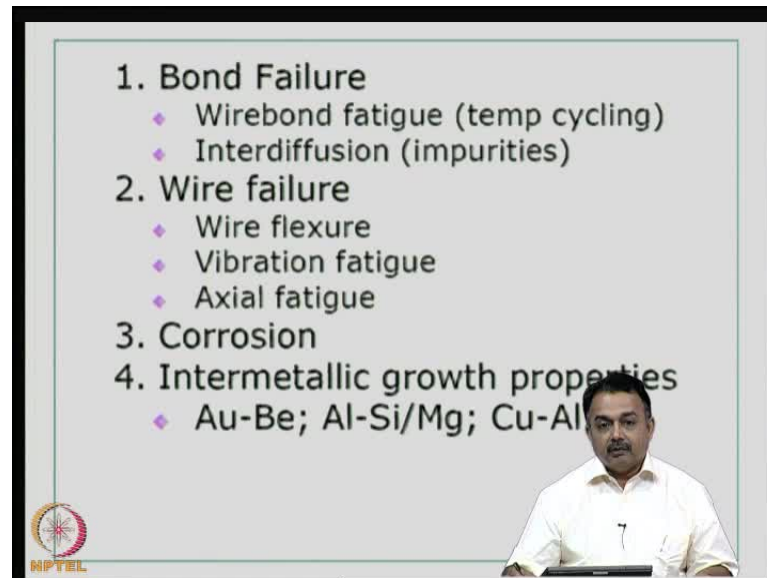
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Wirebonding	Pressure	Temperature	Ultrasonic energy	Wire	Pad
Thermo-compression	High	300-500 °C	No	Au	Al, Au
Ultrasonic	Low	<80 °C	Yes	Al	Al, Au
Thermosonic	Low	100-150 °C	Yes	Au	Al, Au

So, you have seen now thermo compression bonding, ultrasonic bonding and thermosonic bonding. Here, the pressure used is high, low pressure, low pressure and temperatures between 300 and 500 degree Centigrade. Whereas, if you use ultrasonic, it can be much less and So that depends on the material that you are using. In thermo compression bonding, you do not use ultrasonic energy. Here, obviously you are using ultrasonic energy and the wire used for thermo compression bonding is gold. For ultrasonic, it is aluminum and for thermosonic it is gold. The bond pads typically have to match, for gold you can use aluminum or gold, but today, if you are using wire bonding on printed circuit board, you can have nickel gold as the surface finish for wire bonding.

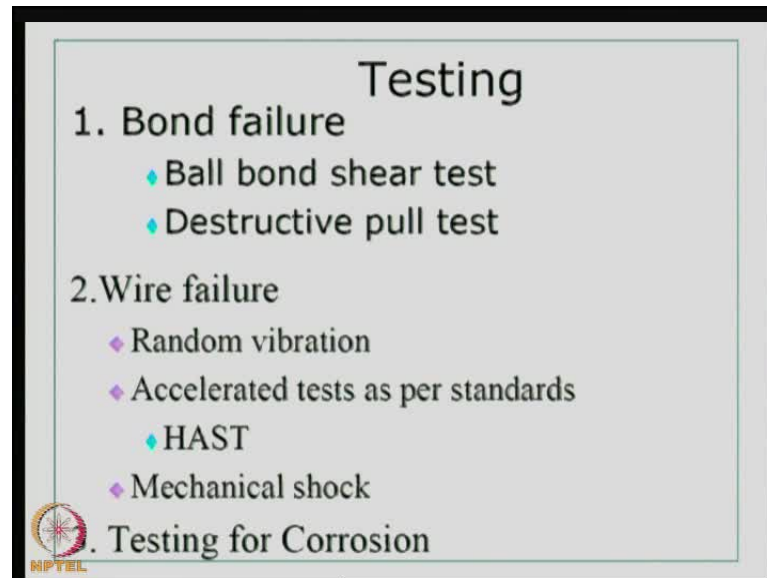
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1. Bond Failure
  - ◆ Wirebond fatigue (temp cycling)
  - ◆ Interdiffusion (impurities)
2. Wire failure
  - ◆ Wire flexure
  - ◆ Vibration fatigue
  - ◆ Axial fatigue
3. Corrosion
4. Intermetallic growth properties
  - ◆ Au-Be; Al-Si/Mg; Cu-Al

Bond failure can always happen, there can be fatigue related to wire bonding because of temperature cycling or basically, when you power up the chip, there can be effects caused by heat. So, typically, you do a temperature cycling to qualify the wire bonds. Impurities can creep in because of various materials that are used, the impurity of the host material. There can be inter-diffusion and that can lead to failure of the wire bonds. It can basically reduce the strength and can increase the fatigue of the wire bonds. Wire failure, wire flexure, vibration fatigue, axial fatigue depends on the application. Corrosion is from the materials that are used from the harmful effects of the intermetallic growth materials that have been formed.

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**Testing**

1. Bond failure
  - ◆ Ball bond shear test
  - ◆ Destructive pull test
2. Wire failure
  - ◆ Random vibration
  - ◆ Accelerated tests as per standards
    - ◆ HAST
  - ◆ Mechanical shock
3. Testing for Corrosion

NPTEL

Basically, you have to do testing, ball bond shear test or the destructive pull test, after the bond has been formed. Other mechanisms like random vibration test because wire bond is subject to fail during vibration accelerated tests as per standards and that means HAST. It stands for Highly Accelerated Stress Test, where you set up certain temperature and humidity conditions as per the standards. It can be military standard or other industry standards. Look at how your wire bonds perform or survive and you can also do standard mechanical shock test, vibration shock test and testing for corrosion.

So, today, we will end here. We have covered all the basic first level interconnection choices in detail. In wire bonding, we have also seen the complete process flow. In the next class, we will start with the process flow for TAB and the flip chip. Thank you.