An Introduction to Electronics Systems Packaging

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Module No. # 02

Lecture No. # 08

Wafer Packaging

Packaging Evolution

Chip Connection Choices

Today, we will start with the review of the previous class.

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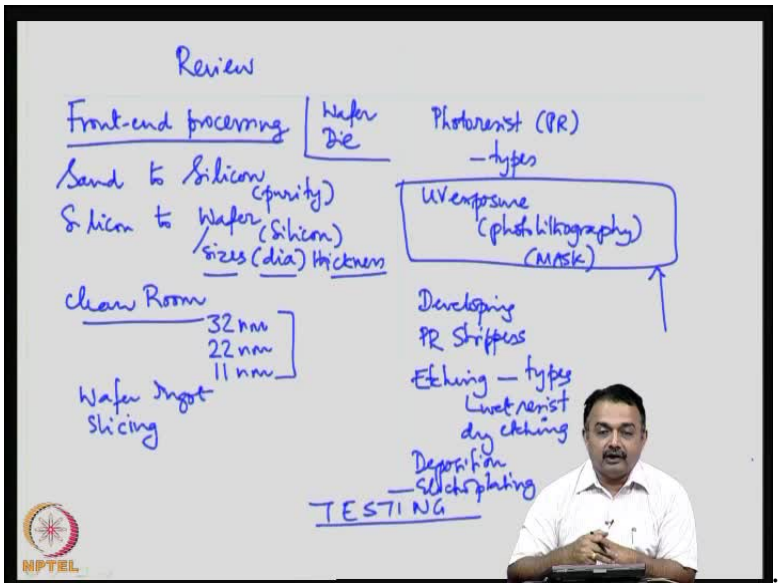

If u remember or recollect, we have looked at the front-end processing of semiconductor fabrication. Some of the important points that we saw in the front-end processing to get a wafer and then a die I will bring out here, so that you can recollect. Basically, we saw

that from sand we tried to look at the process details to get pure silicon. We also stressed on the need for high-purity silicon – 99.999; ((.)) purity is the kind of electronic grade silicon that we need to manufacture.

From silicon, we move on to manufacture a silicon wafer. I also highlighted in the previous class the different sizes of wafers that are currently in use – basically the diameter that are being used today for processing. As the diameter increases, you are going to get more dies accommodated on the wafer, but at the same time the yield percentages have to increase; otherwise, the manufacturing costs are going to be larger and accountability will be very high.

Therefore, whether it is a silicon or a compound semiconductor or other material, sizes are very important; the thicknesses are also very important. We also briefly talked about clean room facilities, because, as you know, we are working on very very fine line widths. Typically, today, the standard in industry is 32 nanometers; we are moving towards 22 nanometers; maybe in 2015, we will be in 11 nanometers. Therefore, the technologies require clean room facilities that have to be maintained and qualified every day and every hour. The clean room maintenance and the costs are going to be very important in the manufacture setup.

Then we saw from the wafer how the wafer ingot is got, how it is sliced into the required thickness and the diameter specified for the particular process design. Then we talked about various process details like what is a photoresist; we saw the different types of photoresists: negative, positive, wet, dry and so on; then the all-important process of UV exposure which you can call as photolithography which basically defines the image that you have got in your mask onto the surface of the wafer. This becomes a very important crucial defining moment for the process of the wafer to the die (Refer Slide Time: 04:03).

The other subprocesses, if you can call them, are the developing process which again works on the photoresist material depending upon whether it is exposed to UV light or not exposed to UV light. We also talked briefly about the advanced methods of photolithography – not necessarily UV exposure, but other methods like x-ray lithography and so on; so, the developing process is very important.

Photoresist strippers – we briefly saw how they define the image and make it ready for etching process. Etching is again a defining process for the image to be well-defined on the surface of the wafer. We saw different types of etchings; typically, wet resists are used, but we also briefly saw how dry etching can be employed in the semiconductor manufacturing or even in the board-level manufacturing like dry plasma and so on.

Then finally, the conductors – the copper conductors or the aluminum conductors depending upon what material you are using – have to be realized by deposition process. We briefly saw electroplating and other methods like chemical vapor deposition, PVD evaporation techniques and so on. Finally comes the testing; by testing, we are going to qualify the wafer by doing electrical tests on the completed wafer; this will qualify the wafer. The next process enters into the back-end process of the wafer fabrication which we are going to look at today.

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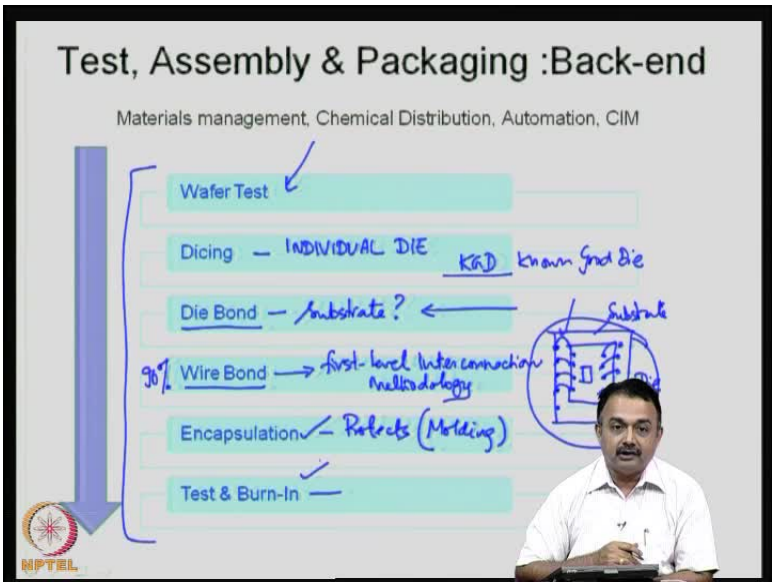

If you look at this flow chart, we are now at the back-end processing of the die manufacturing; this is known as test, assembly and packaging section. The first one was basically from the silicon to wafer. The wafer here is tested, as I mentioned earlier; test becomes very important in every step. I have written about six steps here, but in practice it goes through a very large line of subprocesses including electrical test, materials management, material analysis and so on.

The wafer that is manufactured from the front-end process is tested. The next step in the back-end process will be dicing the material. Here, we have to make the individual dies; the die that is sliced from the wafer and quantified as a known good die (I think I have repeated this term KGD known as known good die) will be bonded on to a substrate. Every die when it is about to be packaged requires a substrate. What type of substrate can be used? Is it a plastic substrate or is it a ceramic substrate? What kind of material requires to be used as a substrate? We will see what is die bonding. Basically, here, the die is attached to the substrate; that is the basic process in die bonding. The first-level connections have to be established; that is known as wire bonding; you can call wire bonding as a first-level interconnection methodology.

Wire bonding is one of the three important first-level connection choices; we are going to see in a short while what the three methods are, but the most common – almost 90 percent – of the first-level interconnections in packages are based on wire bonding. Once the wire bonding is done so…. Basically, if you look at it schematically, there is a die that you have simulated and, for example, these are the bond packs that you are seeing on the die. This requires to be mounted on a substrate; the substrate will also have a bond pad in the periphery. The wire bonding process will take place between the die bond pad and the bond pad on the substrate.

This is the substrate and this is the die (Refer Slide Time: 10:02). You have a very rigid platform called the substrate which will hold the die. Underneath this die here will be an adhesive which holds the die onto the substrate and then the wire bonding takes place using gold, aluminum or copper. We are going to see this particular process in detail shortly. Most of the packages use wire bonding. Once the wire bonding is done, you have to protect the wire bonds; that process is called encapsulation; it basically protects the first-level interconnection that you have done. Finally after the molding…. This is also known as molding; encapsulation is also known as molding.

Once you mold the package with a specified material, it can be plastic or ceramic, finally you do test and burn-in, so that you can qualify each and every individual package before you release it into the market. This completes the back-end process for the die fabrication which includes the packaging part of it. The back-end process becomes important for us because we are going to talk about single-chip manufacture here.

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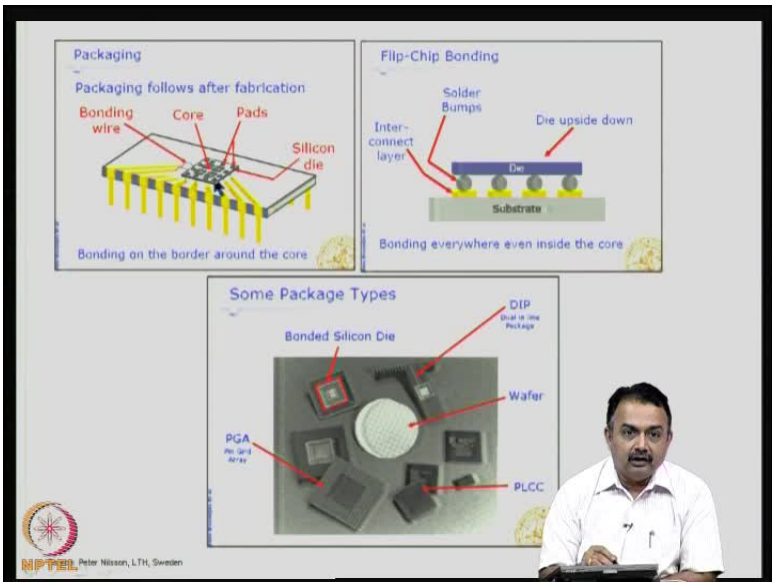

If we look at the slide here, briefly, you can see on the left we have here a substrate (Refer Slide Time: 11:56) – the lead frame – which houses the die that we have manufactured. Here, you can see on the die in the periphery various die bond packs that are marked in black. What you see here are the lead frames which connect to the outside world.

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Typically if you have seen a DIP package here, as you have seen in the previous classes, you can see the lead frame; the black one is the encapsulation. If you rip this open, what

you are basically going to see are the wire bonds. You can see a black bond depicted here (Refer Slide Time: 12:45) from the bond pad of the die to the lead frame.

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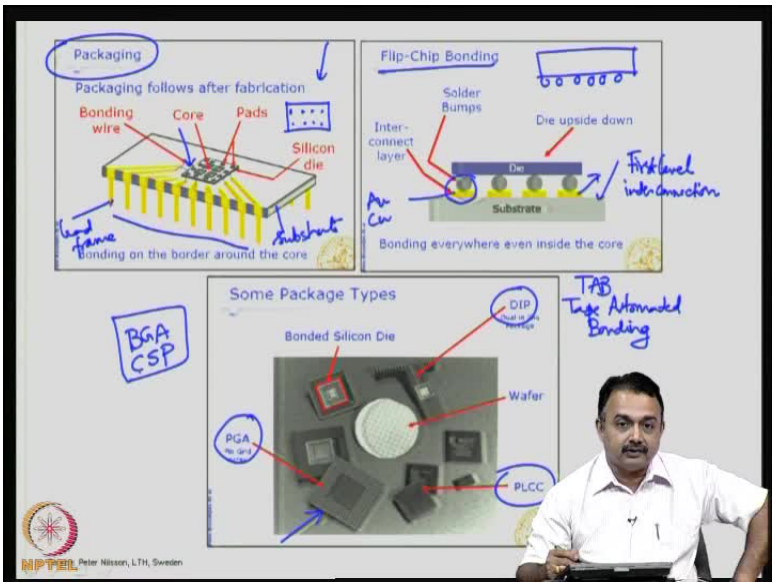

This part is the wire bond, this is the lead frame and you can see this is the substrate (Refer Slide Time: 13:04). This is the lead frame. This is known as peripheral bonding because the bonding takes place on the periphery of the package. The die is positioned at the center of the package on a frame or a substrate; then you have the bond pads visible. This is the core of the die here at the center and then the wire bonding takes place using aluminum or gold. At the periphery, you can see these are the lead frames. This is a very important aspect of packaging the die that has been fabricated. This is one method of packaging a die.

The other method or the current process that we are using today is known as flip-chip bonding. Normally, in this figure, the die is like this and the bond pads are on top – visible. In this flip-chip bonding, you can see this is the die and the bond pads are at the bottom, because we are flipping the chip over; that is why it is known as flip chip bonding.

Basically, you have a substrate and this is the bond pad on the substrate. Then you have the die; the die is upside down. At the bottom of the die, you can see solder bumps; the solder bumps will establish the connection with the substrate. What you see here – the yellow color on the substrate – is the interconnect layer; it can be a normal conductor

like copper or it can be gold; this can be gold or it can be copper. Now, the connection is established between the solder bump and the bond pad on the substrate. This is also known as first-level interconnect or first-level interconnection.

Wire bonding is a first-level interconnection; flip-chip bonding is also a first-level interconnection. There is another method known as TAB; TAB is known as tape automated bonding, which is the third method of first-level interconnection choices that we have. First-level packaging. If you recall the definition that we have looked at in the first chapter, there are three levels of packaging: first level packaging, second-level packaging and the system-level which is the third-level packaging.

In the first-level packaging, studies on these interconnects will be involved including package material, package type, the densities involved and so on. Please remember that we are currently going to look into all the three first-level interconnection choices. What I have described here is a wire bonding process and flip-chip bonding. Once these kind of first-level interconnections are done, you get packages. In the picture below, what you see here, from the wafer you see a DIP package; you see a bonded silicon die onto a substrate; you see a pin grid array here at the bottom and then packages like plastic leaded ceramic chip carriers (PLCC) and so on.

Depending upon the end application, depending upon the number of I/Os or input/output pins that you have designed for a particular package or a die, you can choose the different package formats. It can be a simple DIP package (dual in-line package) or it can be a complicated high-dense pin grid array package; it can be other packages like a ball grid array or it can be a CSP; we have earlier seen definitions or expansions of these terms: ball grid array and chip-size package or chip-scale package.

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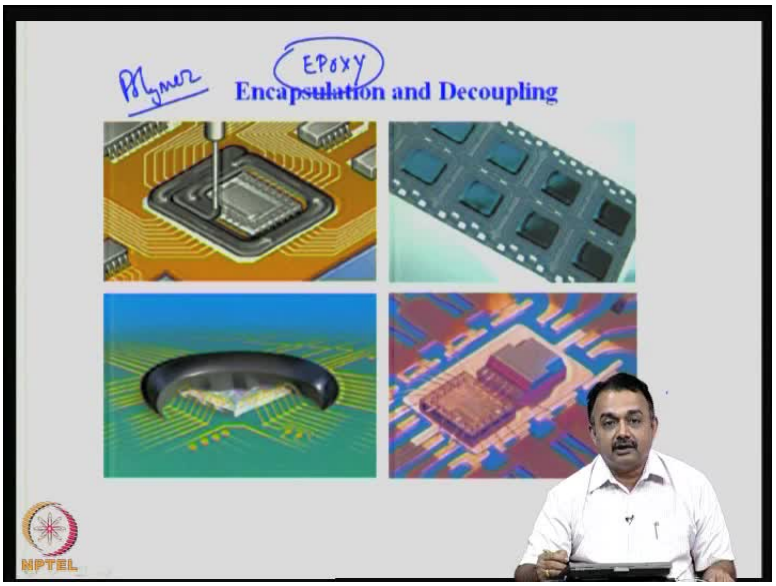

Now, briefly about encapsulation; encapsulation is basically a process of using a polymer material to protect the die from the external environment. What is the external environment we are concerned about? Temperature increase, dust and humidity. The polymer material should be inert; it should protect the wire bonds that you have established or the flip-chip bonding that you have established and protect the die from external influences.

What kind of polymer do we use? Normally, we use a very simple polymer called epoxy which is very widely used. Basically, it is very inert to other chemicals; it absorbs moisture to some extent, but the moisture can be removed by heating it or keeping it in an oven for about 80 degree Centigrade for about 10 to 15 minutes. You have to make sure there are other polymers also that can be used for encapsulation, but if you look at cost, epoxy is the most widely preferred material and 90 percent of the encapsulation process in plastic packaging is done by epoxy.

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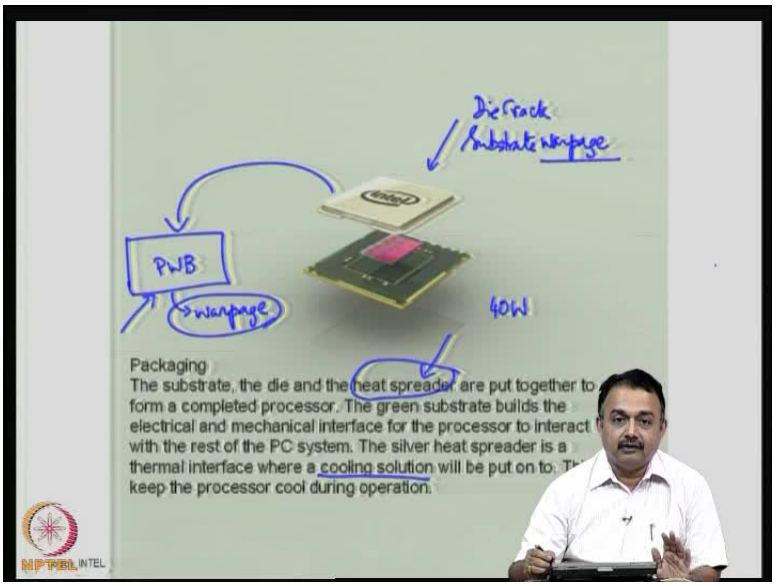

Now, I will continue with the description of the back-end process using some illustrations. As I have told you, these have come to me from Intel who gave permission to use these figures. If you look at it, basically the packaging part of the back-end process involves a substrate; it involves the die; and in some cases you may have to use a heat spreader. Why do we use a heat spreader? All these components together when packaged form a complete processor which is protected and it is ready to use in any motherboard.

For example, an Intel processer like the Core Duo Processor or i7 Processor, whatever it is, now goes into being mounted on a substrate; again, the main processor is interconnected to various other components on the system and then it is powered up. When you power up, heat is dissipated. One of the important concerns for large high-density high pin count processors is what kind of heat you can expect when you power up the circuit – when you power up the board.

In some cases if the chip manufacturer has made a lot of analysis and then comes out with some kind of a figure; let us say, 40 watts is going to be generated from a processor. Do you require a heat spreader to remove the heat quickly? If you do not require a heat spreader, what other mechanisms are going to be available to remove the heat? Can the substrate remove the heat quickly from the surface of the die? These are issues that you have to take care of when you go for packaging.

The substrate will take care of the electrical interconnects; it will also take care of the mechanical interfaces that are required for the processor to interconnect with the rest of the components on the system. Here, I would I like to recollect that the board can perform as a system; the printed wiring board or printed circuit board can be called a system.

The processor will go onto the board and it is interconnected with passives, electromechanical components and so on; it can be a high-dense printed wiring board. Therefore, the presence of a heat spreader on the package is an added advantage because it will provide a lot of relief to the printed wiring board; otherwise, the printed wiring board can experience warpage; it can have physical damages because of heat not being able to be spread quickly to the ((.)).

There are different types of materials that are used for heat spreaders. We will look at it at some other point of time, but the basic question is, or the basic issue here, is a cooling solution has to be thought of when a processor is packaged; this will keep the processor active and it will give longer life for the processor. What are the things that you can expects in terms of failure? There can be die crack or there can be a substrate warpage; warpage means bending due to continuous cooling and heating – expansion and contraction.

These are issues that a packaging engineer will have to take care of when you look at materials that you choose for packaging a die – including the thickness of the heat spreader and the heat spreader material that you are going to use. The heat spreader material can be metallic; it can be a plastic material too; all that is required is a good thermal conductivity that can remove the heat quickly from the surface of the die.

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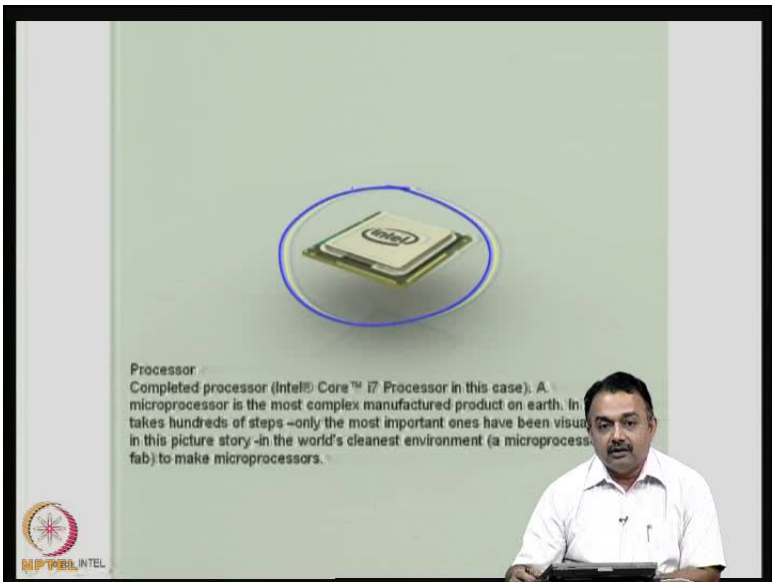

For the processor in this particular example flowchart that we have been seeing over the last two classes, the processor packaging is complete. The illustrations we have seen are very few, but in actual practice there are scores of subprocesses that the wafer has to go through including the back-end packaging, die bonding, wire bonding and so on to make sure that you get a more reliable package.

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Finally, these packages will go for routine electrical test once again, especially in terms of power dissipation and frequency handling. These are electrical tests that will have to be conducted once the die has been packaged; only then it is qualified.

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Then, binning; this is basically a classification of the processors of a particular type into trays that are again well-defined in terms of material choices, shielding and so on because these have to be transported.

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Finally, it is sent for retailing; retail packages are done and this particular processor will then be used for system manufacture by use it will be used by system manufacturers for the specific application that it is intended for. This is an example by Intel for the i7 Processor. Similarly, there are other companies globally that manufacture various microprocessors, microcontrollers and so on that will be used by various customers for different applications; it can be in automotive, it can be in consumer electronics, it can be in communication areas and so on.

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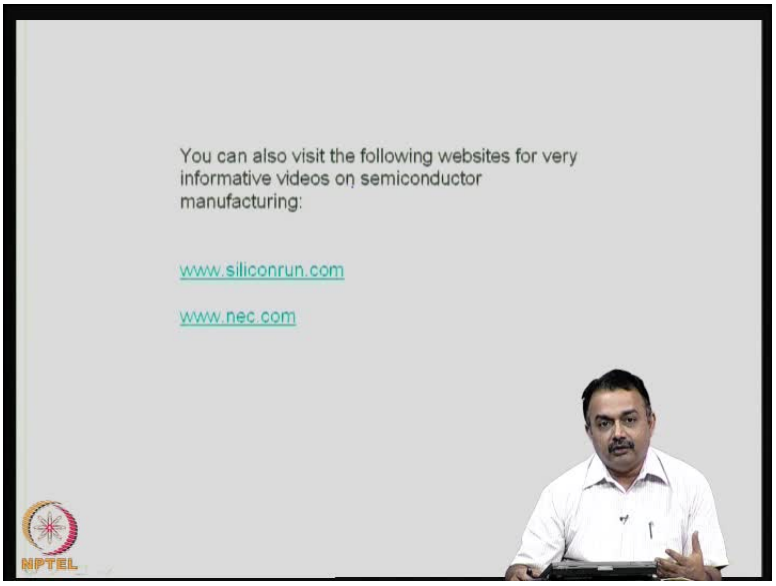

What I have tried to give is a very brief description. You can visit the following Web sites; that is, www.siliconrun.com or www.nec.com for various information on semiconductor manufacturing. You can take up from what I have described here; you can see a lot of informative video highlights that are available for the general public to view.

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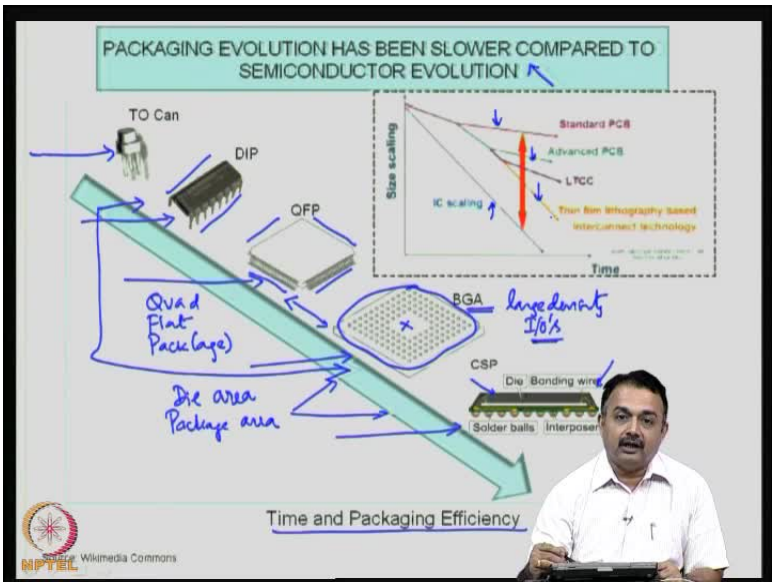

That completes the front-end and back-end process description. Now we will try to look at the first-level interconnection choices. If you look at packaging evolution, it has been slow compared to semiconductor evolution. As I said, semiconductor fabrication does not really come into the ((.)) of packaging. First-level packaging starts with a finished die.

If you look at this time graph, you have time and packaging efficiency here; we started decades earlier with a TO – transistor can; then we started using the DIP packages which were very common; even today we are using DIP packages (DIP means dual-in-line package); then we progressed into quad flat pack; this is known as quad flat pack or package (Refer Slide Time: 27:43).

You can see from the name dual in-line that there are two rows where the lead frames are; so, it is called as dual in-line. In quad flat pack, on four sides the pins are arranged symmetrically; the I/Os are distanced carefully by a well-defined pitch between the lead frames; this is known as the quad flat pack; this also has got a package housing. Today, we are into the world of ball grid arrays.

As you can see, the difference between these two packages is the bonding here is at the periphery in the QFPs, whereas in the ball grid arrays you can see the input/output pins occupy the entire area – almost entire area of the die – except at the center which is

probably used for heat dispassion. So, directly under the die you really do not have to mount the I/O pins, but effectively and theoretically you can even utilize those areas.

Here, you can expect large density – large I/Os. As I mentioned in one of the slides earlier, BGA is the workhorse of the industry today; more and more designs are being converted into ball grid arrays because you can look at it ((.)) from the DIP package to the ball grid array. This is a very large package (DIP package), whereas the ball grid array package is definitely smaller in size; at the same time in terms of performance, you can expect more reliable performance electrically and thermally.

We are now again looking at new packages called chip-size packages or chip-scale packages. The difference between BGA and CSP is basically in the package area. If you take two terms called the die area and then package area, in a BGA the package area is slightly larger than the die area, but in a CSP the package area and the die area are almost the same – it is only a question of 20 percent difference, whereas in BGA it can be more than 20 percent. If you have a package in which the package area is almost the same size of the die area, then it is called a CSP.

You can look at the cross-section of the CSP here; you have a die; then you have the solder ball interconnections at the bottom; the white area is the die where it is connected to the bond pad of the substrate by wire bonding (Refer Slide Time: 31:00); then it is packaged. There is a package, but the package volume is very small. That makes it more reliable in terms of electrical performance and the profile or the thickness of the package is fairly small. Today, we are in the world of BGA and CSPs.

If you look at the figure at the top, the reason for this statement which I have written here that packaging evolution is slower compared to semiconductor evolution is because the IC scaling is very large compared to the standard PCB production because PCB is a substrate for the second-level packaging that we are talking about. There is a large gap between standard PCB and IC manufacturing, but today advanced PCB techniques have narrowed down the gap in terms of better photolithography and so on. If you look at thin-film lithography used on ceramic substrates or organic substrates, it can probably still reduce the gap between IC scaling and second-level packaging.

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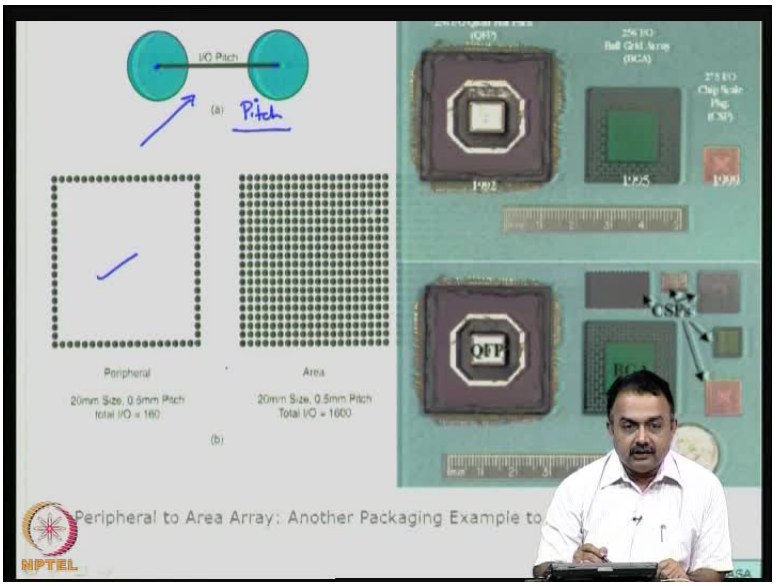

This figure will give you some idea about the utilization of the area under the die. Firstly, if you look at this figure the top, I have defined what a pitch is – input/output pitch (I/O pitch) (Refer Slide Time: 32:42). If this is the center point of a bond pad or an I/O and here again this is the center point of the adjacent pin, the distance between the midpoint of the first and the second – the distance between these two – is known as the pitch. The pitch will give you very good information about the sizes; the pitch also relates the assembly techniques that you need to use; it also indicates the capability of handling these packages.

If you look at this figure here, this indicates the I/O pins at the periphery of the package; all around, you can see that the I/O pins are arranged at the periphery (Refer Slide Time: 33:42); the center of the package is not utilized. A typical example for this will be your quad flat pack. As an example here, if this is 20 mm size with a pitch of 0.5 mm, that means the distance between this and this midpoint is 0.5 mm or 500 microns, then the total I/O possible here will be 160 pins or I/Os (Refer Slide Time: 34:06).

The same thing happens with area array packaging. If you theoretically utilize the entire area under the die, not just the periphery but the entire area under the die with the same 500 micron pitch or 0.5 mm pitch and the same size – 20 mm size, you can actually get 1600 I/Os, but practically it may not possible to get 1600, because ideally you would like to have a staggered arrangement of I/Os for various purposes including electrical and

thermal performance – better performance. This is known as area array packaging; this is the configuration you will see in area array packages, typically in a BGA or a CSP (Refer Slide Time: 35:05).

The photographs alongside here will give you a quick idea or illustration about the sizes that we are seeing over the years; this picture is courtesy of NASA. For example, in 1992, a 256-pin quad flat pack – you can see the size; the same 256 I/O can be generated in a ball grid array – 1995; see the size – different shrinkage; and chip size – 275 I/O (Refer Slide Time: 35:41). You can see a dramatic decrease in the size of the package itself; also, you can expect that the pitches in CSP will be much smaller compared to a BGA and then compared to a QFP. This is again another illustration about various small-format CSPs that are available in the market today (Refer Slide Time: 36:08).

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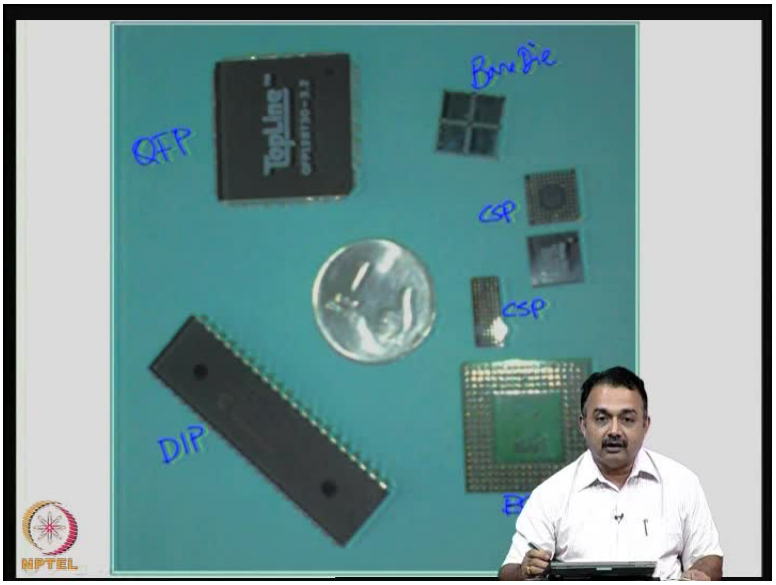

These components I have in my previous class tried to show you, but I have tried to put together here one single picture where you can compare it with our one rupee coin. This is our DIP package. This is the DIP package; then you have the QFP; then this is the BGA – ball grid array; this is CSP; these are the two sides – the bottom side and the top side of a CSP; this is a bare die.

You get a very good idea about shrinkage in sizes, but at the same time shrinkage means high density, high performance and sometimes vertical integration in terms of number of layers of interconnects. These are all the features of the package at the board level. From

the first level, we are trying to see how we are integrating these devices at the board level to make it a high-density interconnect structure.

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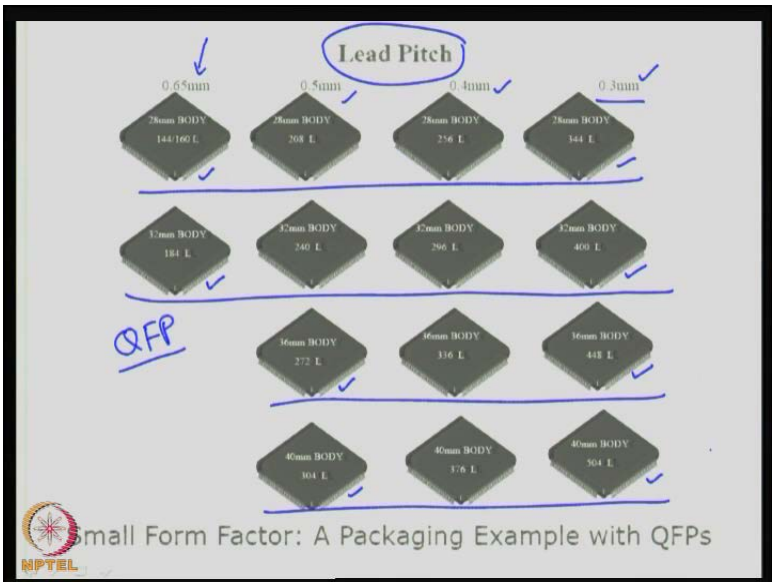

Another example I would like to give you to impress upon you about the packaging evolution and sizes. You should always get a feel about lead pitch; once you get a feel about the sizes and the number of lead pitch, you will be able to appreciate technologies that are being used at the board level. Pitches are also very important at the chip level, because you need to understand what pitches are available at the die level.

For example, this is a quad flat pack structure format. If you look at the pitch, this is 0.65 mm pitch, then 0.5, 0.4 and 0.3 (Refer Slide Time: 38:21). 0.3 is probably the smallest of the maximum reduction possible today with QFPs. If you look at the 28 mm body size that is being used for each of these here, you can see the pin counts have increased from 144 to 344; so, reduction in pitch means you can handle more I/Os.

Similarly, with the 0.65 mm and 32 mm body, these are all 32 mm square bodies, we move from 184 leads to almost 400 pin count (Refer Slide Time: 39:05). Similarly, with 36 mm in 0.5 to 36 mm in 0.3, we are moving from 272 to 448 and with 40 mm package in 0.5 to 0.3, 304 to 504. This has been illustrated here basically to give you an impression about the impact – the impact of lead pitches on packages of a similar type.

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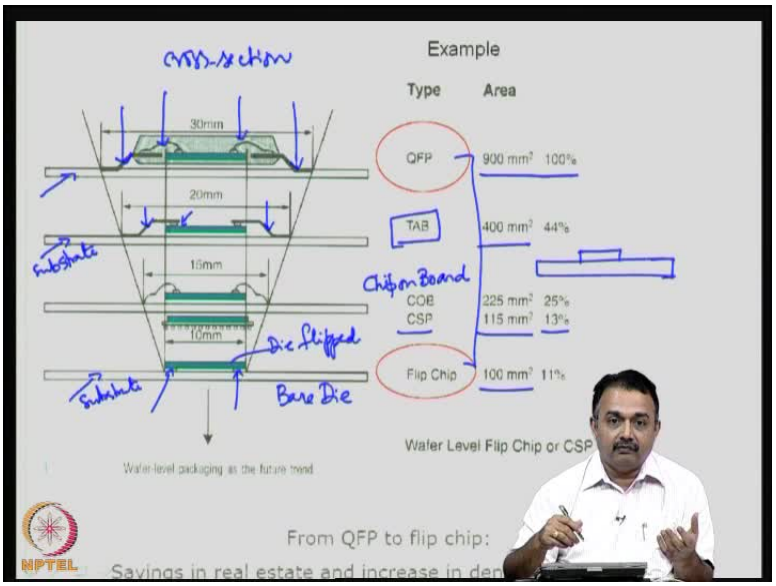

You can expect that in different package formats the impact will be much larger. For example, if you look at a QFP with an area of 900 mm square (this is the starting point for us and so 100 percent), you can see here in this picture that this is the substrate. These are the lead frames of the QFP package – the black ones; this is the package body; inner, you can see here the wire bonds (Refer Slide Time: 40:14). This is the quad flat pack cross-section; what you are seeing here is a cross-section of packages.

If we move from quad flat pack to a package type known as tape automated bonding, here you can see that the package volume has reduced – the height has reduced. You can see the first-level interconnect here; this is the bond pad at the die level; this is the substrate (Refer Slide Time: 40:54). You can see that the area is reduced to 400 mm square – 44 percent from 100 percent, if that is the standard.

Then, other techniques like chip on board (COB stands for chip on board); we are going to see what is a chip on board). What we are trying to say is a bare chip mounted on a printed wiring board is chip on board. If you take an organic substrate like this, you try to assemble a bare die without packaging (Refer Slide Time: 41:29) or a CSP which is close to being called a bare die, but it has got some amount of package material; so, we move down to 115 mm square; it is now 13 percent.

Then, we talk about flip chip; flip chip is nothing but a bare die which does not require packaging material to be used; you can see that the die here is flipped. The

interconnections are at the bottom; this is your substrate (Refer Slide Time: 42:09). When the interconnections are done at the bottom, you really do not require encapsulation at the top, whereas at the top figure QFP you require encapsulation to protect your very thin wire bonds.

From a QFP right down to your bare die, you can see we have moved from 900 mm square to 100 mm square – almost 89 percent reduction in area. This gives you an example about the size reduction, savings in real estate and different form factors for the same application; it can provide beneficial to be used in reducing your board area, increasing the wiring density and connection density and increasing the number of I/Os.

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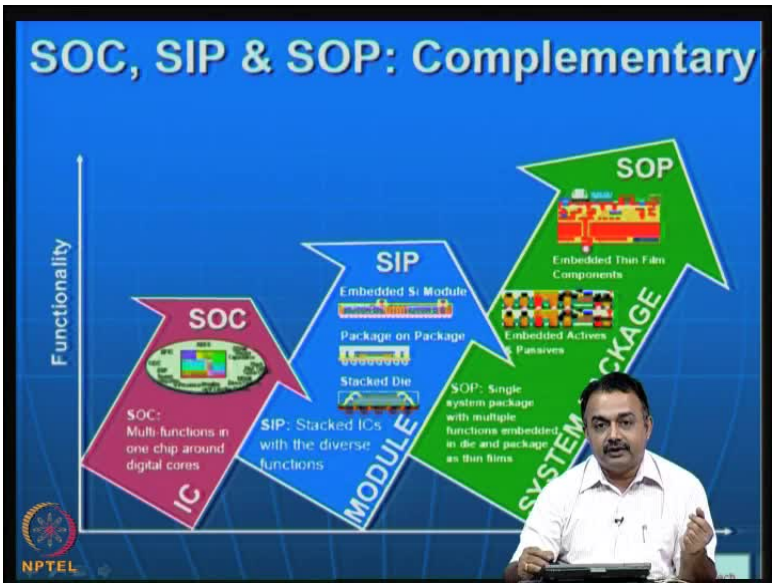

These three terms I think we have mentioned: system on a chip, system in package, and system on package; they are complementary to each other. System on chip means built-in functions – multi-functions – in one chip around digital cores. System in package means you can have different ICs from different vendors; they can be grouped together on a single substrate stacked and interconnected by means of wire bond or flip chip and then they are packaged.

Now, it behaves as a single package, but effectively you have used different functional dies. One can be an EPROM; one can be a cache; another one can be a memory or a controller codec (whatever it is). You can have three or four dies grouped together on a single substrate. In system on package, basically we are talking about multi-functions

embedded in a die and packaged as thin films on organic substrates; this is typically talking about, the third one talks about, system-level packaging.

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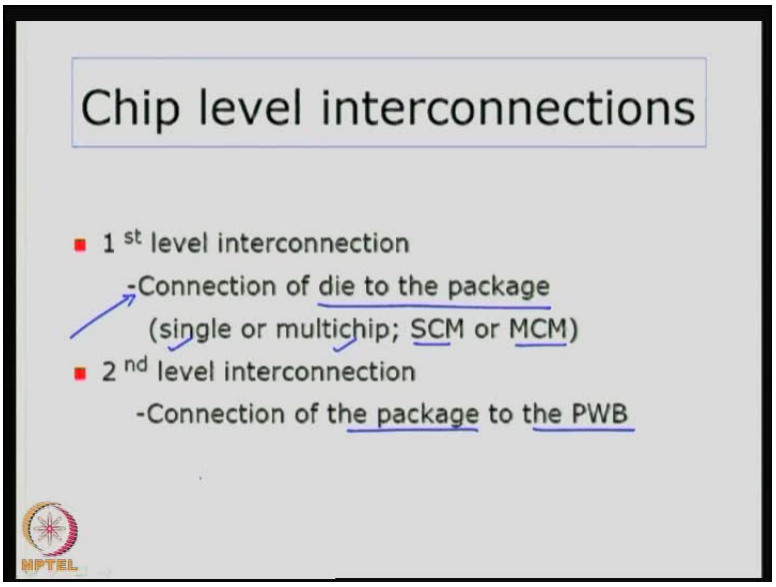

We will move into some details on chip-level interconnects or first-level interconnections. The first-level interconnections – now you have got a better idea – talks about connection of the die to the package. Basically, we have to look at how you can connect the bond pads of the die to the package substrate. As a result of the first-level interconnection, you will get either a single-chip module or a multichip module (SCM or MCM); SCM stands for a single-chip module and MCM stands for multichip module. The second-level interconnection talks about connection of the package to the printed wiring board. Basically, QFP or a DIP package or a BGA, as you know, all of these are single-chip packages.

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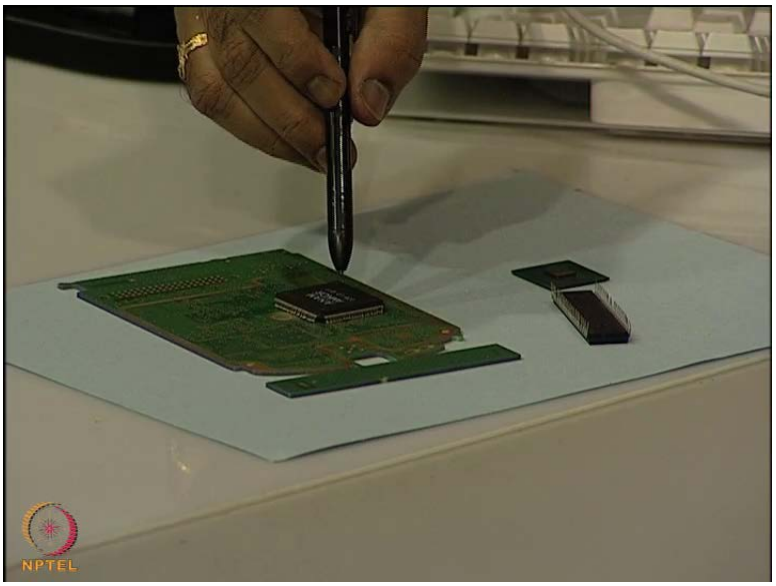

Now, we are going to use a printed wiring board like this and try to see how we can establish a connection from the first-level package to the second level. Connections on this board are known as second-level interconnections (Refer Slide Time: 45:45); connections here are known as first-level interconnections; I hope it is clear.

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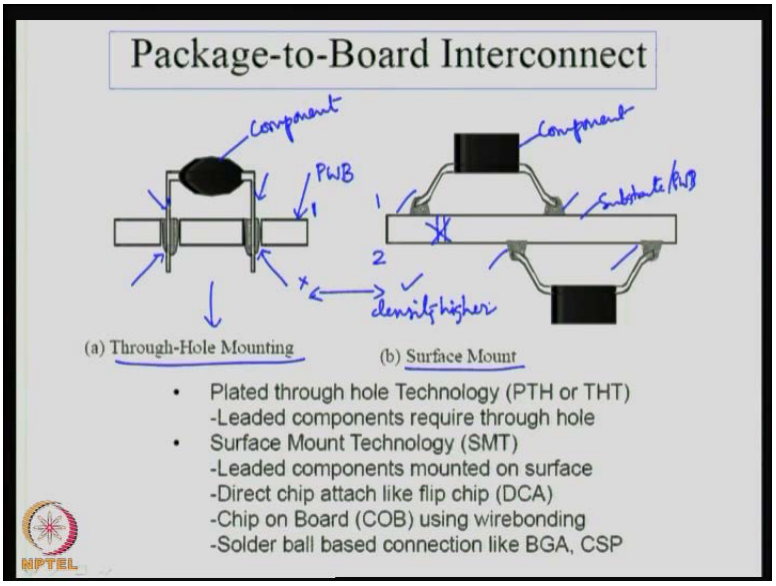

If you look at Package-to-Board Interconnect, basically this is second-level interconnect. If you look at this figure, this is your printed wiring board and this is your component – the package (Refer Slide Time: 46:09). These are known as through-hole packages. This

component has leads which are very long and these need to be inserted through the holes present in the printed wiring board; so, these interconnection choices are known as through-hole mounting interconnects.

The second one is known as surface-mounted interconnect where the component is mounted on the surface of the substrate, as the name indicates; this is the substrate or you can call it as printed wiring board (Refer Slide Time: 46:48). It does not require a through-hole connection; the connection is done on the surface; the components can be assembled on both sides of the board – the first layer as well as the second layer, whereas, here typically, you can do it on only on the first layer. This itself indicates that the board density is going to be very high here compared to this one (Refer Slide Time: 47:23).

Plated through-hole technology known as PTH or through-hole technology requires leaded components and they require through holes on the substrates. In surface mount technology, leaded components are mounted on the substrate; direct chip attach components like your bare die or flip chip can be mounted on the substrate; chip on board (that is, a bare die with its face upside face up on the substrate) requires wire bonding to be done on the substrate; solder ball connection is done for BGA and CSP; these BGA and CSP components can be mounted onto the substrate.

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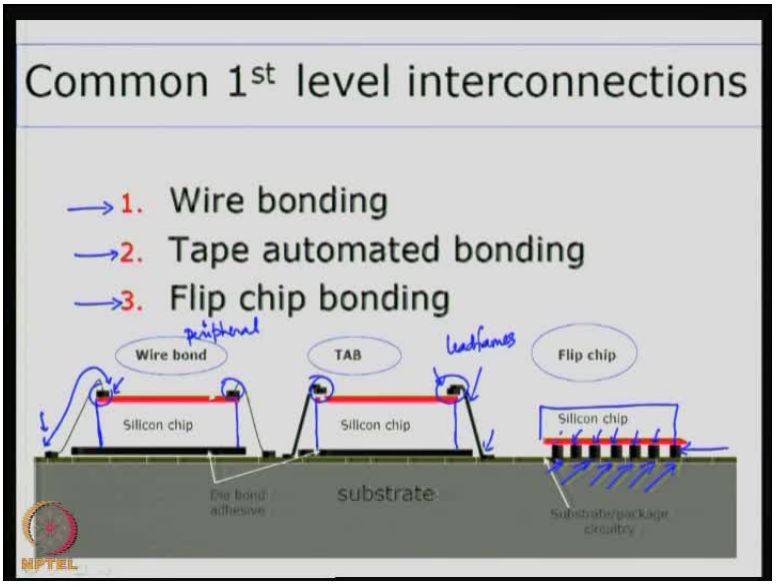

The common first-level interconnections are wire bonding, tape automated bonding and flip chip bonding; these are the only three first-level interconnections. If you look at the first figure here, this is the substrate – common substrate – assumed for describing all the three processes. Wire bonding contains a silicon chip like this – a bare die (Refer Slide Time: 48:42); that is now mounted onto this substrate here; then you have the wire bond; the wire is drawn like this from the bond pad of the die to the bond pad on the substrate.

This is basically done on the periphery; this is the cross-sectional figure. You can imagine that you can have n number of pins at the periphery. In the second example which is tape automated bonding, you have a silicon die or a silicon chip mounted onto a substrate. Instead of a wire bond here, you have thin lead frames, very thin lead frames, which represent the typical wire bonding process; these are connected via bonding at the top and a bonding on the substrate; this will again describe to you the peripheral bonding in the package.

The third one is a bare die like a silicon chip here; this is known as flip chip; the chip is flipped over. As you can see here, in wire bond and TAB the bond pads are at the top, whereas in the flip chip the bond pads are at the bottom; that is why it is known as flip chip. The connections are established by registering perfectly the bond pads on the die with the bond pads that you have to generate on the substrate; interconnection is established in this way. These are the three methods; two of them are of a similar type in the sense that the die bond pads are facing up; in flip chip, the die bond pads are face down; this is the basic difference between the three connection choices.

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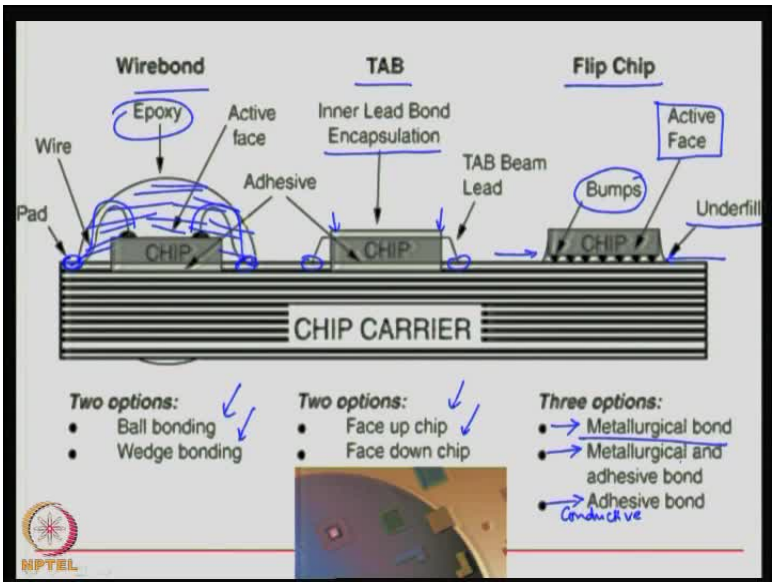

This is a much better figure where you can see the chip in all the three cases: wire bond, TAB, and flip chip. We call these interconnects for the flip chip as bumps; bumps will be created on the flip chip die, so that they can register with the bond pads on the substrate; these are known as direct chip attach method or a flip chip methodology. You can see in flip chip, the active face is down; in the wire bond method, the active face is on top; the wire bonding is done here like this (Refer Slide Time: 51:50).

Then, you can see that it requires a bond pad on the substrate, so that it can establish a connection and similarly here for TAB. Then after the wire bonding is done, you see that the wire bonds are protected with an epoxy polymeric material. This encapsulation process will take care of protecting your first-level interconnects – epoxy encapsulation. In the second also, once the leads are connected to the substrate, we also encapsulate the chip, but in this case the encapsulation is done only for the inner leads; the inner leads are present here (Refer Slide Time: 52:41); the outer leads are on the substrate; this is the minor difference between wire bonding encapsulation and tape automated bonding encapsulation.

In a flip chip, you typically do not have an encapsulation; as you can see in this figure, there is no encapsulation process, but we use a process called underfill technology which is to protect the die. As you can see here, there is a small gap between the die and the substrate where the bumps are present. This area between the die and the substrate has to

be covered; that is the only area that is open. You can use a process called underfilling to protect or fill up that area so that the entire die and the substrate together in unison are protected.

These are the encapsulation or protection methods used for wire bond, TAB, and flip chip. There are two options in wire bonding: one is known as ball bonding and the other is wedge bonding. There are two options of placing your chip: one can be face up and the other can be face down. There are three options of bonding in terms of how you establish the basic solder connection or wire bonding; it can be a metallurgical bond; it can be a combination of metallurgical and adhesive bond; it can be an adhesive bond. You can have conductive adhesives used to make electrical interconnections or you can do a simple metallurgical bond – bonding two metal surfaces using high temperature or pressure – and then establish an electrical interconnection.

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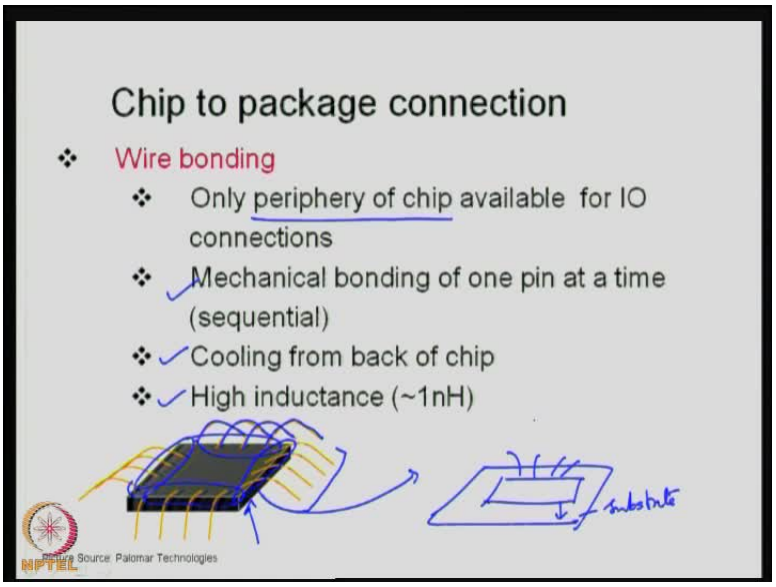

Chip to package connection in the case of wire bonding. I hope you are very clear about terms like periphery of chip is available for I/O interconnections in the case of wire bonding. I think this figure will give you the clear difference. You can see that only the periphery of die is used; like in the case of a QFP, wire bonding is done in the periphery. This wire bonding process involves mechanical bonding of one pin at a time; it is a sequential process; it is not a parallel process of bonding all the bond pads at the same time. The equipment that is used for wire bonding will bond one pin at a time; the first

bonding will take place and the second will take place, but it has to happen at high speed; today, equipments are available to wire bond at a very high speed with high reliability.

The cooling of the device will take place from the back of the chip; that means when you mount this area onto a substrate… Suppose this is the substrate and this is your die and here the wire bonding takes place, the die surface that is attached to the substrate will transfer the heat to the substrate quickly; therefore, the substrate has to take care of the heat dissipation. There is a reasonable length for the wires; so, it has got high inductance around 1 nanohenry.

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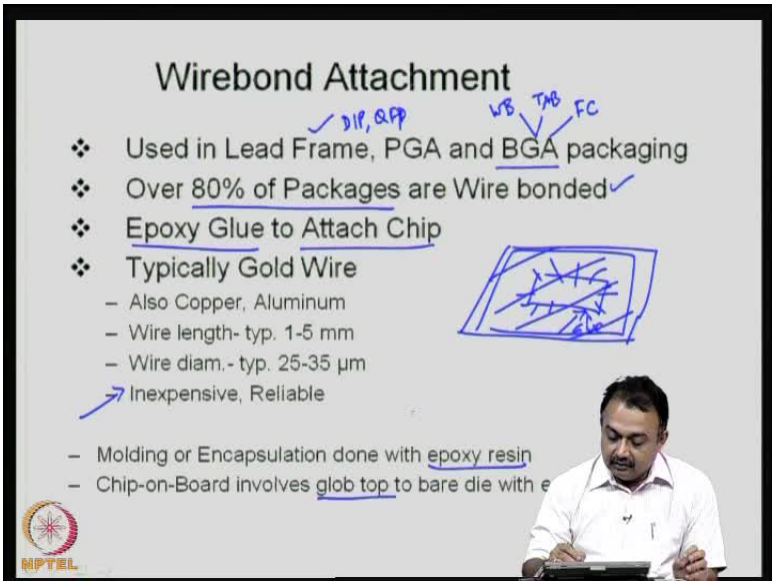

Wire bonding is used in the case of lead frame packages; for example, DIP packages, QFP packages and so on; it is also used for PGA packages – pin grid array; in some cases earlier, it has been used for BGA packages, but if you use BGA and wire bond, obviously, the height will be more compared to using flip chip. You can use wire bond or you can use TAB or you can use flip chip for BGA packaging, but over 80 percent or 85 percent of the packages are wire bonded because it is less expensive, more economical, the methodology is well-established, the equipments are well known and you can get a high reliability and yield or throughput. Yield and throughput are two different terms; from the equipment point of view we want high throughput, but process-wise we want high yield in terms of less defects.

Epoxy glue is used to attach this chip onto the substrate. As you know, if you take a substrate, the first process of bonding the die to the substrate is by using glue; only then the wire bonding takes place; after that comes the encapsulation. Typically, gold wire is used; copper and aluminum are also used today. The wire length is typically 1 to 5 mm; the wire diameter is typically 25 to 35 microns; it depends on the spacing available for you to do that.

If you are going to use it ((.)) chip-on-board, then you might have more space; therefore, you can use a thicker wire, but again electrical considerations are more important in choosing the thickness of the wires. Ideally, it is a very inexpensive, reliable and well-known process. As I said before, after the wire bonding is done, molding or encapsulation is done with epoxy resin – the most common resin material that is used to encapsulate. Chip on board involves using a process known as glob top.

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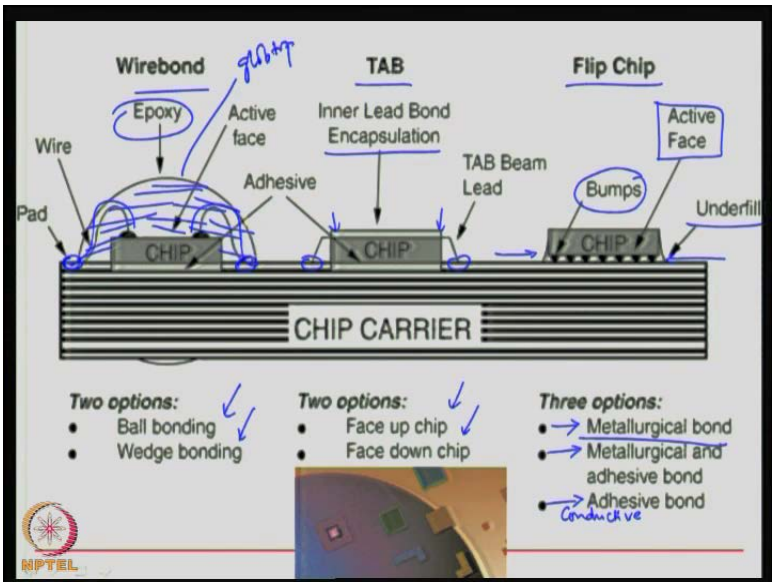

As I said in the previous figure, this is known as a glob top. This process here, what we have seen, is known as a glob top process. We use a glob top to bare die with epoxy resin (Refer Slide Time: 59:19).

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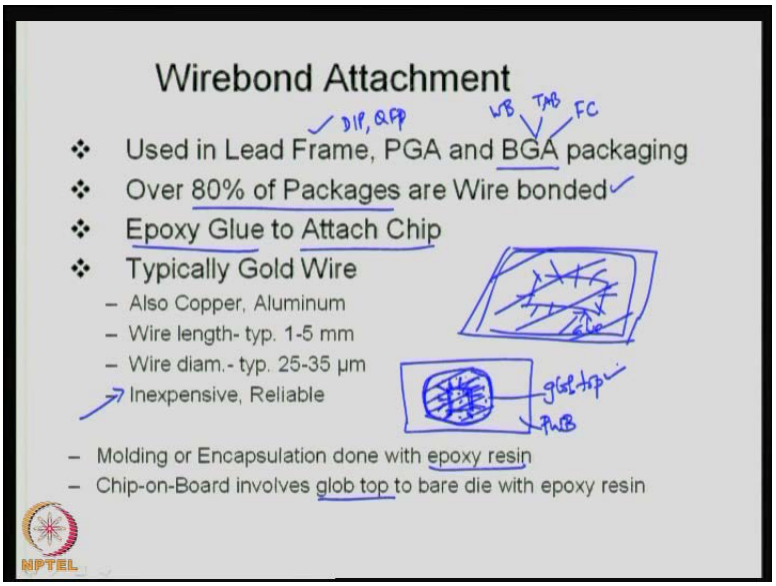

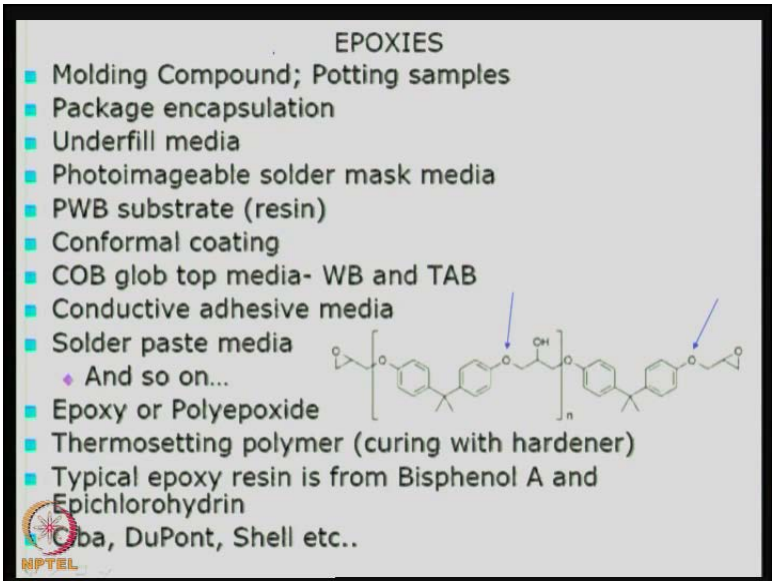

Wire bonding is considered more economical. The advantage of using wire bond is that if you are going use a printed circuit board and if you use a bare die and if there are bond pads on the die, you can create bond pads on the organic substrate, you do a wire bonding using a wire bonding equipment and then put a glob top. If you look at the chip-on-board activity, what basically can be done is if you have printed wiring board and then you have the die placed here; the bond pads are present on the die; the bond pads on the substrate will establish the first-level interconnects.

Once that is done, you pour a globule of epoxy resin on top and protect the die along with the wire bonds. This is known as glob top; glob top is done with epoxy resin which

is the most economical method. In the next class, we will see about epoxy material; we will also look at the other two interconnection choices at the first level.