An Introduction to Electronics Systems Packaging

Prof. G.V.Mahesh

Department of Electronic Systems Engineering

Indian Institute of Science, Bangalore

Module No. 02

Lecture No. 07

Wafer fabrication, inspection and testing

Welcome back. This is another session of chapter 2, which deals with semiconductor packaging.

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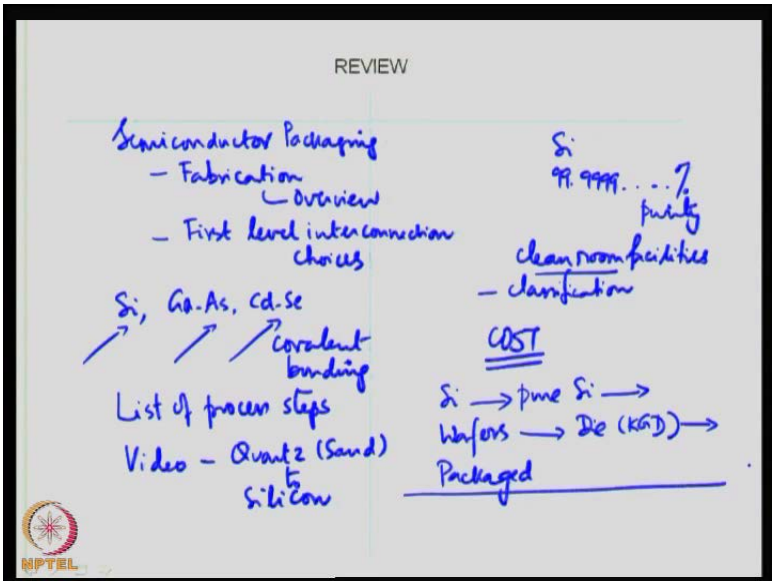

As I mentioned earlier, in this, we are going to look at semiconductor fabrication. That will be a very quick overview. Then briefly, we will see the first level interconnection choices.

In the last class, we basically touched upon the fundamentals of the building blocks of semiconductors. We talked about silicon and we talked about some compound

semiconductors like gallium arsenide and other compound semiconductors like cadmium selenide and so on. Now, we also saw the crystal structure of silicon and how bonding takes place in compound semiconductors by covalent bonding.

We also listed the process steps for the fabrication of semiconductors; and we also finally looked at the video, which really talked about the major challenge of converting quartz or sand to silicon. Now here, we are talking about silicon that is electronic grade purity and we are talking about 99.999999999 percentage of purity; and we also talked briefly about the environment in the manufacturing setup, especially with regard to clean room facilities.

I hope you can remember that we talked about various classifications for clean room, like class 1, class 10, class 100, class 1000 and class 10000 and what each of it denotes. For example class 1 would denote 1 particle per cubic feet having a particle size of around 0.5 microns; so you can expect the level of cleanliness, when we talk about semiconductor fabrication or manufacturing. We also briefly touched upon cost issues, because setting up a wafer fab is going to be expensive and therefore, apart from the expense of setting up the fab, we also emphasized the cost of maintenance, especially as far as the clean room is concerned.

That video was very short clip and which quickly took us from basic sand material to a wafer, and how a wafer is singulated into a basic die, and how it is packaged. The process flow is basically starting from silicon to formation of pure electronic grade silicon, then from there it goes to formation of wafers, and from there, formation of die and this is basically known as a known-good die, and from there, the die is packaged.

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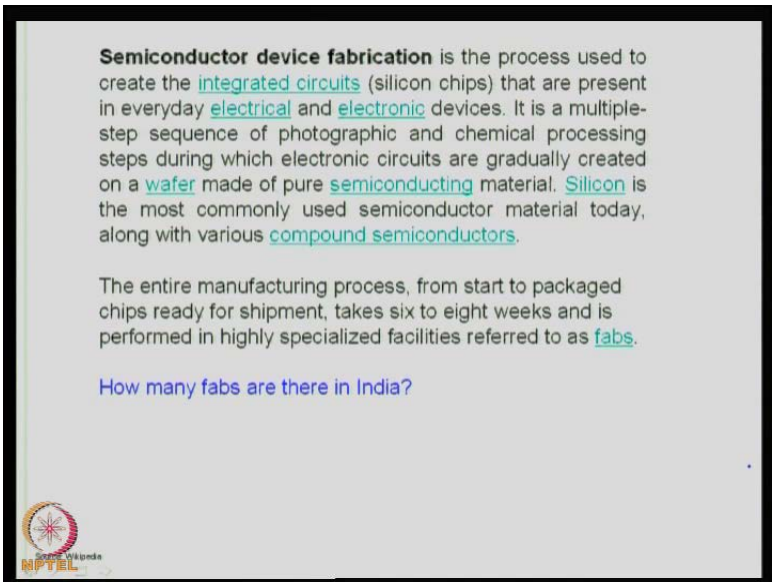

This can be a package containing an IC, which is a microprocessor, microcontroller, a power device and so on. This is the path flow for the semiconductor manufacturing, including packaging. Today, I will take you through a series of photographs that will illustrate what we have been discussing since the last class. Initially, let us describe in a few words, what is semiconductor fabrication? As you can see here, listed in the slide, semiconductor device fabrication is the process used to create integrated circuits; silicon chips, microchips or active devices as you can call them; that are present in everyday electrical and electronic devices.

It is a multiple step process or a sequence of photographic, followed by chemical processing steps during which process, the electronic circuits are gradually created on a wafer, made of pure semiconducting material, it can be silicon or it can be compound semiconductors also; but, silicon is the most commonly used semiconductor material today along with various compound semiconductors.

The requirement of compound semiconductors will arise when you want better electron mobility and for various other electrical properties that you may require for a particular microprocessor. There is also a case of ease of fabrication when use compound semiconductors or silicon and also based on your CAD design, how many layers of interconnect conductive material we are going to generate and interconnect between the layers. The entire manufacturing process from start to packaged chips, ready for

shipment, takes about six to eight weeks. That is a long process and each process, as I have emphasized, goes through quality control check and batch-wise, they are specifically check for electrical test and functionalities.

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These are performed in highly specialized facilities referred to as fabs. Now question to all of us is, many of you may not be aware, how many fabs are there in India? Do we have fabs at all? If so, how many fabs are there? In India, we have specifically semiconductor complex in Chandigarh, which is one of the oldest manufacturing units for semiconductor fabs in India and we have other centers like the DRDO, Indian Space Research Organization and Bharath Electronics Limited. They have facilities that are limited, but at the same time some of them are state of the art.

There may not be volumes manufactured here, more could be prototyping facilities for research; and semiconductor complex is a volume manufacturing unit. This is the information about what we have in India regarding semiconductor fabrication units.

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Now, from this photograph, I will begin listing you or describing you the various process sequences; what you saw in the video is a very short clip; it is very difficult to quickly digest what has gone through the entire sequence. Here, I will list one by one, so that it becomes very clear to you, without any question or without any doubt in the manufacturing steps. I think any packaging engineer needs to know about this because finally, you are going to handle bare dies and then package it.

Now, the starting material is sand; with about 25 percentage of mass, silicon is the second most common element in the earth crust after Oxygen. Sand; and you can call it quartz material, has a high percentage of silicon in the form of silicon dioxide, and is the base or the basic ingredient for semiconductor manufacturing. We are going to start with silicon dioxide that is present in quartz.

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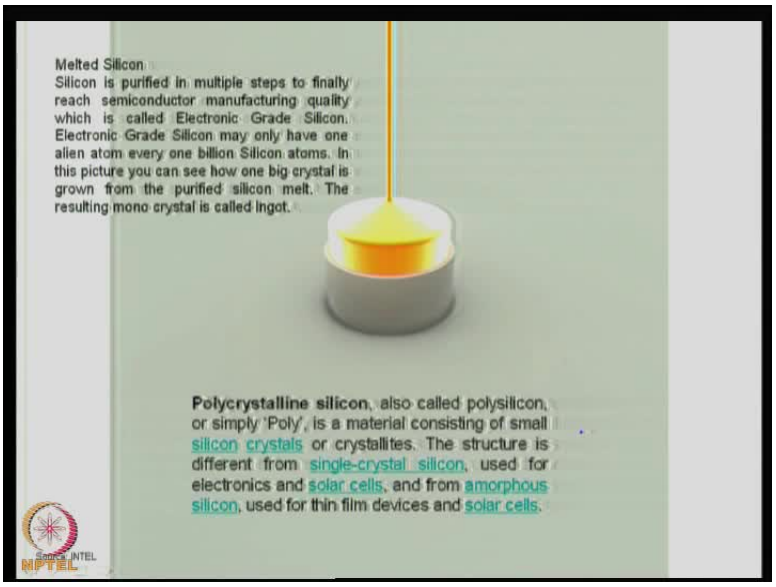

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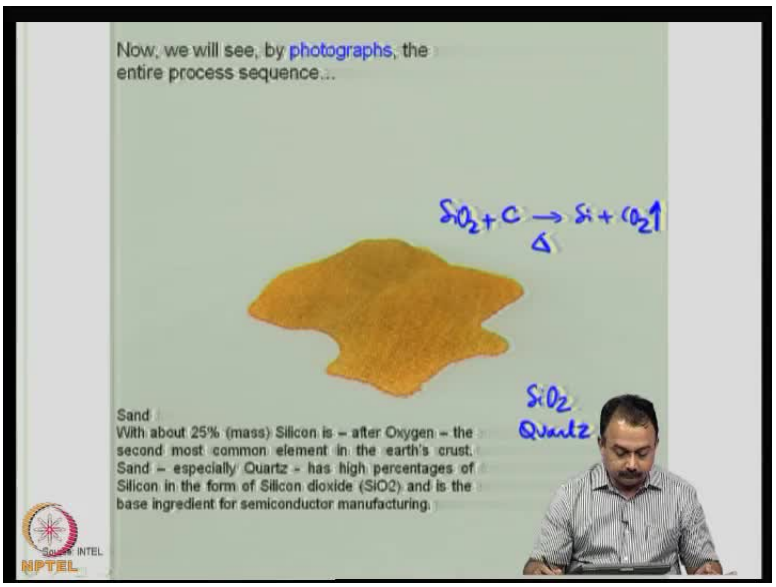

Now, how do you convert silicon dioxide to silicon?; that is the first step, right? Typically, silicon dioxide is made to react with carbon and this forms silicon plus carbon dioxide. This is the basic reaction and this happens as at higher temperatures. So, you get the first step of the formation of silicon.

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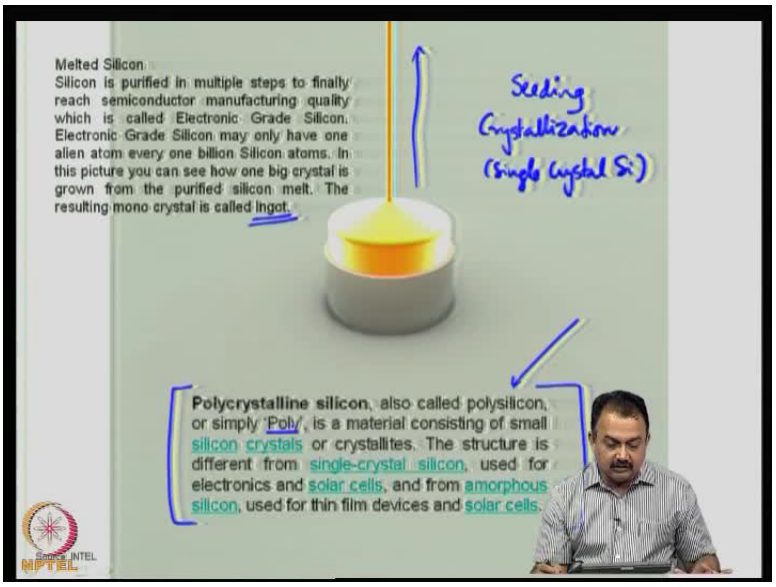

After the silicon is formed, now, you have to make it more pure, that means you want to make it electronic grade silicon; electronic grade silicon is the highest purity that you can achieve; there are other grades of materials or metals or elements or compounds that are available; you call them as lab reagent, analytical reagent and then comes the electronic grade material. In this case, silicon is purified by multiple steps, to finally reach a state called the electronic grade silicon, and that can be used in the semiconductor manufacturing arena.

You have to a do high temperature melting and now, the idea is to create one big single crystal from the molten silicon that you are processing at high temperatures. Here, if you can see this picture what you're trying to do is a seeding process for crystallization. Because, basically you want to create a single crystal, a large single crystal of silicon. The electronic grade material, after it has been recrystallized number of times from a lower grade, until it has reached 99.999999999 percent purity, you try to melt it; then introduce a very pure crystal of silicon that is again of the equivalent terms in percentage purity, then allow with cool slowly. Basically, there is a container in which it is molten and then there is a seed crystal and then you slowly drag it out. Then you get what is known as a monocrystal called ingot; these are known as silicon ingots. This is the first step. Now, I want it to understand some other terms that may be used in the silicon manufacturing or design scenario as well. You will also come across term called polycrystalline silicon, also called polysilicon or simply poly that is a material consisting

of small single crystals or crystallites of silicon. The structure of this is different from that of a single crystal silicon that you are seeing here in a picture above.

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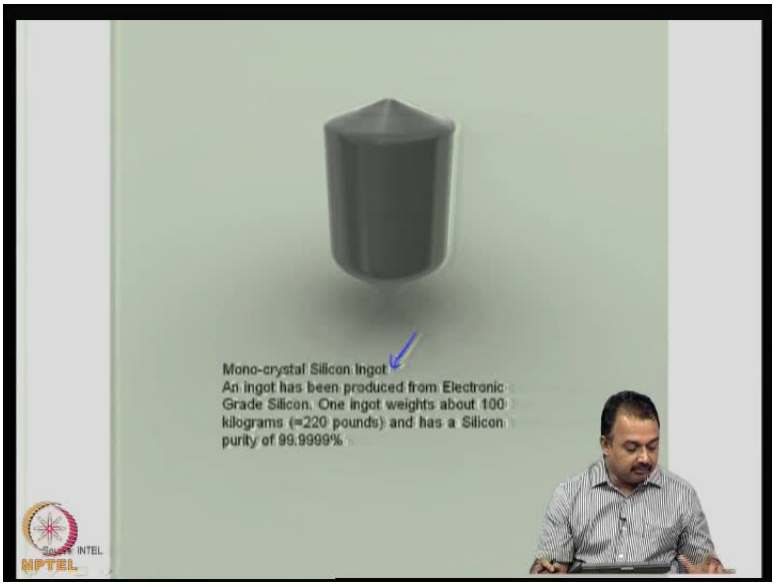

Now, this single crystal silicon is used for electronics purposes and solar cells; and they are different from the amorphous silicon; these are used for thin film devices and also for solar cells. The polysilicon is used as a special material for building up the layers in the device, during the fabrication; you call it as poly. This is the first step to get what is known as a ingot. You can see in this picture; here, this is a very good example of a mono-crystal silicon ingot material that was molted and then slowly cooled to get a single crystal silicon ingot. Now, this ingot has been produced from electronic grade silicon. The properties: typically, one ingot weights about 100 kilograms and has a silicon purity of 99.99 percent. In some cases, we have seen the these silicon ingots are very huge, as big as 1 meter. This is a very heavy block of pure silicon material which will be the starting point for the wafer fabrication.

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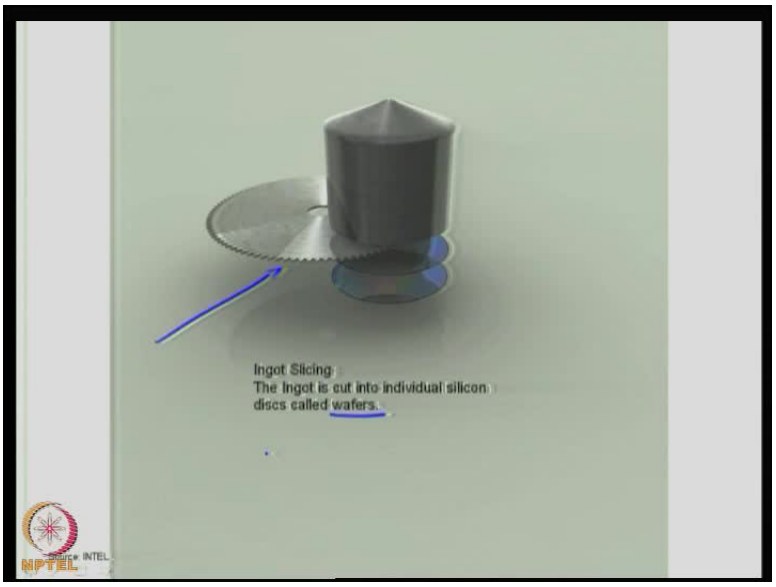

Now, the next step is we have to slice this ingots into individual silicon discs called wafers; that is a next process.

As you can see here, what you are seeing is a wafer; typically, this is about less than 1 mm thick, and today's process requires wafer in the diameter range of 300 mm to 450 mm. So, basically the ingots will also we prepared with those diameters and then using a very good dicing process, this ingot is sliced into wafers. Now initially, the wafer will be very thick and it is on those wafers that you will build the dice; and finally, they will be polished to a very thin wafer, because finally, you do not want too much of unused silicon on the transistor. Therefore, after the imaging and after the buildup is completed, at the back end of the die polishing will take place, so that you can reduce the thickness of the wafer. Right now, it will be a very rigid.

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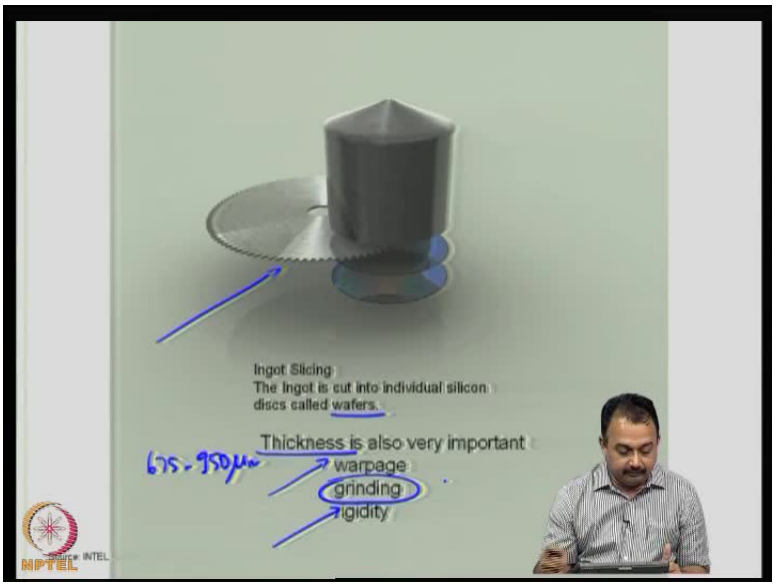

Thickness initially, is very important because, if you start with a very thin wafer, during the process there can be warpage; in some cases, the dice that you have generated can undergo some dimension change because of continuous warpage; or your photolithography will not be exemplary. Therefore, the starting thickness, typically the recommended thickness will be around 675 to around 950 or 975 micrometers or microns. So, warpage is very important; rigidity is very important; all of these are very important for process because the wafer, in lots of 25, will go through various chemical and mechanical processes. They have to sustain or which stand the chemicals, various rinsing processes are going to be present during the cycle.

Now as I said earlier, grinding will take place finally, after the entire processes completed, to reduce it to the required thickness of the die.

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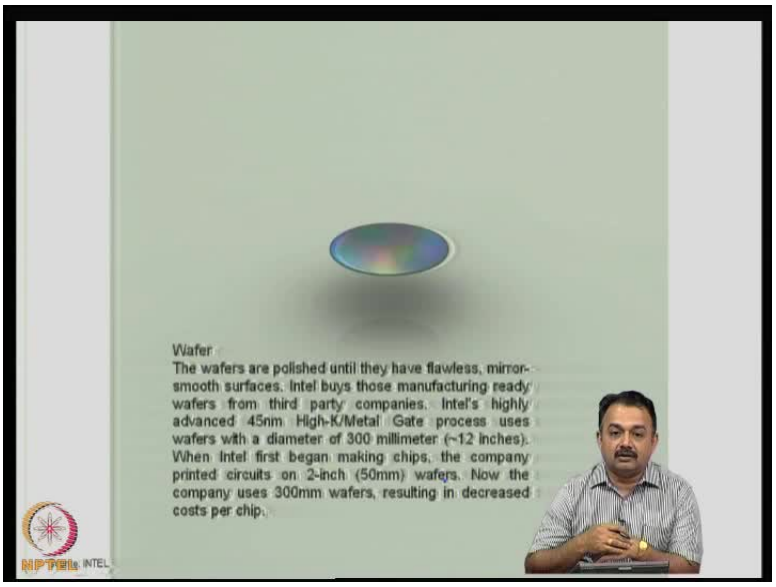

Now, the wafers are polished. Once you get the first cut wafers, before is start doing the imaging process on the wafer, you want to make sure that there is no defect caused by the cutting or extraneous material or surface defects. So, you want to polish it; and you can see that polishing can give you a very nice, mirror-like image, as you can see here.

They should be flawless; mirrors smooth surfaces need to be a obtained. That is when you are ready to begin the imaging process.

As I mention before, these photographs have been given to us for this particular course by Intel. Now, as an example, I want to say that companies like Intel, who are making the microchips other microprocessors, they have the fabs, but sometimes instead of doing the wafers by themselves, they can directly buy the wafers from third party companies. There could be companies in this industry, which is specialized on crystallization process; manufacturing or getting the ingots done to the required sizes and the diameters and then slicing it into wafers and then distributing these wafers to chip manufacturing companies like Intel or AMD and so on. That is the point I want to make here.

As an example, you can see Intel's highly advanced 45 nanometer High-K/Metal Gate process uses wafers with a diameter of 300 mm, around 12 inches and when Intel first began making chips, the company printed circuits on 2 inch, that is, 50 mm wafers. Now,

the company uses 300 mm moving to 450, resulting in decreased cost per chip; and at the same time, the yield also very high.

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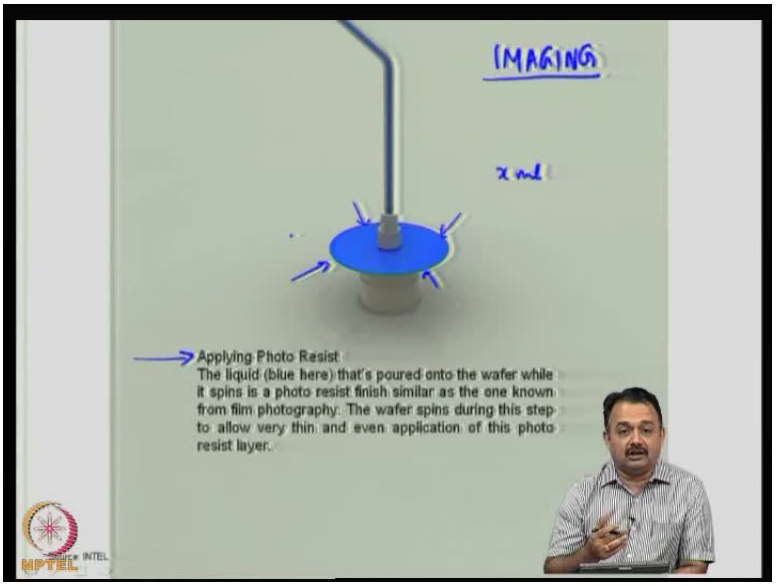

Now, the next step is typically imaging; but, for imaging your CAD design onto the surface of the wafer, you need to have a medium that will translate or take up your design and realize it on the wafer. We go through what is known as a photo resist application process; therefore, the next step is applying photo resist on the surface of the silicon wafer. In this picture, as you see, the blue color depicted, is the liquid photo resist material that is applied.

So, the liquid here is poured onto the surface of the wafer; and you have to make sure that the thickness of the photo resist is uniform throughout the surface of the wafer. You cannot have uneven thicknesses from one end of the wafer to the other end.

After the photo resist is applied, you have to measure the thickness, or by trial and error method you have to make sure that if you take let us say x ml of the photo resist, for a given area like this; and depending on different methods coating, how much thickness of the photo resist you will get on the surface of the wafer?

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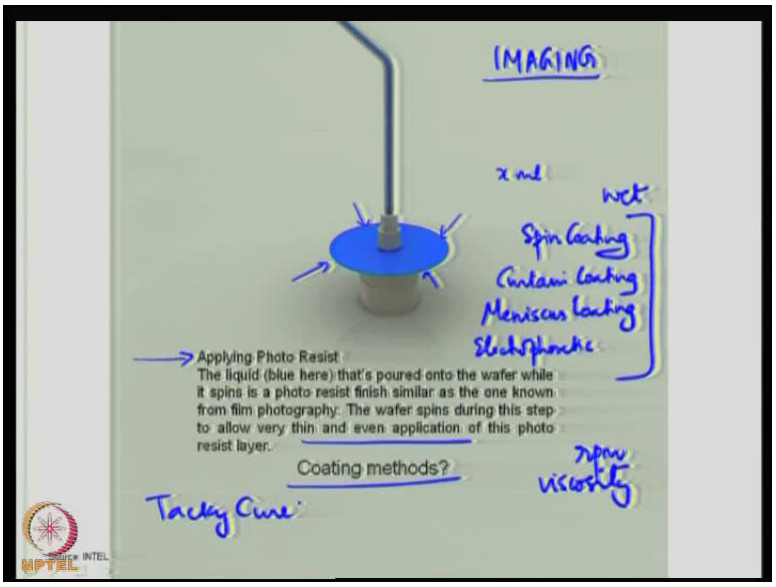

Now, what are the coating methods that one can employ? Typically, in the semiconductor fabrication industry, people use what is known as a spin coating; it is a very common method; there can be instances, where people can use curtain coating.

Other methods that are well known in this industry is meniscus coating; or you can also have electrophoretic coating.

So, these are the different methods that can give you very low thicknesses, very small thicknesses of the photo resist. Remember, this particular process has to be standardized to get very low thickness. You cannot work with larger thicknesses of the photo resist because, your line widths are very small and you cannot get a very high resolution and aspect ratio, if your photo resist thickness is going to be large. Please remember this particular important issue, when we talk with talk about photo resist application.

So, we have seen what are the coating methods; they can vary from industry to industry; they can also vary depending on the material that you are using; and these are typically for wet materials. Now, as I said here, when a material is poured on to the wafer and it is spun around at a specific rpm, it depends on the viscosity of the material that you are using, accordingly, you will get a very thin and uniform application of the photo resist material on the surface.

Now, the post process of this could be what is known as a tacky cure process; that means some of the solvents will be evaporated by drying in an oven; in some cases, the photo resist may have one solvent or couple of solvents and these have to be evaporated.

Now, these solvents have to be environmentally accepted; you cannot use organic solvent that are posting hazards to the environment. So those thinks will be taken care by the industry.

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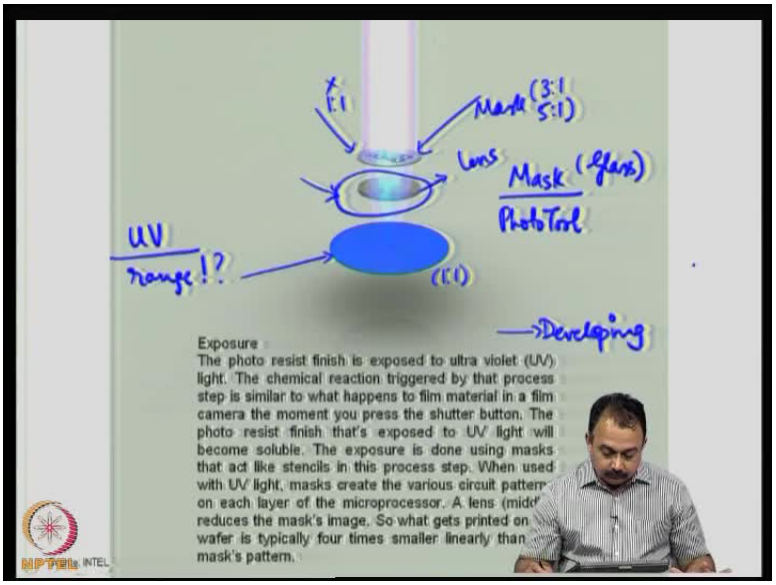

Now, we are talking about exposure; that is the next step. What is exposure? You are exposing this photo resist to UV light and when you exposing this, you are going to use what is known as the mask or the tool photo tool, typically made on a glass substrate.

This will be used to specifically transfer your design on to the surface of the photo resist. Those areas, which require capture of the design circuit will be translated on to the photo resist, using UV light. Exposure here means exposing the photo resist to a particular source of light, typically UV light.

The photo resist finish is exposed UV light; there will be some chemical reaction that will be triggered by this exposure to UV light; and what happens is basically is this thin film of material changes its chemical property and its physical property. That is the purpose of exposing this; and how you tackle this post exposure is known as developing process, which will define the latent image that is created initially on this photo resist.

Now there are different equipment for exposure; we are not going to deal with them here. Typically, we use UV light; now, we are going to see what range in the spectrum we are going to use UV light; that depends on the material that we are going to use; this is not standard. Initially, you have to look at the material; look at the compatibility of the frequency or the wave length of the UV light that you're using and make some trial and error findings; and if a satisfied with the minimum error that you're getting from these set of experiments, then you can proceed with this; or in some cases, the photo resist manufacturer will suggest the thickness and the UV intensity to be specifically used for the semiconductor fab applications.

Now, this exposure to UV light happens and those areas, which are exposed to light, will not become soluble in the developer, because the next step is developing process. Developing uses particular chemicals to remove unexposed photo resist, when I say unexposed, it is unexposed to UV light, so, developing is a process which will remove unexposed photo resist material from the surface of the wafer.

The exposure is done using masks, and this acts like a stencil, which block certain areas; which will allow certain areas, to accept UV light. You have to make sure the there is no air gap between your mask and the surface of this wafer. This will transfer the various circuit patterns onto each layer of the microprocessor buildup. There can be multi layers, 4, 5, 8 poly layers; and each of them are requires a different mask; and each requires different exposure operations and developing operations to realize the circuitry. Now, as you can see from this picture, there will be a lens, which will reduce the masks image. Typically, what will do is; this is for example, the mask, and this is, let us say, the lens; your mask will be of a larger size, let us say, 3 is to 1 or 5 is to 1 and so on; and here, you want a 1 is to 1 translation. Therefore, the lens will project the image, will downsize the image onto the wafer, to get a 1 is to 1 required ratio, translated image. The lens here actually collimates, it does a good focusing and it brings good resolution, so typically in these kind of manufacturing, you do not want to start with a 1 is to 1 mask, because if you use a 1 is to 1 mask, you will lose upon the resolution; that is the reason why we start with the mask, which is 3 times or 4 times or 5 times larger than the required dimensions.

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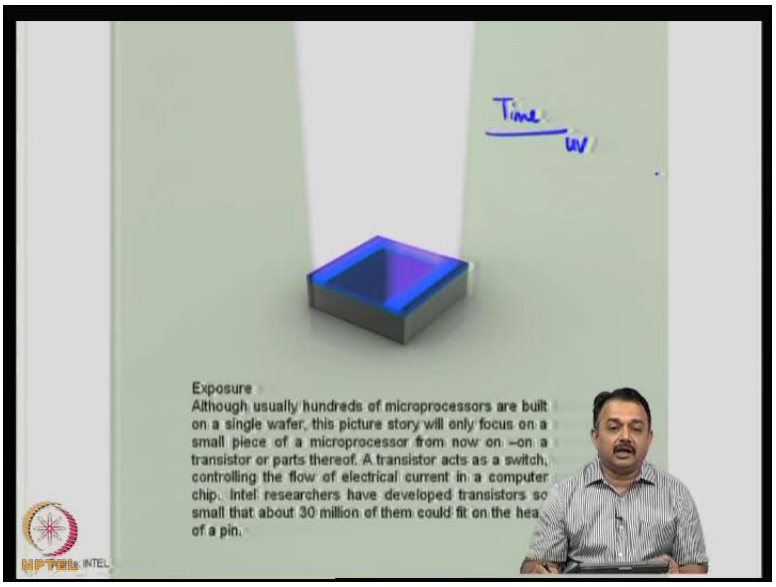

Along this entire exposure process, you do not want, to lose, any changes; any dimensional problem should not be there; you do not want to lose any features; and two things, one is the thickness of the photo resist and the time for exposure, time is also very important, you cannot keep exposing the photo resist material to UV light for a indefinite period of time, this is also recommended by the manufacturer. All these properties are inter-related and to get a good image with a high resolution, you need to work up on all these issues.

Typically, after a exposure as you can see, certain areas are affected, certain areas are not; that depends on the mask; hundreds of micro processers are built on a single wafer. This entire process sequence that I am showing here, will show you how the buildup is done for a single die.

Now, we will see a single transistor build. A transistor acts as a switch controlling the flow of electrical current in a computer chip. Intel researchers have developed transistors so small, that about 30,000,000 or more can be fitted into the area as small as the head of a pin. You can imagine, now, with this particular statement as an example, what kind of exposure methods; what quality of photo resist material; what quality of glass mask needs to be present in the manufacturing and therefore, that is a big challenge on the equipment manufacturing also.

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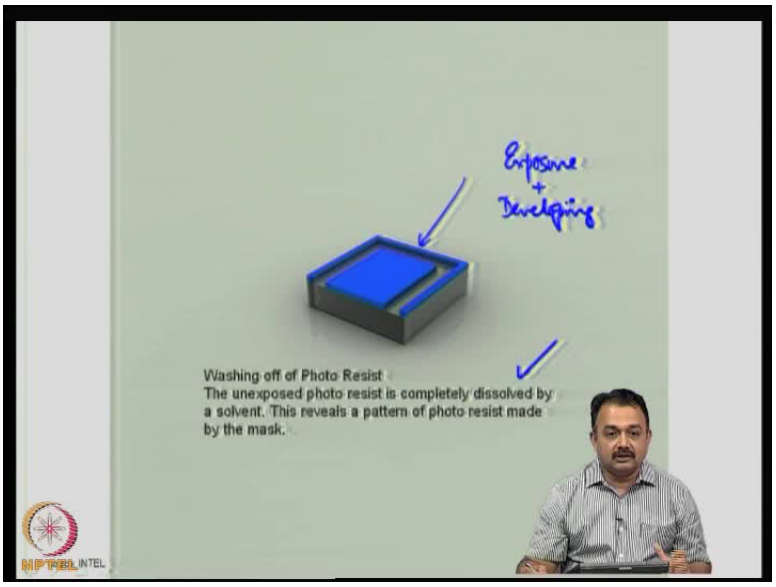

Now, other advanced exposure methods, briefly I have discussed in the last class, because we are trying to get to the end of the tunnel, in some sense because there is limitations with UV exposure imaging. Therefore, other methods like electron beam lithography, x-ray lithography or Excimer laser photo-lithography; all these are coming up and probably in the next few years, we will see these lithography methods taking dominance in this industry. Once the photo resist is applied; and you have exposed; and also you have developed, you are now seeing the image of one of the layers; as you can see, the blue layer is present, and that represents those areas of the photo resist that need to remain there, protecting certain areas of the base material or the silicon, here, or the silicon dioxide, as the case may be. Now, the unexposed photo resist is completely dissolved by a solvent, which I had mention briefly now.

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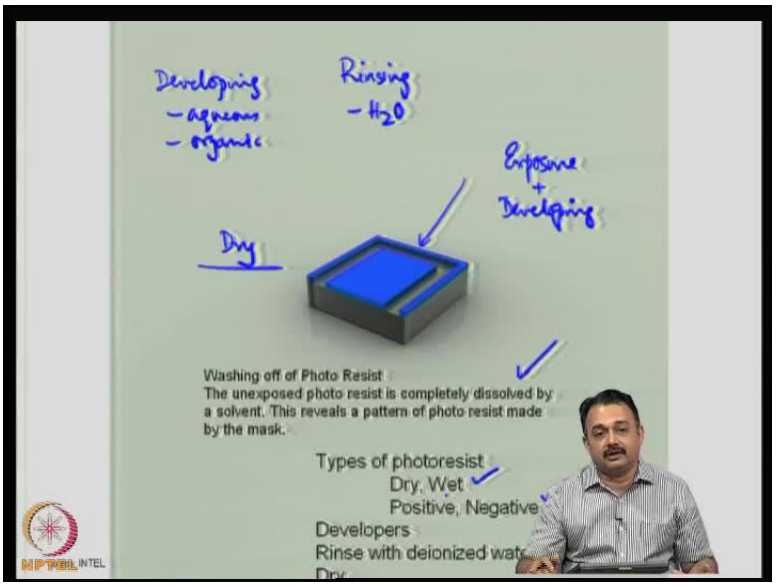

This process of exposure plus the developing will give you the completed image. This reveals a pattern of the photo resist made by the mask. The types of photo resist can be dry or wet; it can be positive photo resist or a negative photo resist; developers, typically, the developing material or the developing chemical can be aqueous and they can also be organic, but organic solvents needs to be environmentally friendly. Then, there is a lot of rinsing done during this fabrication process; rinsing is done with water, so, we have to use deionized water, which is free from all the anions and cations that normally present in impure water; so we need to use deionized water. And drying; drying is the final step. So a combination of exposure, developing and rinsing will give you a complete set of a process in the manufacturing or in the imaging sequence. Now, if you use the positive photo resist or if use you negative photo resist, then the developers will change. I am not going to spend too much time on this; we will discuss types of photo resist in the PWB technology section, because these are similar processors. Therefore, we talk about what kind of mask you will have to use, when you use a positive photo resist and what type of photo resist you will have to use, when you use the negative photo resist. The mask is not identical for each of the resist because the developing process is dissimilar; and when to use a positive mask and when to use a negative mask depends or what kind of image of the circuit you need to have on the surface of the wafer; it can be the first step or the n th layer. So depending upon the inter connection pattern and depending upon the

availability of certain chemicals and equipment, you have to carefully choose the photo resist type.

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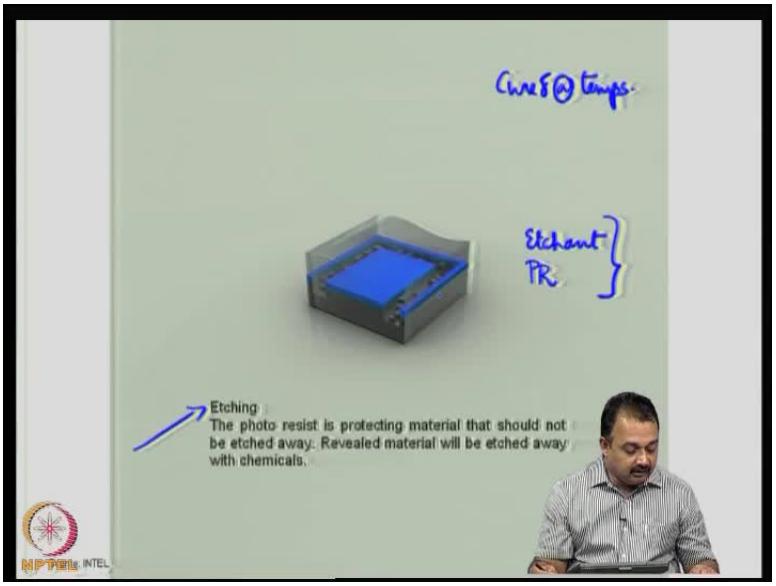

Then, once this photo resist, which is basically cured now, at specified temperatures so that it becomes very hard and it protects from certain areas on the wafer. Now you want to remove unwanted material in this stage, from the base substrate.

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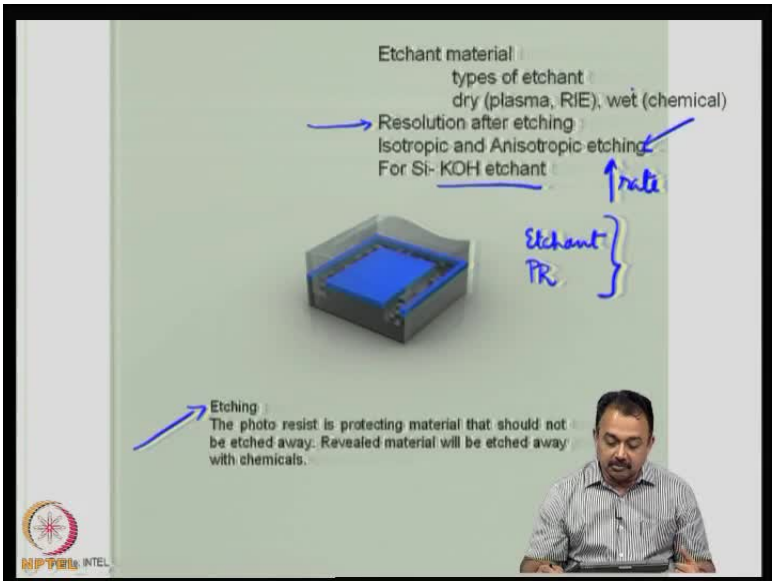

The next process is called etching; the photo resist is now protecting the material and it should not be etched away; therefore, one of the conditions is that the etchant should not remove or it should not react with the photo resist. Etchant- there are different types; now, in this case you have the photo resist also. The compatibility has to be studied and the etchant should not react with the photo resist. The revealed material, that is, the material where the photo resist is not present currently will be washed away by the etching chemical. If you look at the etchant material, there are different types of etchants. You can also do dry etching, which is basically plasma etching or reactive ion etching. Typically, we use wet etching, that is, by chemical. For example, for silicon, potassium hydroxide, KOH, is the etchant; there may be other etchants for different materials, even in the same semiconductor fab process.

Now, the resolution of etching is what is more critical and you have to spend a lot of time examining the trace widths that you have to generated, after etching and this should be equivalent to your design implementation, plus minus certain tolerances. At every stage of the process there are certain tolerances values that you can give and then qualify the wafer.

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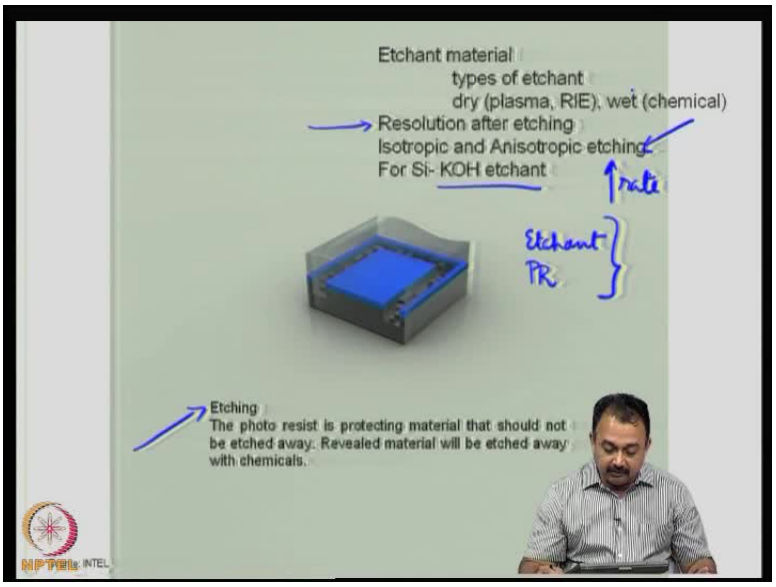

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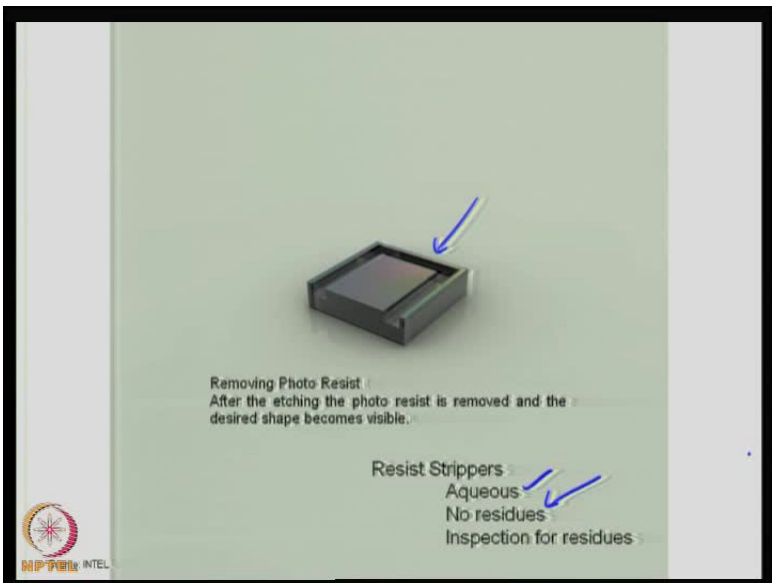

In etching also, you have a lot of problems, because you can have a difference types of etching, isotropic etching and anisotropic etching; some chemicals are isotropic; and you can use some etchants that are anisotropic. Depending upon the thickness you can have and depending upon the rate of etching you want to have, you can choose between isotropic and anisotropic etchants; each will give different types of defects. So, one has to be careful to choose the etchant type. Plasma etching involves reaction of say, 2 different gases, which produces some free radicals; and these free radicals will react with

your substrate material thereby removing it. In-situ generated free radicles or ions will react to surface and that is known as plasma or reactive ion etching. Etching is a very important step. After the etch process is done, as you can see, material has been removed. If you compare the previous one and this one you can see certain blocks of the material have been removed; now, you can remove the original photo resist material; you can see the blue layer is removed here. The design shape is now visible and this step is now complete; that is the first level, imaging is now complete. For removing the photo resist, we use materials known as resist strippers - stripping chemicals; and they can be aqueous; in some cases organic; this strippers, after the stripping process is over, should not leave any residues on the surface of the wafer, because any residue will be taken over to the next step, if the rinsing process is not complete or well done; therefore, after stripping process you again do a quality check and you have to qualify the wafer at this stage also. So, a good time is spent on inspection of the residues.

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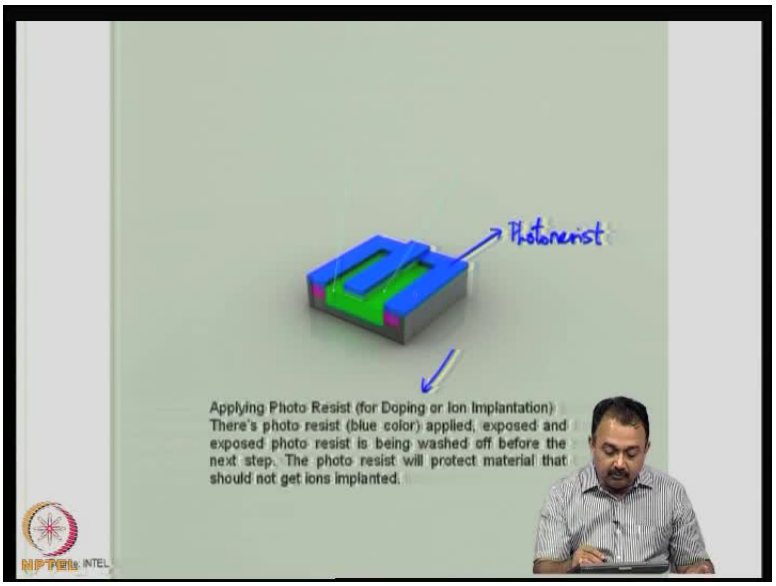

Now, again you are going back to the photo resist application. This time, the reason is you want to dope or implant some ions or use some dopants, I talked about dopants in the last class; dopants like phosphorous, boron, copper or arsenic are some of the dopants. They have used to change the property of a semiconductor, to improve the electron mobility; and therefore, the next step will be, in those areas where the transistors are going to defined, we are going to do some kind of doping. So, you have to predetermine what dopant you are going to use. The area that takes at the dopants here is

well marked here by these arrows, you can see. Other areas are covered with the photo resist; this is the photo resist material. So, again we start with the photo resist application, baking and then you keep the area exposed for doping.

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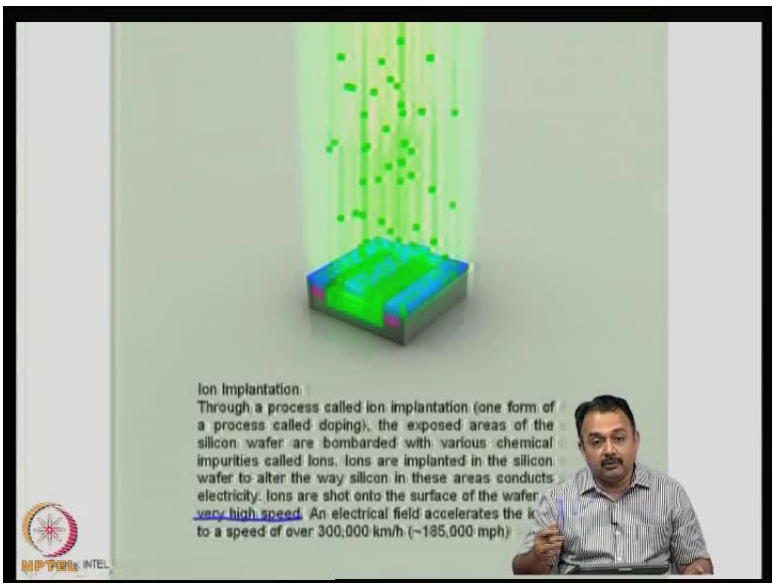

The photo resist will protect the area and this area will not take dopants. This is the ion implantation process; there are different equipment that will be used for ion implantation; basically, you require bombarding of these ions onto the surface of the silicon wafer and therefore, these ions, during this process, are implanted into the silicon wafer, to alter the way silicon in these areas need to conduct the electricity. This is very specific to the areas that are exposed; the areas that are covered by the photo resist are not altered, they are not affected. If you look at this ions are shot onto the surface of the wafer at very high speed; it is a bombardment that takes place, only then the doping or implantation can take place. The electrical field accelerates the ion to a speed of 185,000 miles per hour. It breaks into the crystal lattice and then it creates a new environment for improving the conduction property.

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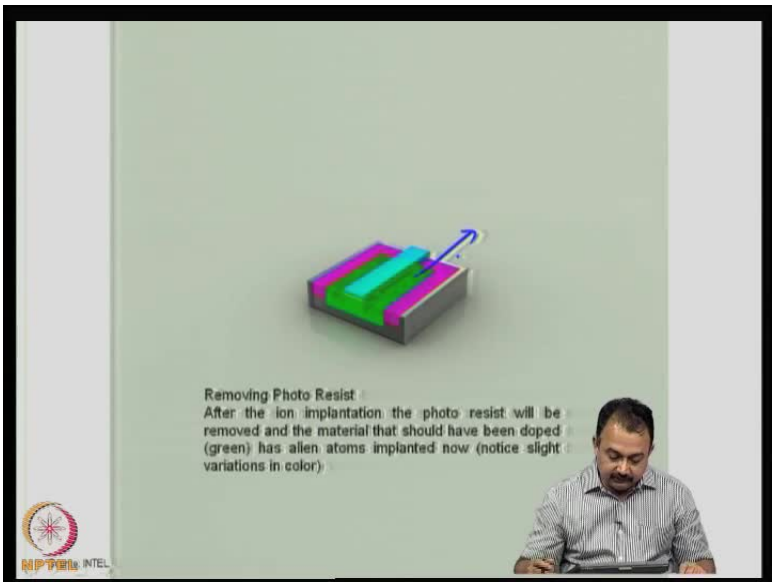

Now, once the job is over, you remove the photo resist and the material that should have been doped, green, in this case, has now got the dopants, the new material implanted; and you can see, there will be variations in the properties of these host material plus the dopant.

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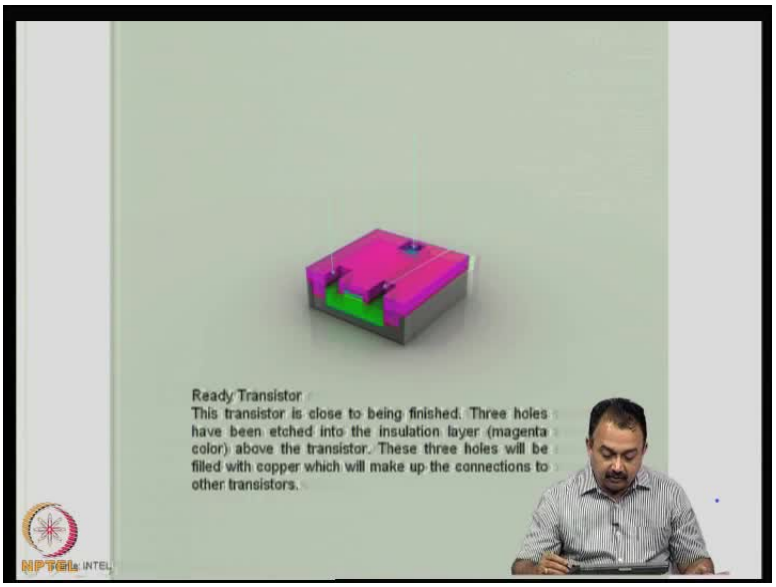

Now, the transistor is now close to being finished. Three holes have been etched on to the insulated layer; this magenta material is the insulating layer; you want to insulate it because that particular process is over; so you convert the surface into an oxide and then

make a passive; so you make it convert it into oxide. These holes are generated now and these holes will be filled with the copper conducting material, which will finally, be the connectors for these transistors.

I hope it is very clear. The top surface is magenta in color which is the passive oxide layer and the arrow shown here, represent the three holes, represent the transistors for this particular device.

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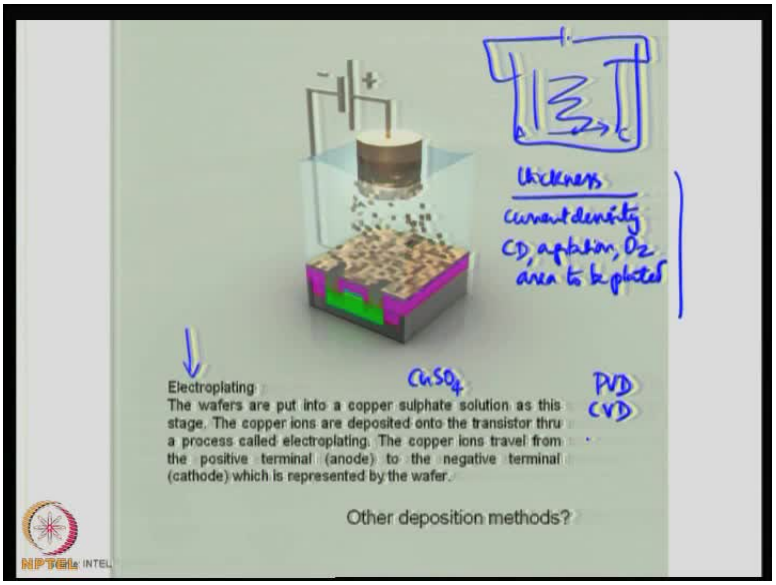

Now, how do you make this area conductive? The exposed area, as we seen in the previous slides, the open areas need to be plated with the conductor; typically, we are going to use copper. In this particular example we are taken up the process called electroplating.

Electroplating - All of you know basic electrochemistry; we have an anode and a cathode, and then you have an electrolyte, and then you apply external DC and then due to the transport of ions through the electrolytes, at the cathode, the metal will be the deposited. The metal from the pure anode will dissolve into the electrolyte and then they will be deposited onto the cathode. In this case, since we are using copper, we can take copper sulfate solution, at this stage; and the copper ions are deposited onto the transistor areas, that is, the terminals here, representing the three holes of the transistors; and this will nicely deposited the required thickness. The basic anode, cathode, then we have the

electrolyte and then you have the external DC connection, as you know; so, from the anode to the cathode there will be a ion transportation, which will deposit on the cathode.

Now, you have to make sure that the materials are pure, the copper materials is pure here; and also thickness here has to be well understood, because you cannot keep depositing larger thicknesses of copper. You can, by certain calculations and by adjusting the current density that you give in the electroplating process, for a given area, you can calculate the require thicknesses of copper that it will be deposited over a period of time. Current density and the agitation, then oxygen content, the purity, area to be plated: all of these matter to get a require thickness.

These are all important factors in determining a good deposit. The deposit should adhere well to the host surface and it should not delaminate. Other deposition methods could be physical vapour deposition, chemical vapour deposition, evaporation or sputtering; all these are other methods; it need not be electroplating alone that can be used; there are other methods that can be used for depositing the conductor material.

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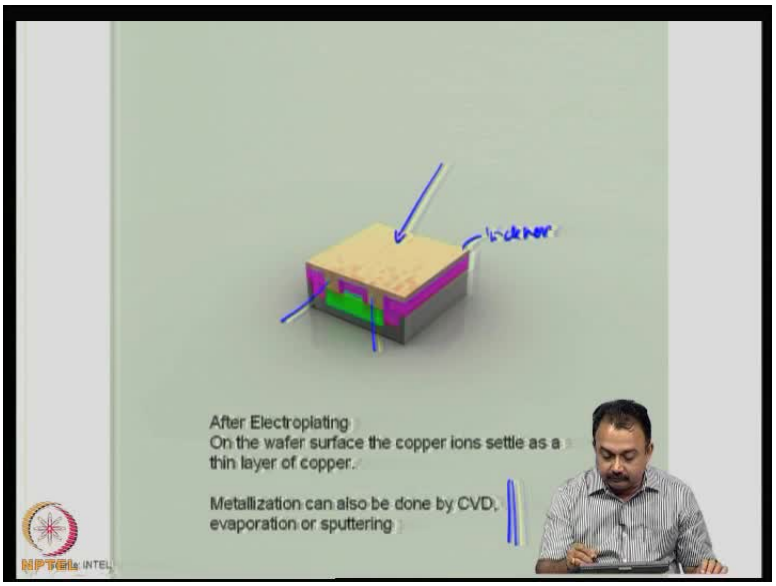

So, after electroplating, on the wafer surface the copper ions settle as a thin layer of copper, you can see here, very nicely, the entire surface has been covered with copper, including these areas, which define the transistors. Now, as I mentioned before,

metallization can also be done by the CVD, evaporation or sputtering. In any case here, thickness is very important.

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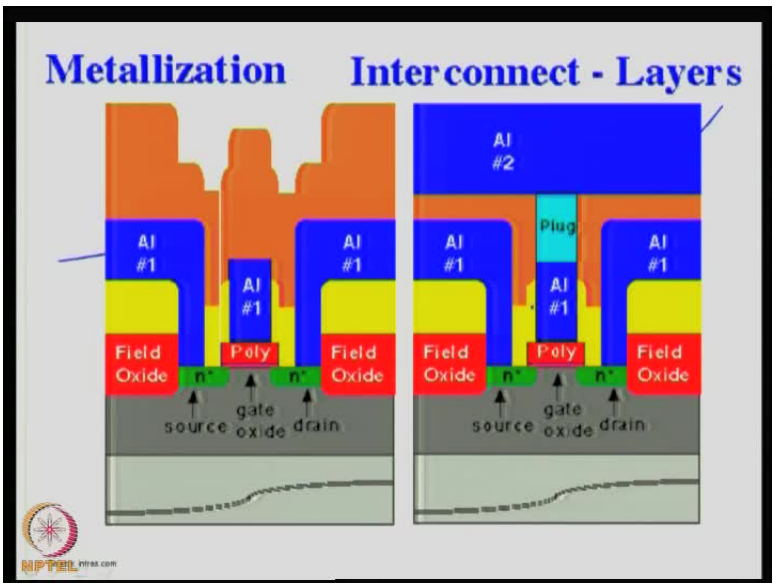

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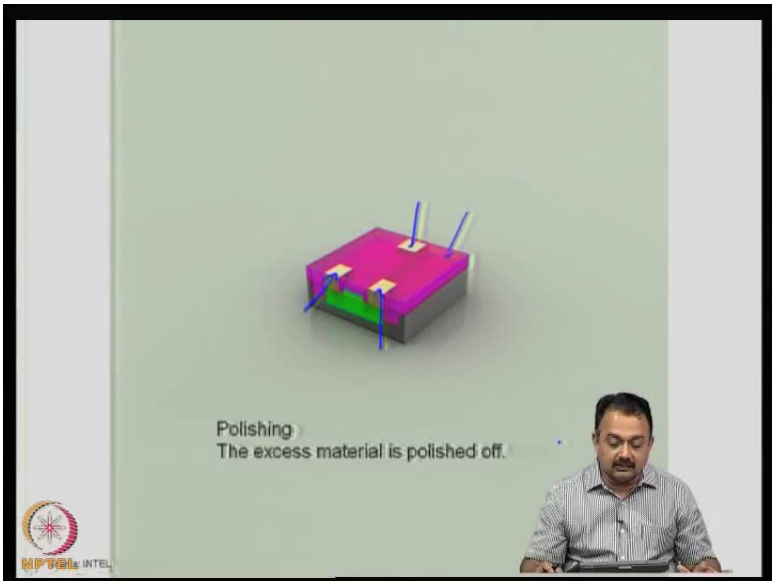

This is a different example, in this case, for example, the conductor is aluminum, rather than copper; and you can see how the source, drain and the gate are defined; how the field oxide is the deposited; there is a dielectric layer; and then here comes the metallic conductor; and then finally, they are polished; obviously, you cannot deposit the exact amount of the conductor material, therefore, you will use what is known as a polishing

methodology or CMP, as it is known as, Chemical Mechanical Planarization; and the excess material that you saw in the previous slide, here, will now will be polished and removed; and finally, you will get only the required amount of copper that is now acting like a like a plug for your source and the drain and the gate of the transistor.

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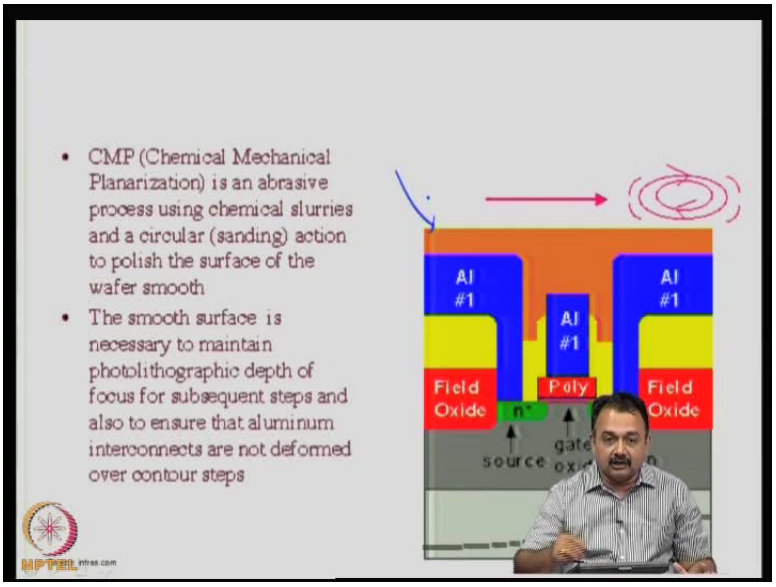

Therefore, polishing is going to be very important step and this determines the final thickness of the conductor layer. CMP, as it is known as, is an abrasive process using chemical slurries; that means you take the wafer and it would be ground on an equipment and until you remove the excess copper from the surface; so, if this is the grinder surface there will be a wet slurry coming and falling on this material; there will be an abrasive material that will be used and the silicon wafer is polished continuously, inspected and you have to see whether we have the reached the designated thickness. This smooth surface is now necessary to maintain photographic depth of subsequent steps, because again, this is not the end of the process; we are now going to build additional layers. We require to maintain minimum thickness; and also, this a CMP process should not deformed the buildup that you have already done; if it is going to deform or create cracks in the conductor buildup, then the entire effort is lost; so, the CMP is going to be a very crucial step in defining, as you can see, the final thickness of the conductor.

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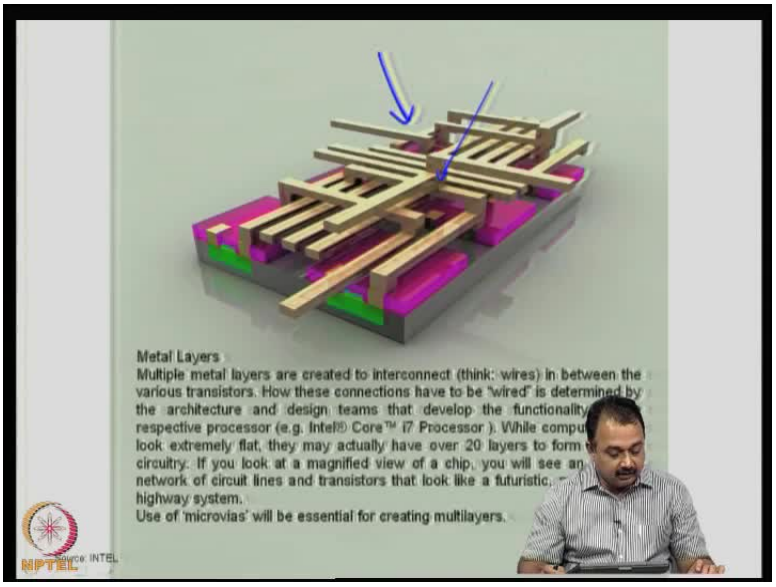

Now, you can see in this particular picture, this is consolidated. Now, you have seen one complete process step; subsequent steps can continuously be done in the same way, by repeating the cycle; this particular figure will give you very good information or understanding on how to create interconnects. Now, that the basic transistors have been formed in the base layer, we are going to interconnect between transistors using different layers; this picture, here, shows you how interconnect wires are formed to connect the various transistors below. This is also known as the wire, so, wiring density here is very important and in this particular case, for example, the connections here are between various layers of copper interconnected by small vias; microvias are used to create connections or established connections between various conductors.

There may be eight ten twenty layers of interconnect layers, in there is complex systems and if you look at the magnified view of a chip you will see intricate network of circuit lines and transistors that look like a multilayered building, like a Manhattan skyline or Manhattan building. We can see the various interconnect structures are tall and have very fine thicknesses.

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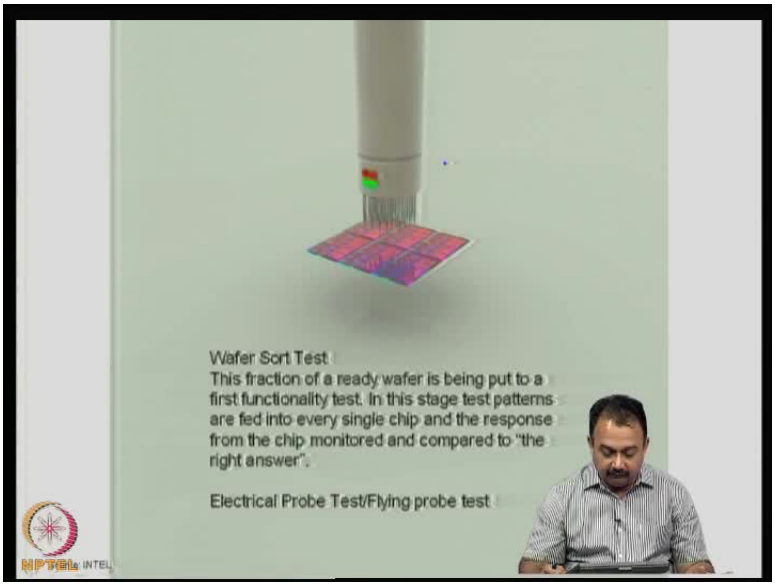

Use of microvias structures or use of vias are very essential to interconnect. Once this is done, once the complete interconnections are done, we basically go for the wafer sort test. What is this basically? We have to look at every wafer and do electrical test, functionality test; so in this stage, patterns are fed into every single chip and the response of the chip is monitored and compared to the required electrical function. Basically you can do an electrical test so that you ensure that your buildup is correct and every single die can be looked into with this particular test; you can do an electrical probe test or flying probe test.

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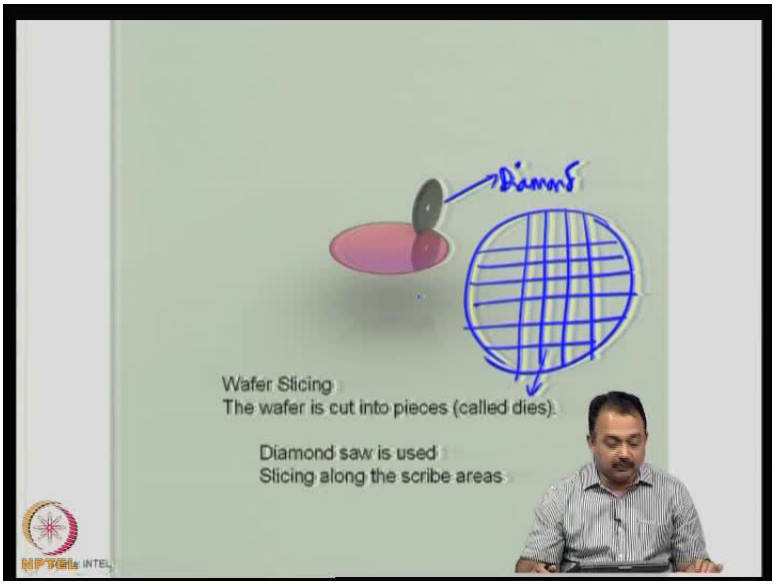

Finally, after this electrical test is done the wafer is now sliced; it is cut into pieces called dies; at this stage, probably after the test is over, we can now singulate of each of them; this is by using a diamond saw. This is the process, which I mentioned, where in a wafer flat, as you seen in the last class, there will be some scribe lines, so the cutting has to take place along these scribe lines. That depends on the crystal structure and it is very important that the scribe areas well defined; each thickness is also defined alongside the diamond saw thickness and when you slice it also, you have to make sure that the adjacent dies are not affected due to vibration or other factors in the equipment.

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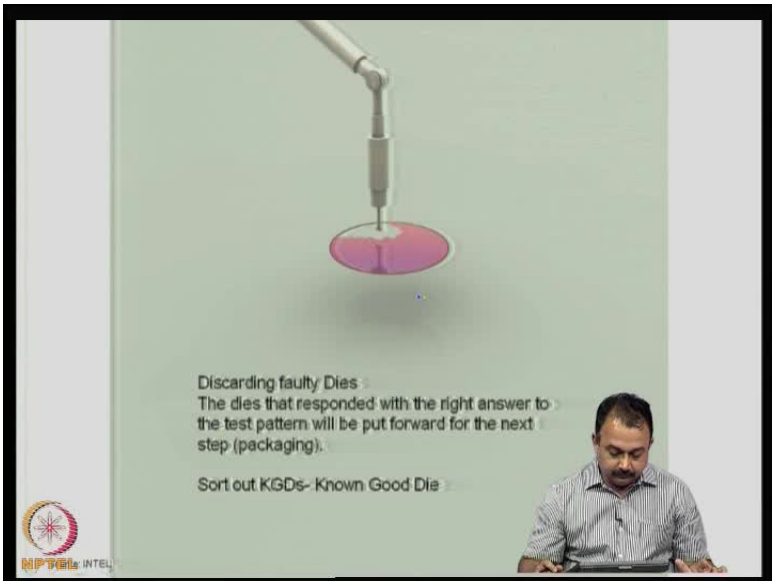

After the dies are singlulated, you get single dies now; and you have to qualify it has a known good die, KGD so, again you can probably do an electrical test for each of these dies and it can put it through a series of programmed testing, which will say whether this die has passed the requisite test.

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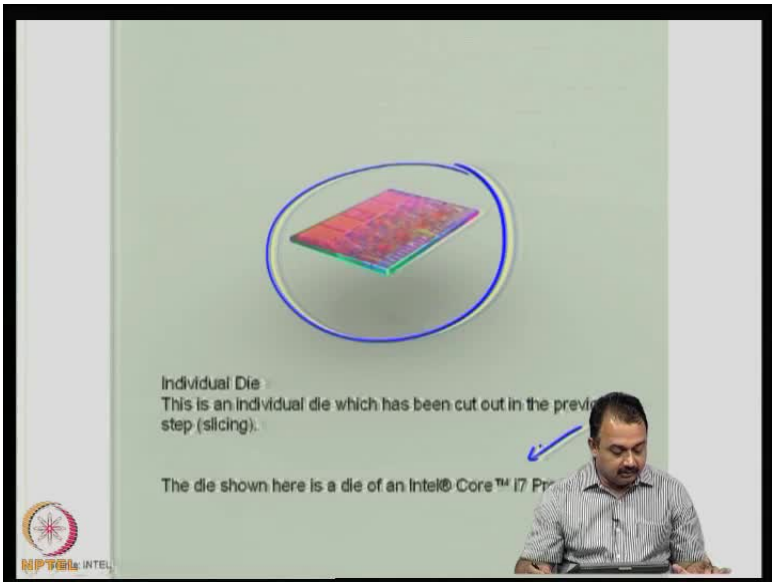

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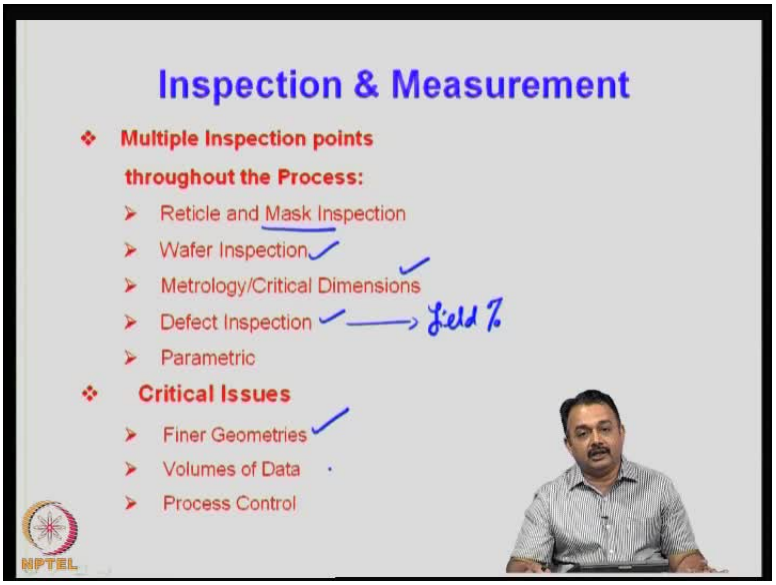

This is how you will get an individual die. This die has been cut in the previous processes, as you have seen, by the dicing process. So the die shown here is that of a Intel core i7 processor, which is current. So, this completes the front end process of the fabrications or making of a single die; now the single die will go into the back end process called packaging, to get a single chip package.

I want to emphasize here, that inspection, measurement and quality control at every stage; the steps that we have mentioned may not exactly be the same, because there may

be very many intermediate steps including rinsing, other methods of cleaning and inspection and so on. It takes a while from the silicon wafer to a single die to be complete. At each step, the quality control personnel will have to look for various defects and certify it. Right from inspecting the mask; the mask us to be perfect; there can be no dimensional variations in the mask; if there is dimensional variation seen, then you have to prepare a new mask; wafer inspection; then you have metrology and critical dimension inspections at every stage, including photo resist; defect inspection- this also goes into yield calculation, yield percentage calculation; and parametric inspections. Critical issues will be finer geometries – how they are well defined; and then you have to probably keep note of what has gone into various batches of the processes including data control, process control difficulties and so on.

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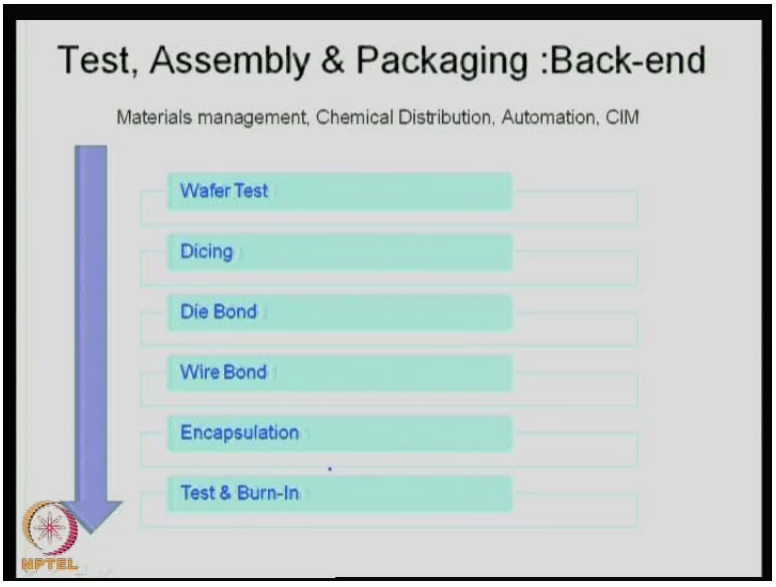

In the manufacturing, it is a large cycle that has to be completed and in the next class, we will see the back end processes. In the back end processes as I mentioned earlier, we're going to take this singulated die that we have got from the front end process and we will see how it is, again, tested, assembled and packaged, before it goes into an electronic product. The summary of today's class is that we have seen complete illustration package, covering the front end processes. Thank you.