An Introduction to Electronics Systems Packaging

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Module No. # 02

Lecture No. # 06

Basic of Semiconductor and Process flowchart

Video on "Sand-to-Silicon"

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Welcome back to this edition of electronic systems packaging course. If you recollect, we have finished module 1 last time and that module 1 covered a complete introduction or an overview to electronic systems packaging. In that we have seen various sub topics and we have spent a lot of time defining basic fundamentals of packaging. Towards the end, we defined the application areas and we also looked at case studies to understand packaging aspects in different electronics systems, which can pertain to different application areas. I hope you have gone through those modules again.

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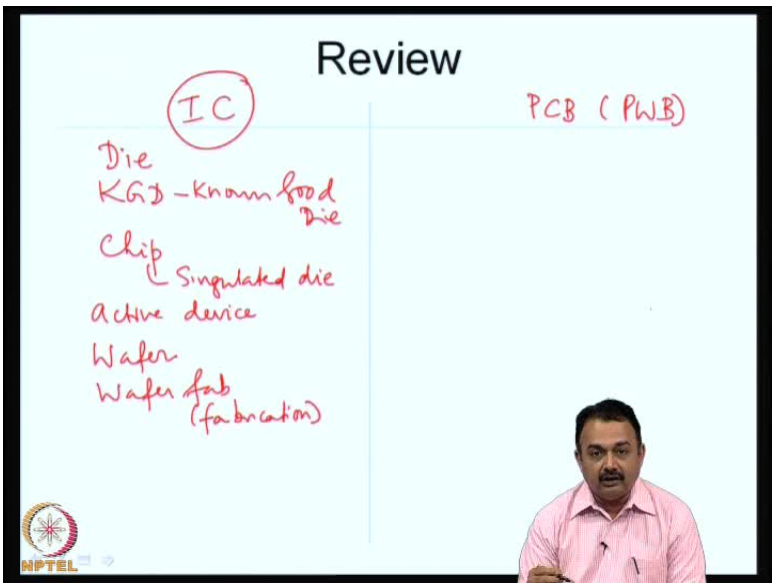

Now as a prelude to the second chapter, what we will just do is a quick review of some of the terms and glossary, so that you are familiar from now, on the very common terms that will be used. I will do a quick review and then we will proceed to chapter 2 or module 2. The first thing is I want to do a review of some terms that is used at the IC level and then some terms that are used at the printed circuit board level or printed wiring board. First, let us look at some terms that we have seen in the last chapter; as far as the IC is concerned, IC stands for integrate circuit; you can also use terms like a die. Die also represents an active device. We also looked at the term called KGD, which is known as known good die. A known good die is one that is tested after fabrication.

A common term that is used is a chip or a microchip that also represents a device that has been fabricated out of silicon wafer. So, it can be a singulated die, that is from the wafer it has been singulated and it is ready for packaging.

Then the other term that I have commonly used is active device. It can be a microcontroller or microprocessor, various active devices that perform different functionalities. Then, some other terms that we have seen is a wafer. Then, we have seen the term called wafer fab; fab stands for fabrication.

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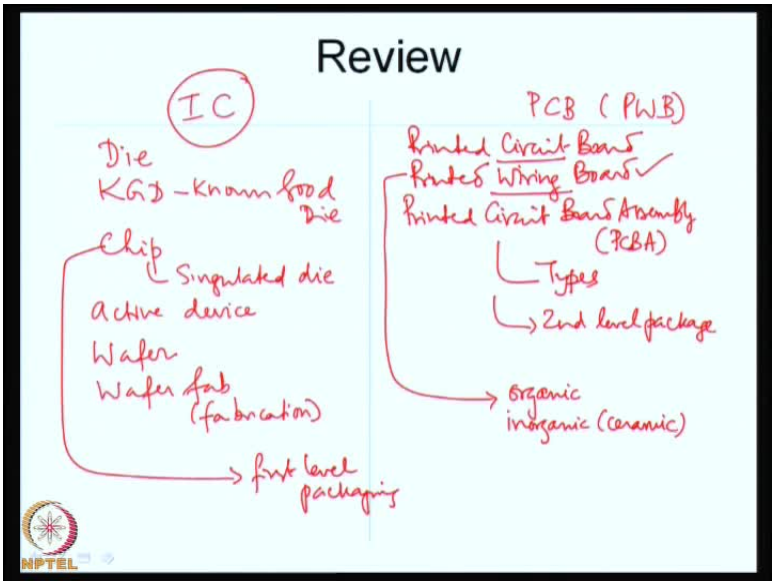

These are some other terms that we have seen under the head IC. Now coming to printed circuit board or printed wiring board, I told you in the middle of the last chapter that these two terms printed circuit board and printed wiring board are used interchangeably,

so you can say, you can write it as printed circuit board or you can call it as a printed wiring board

Basically, if the board is processed then you call it as a printed wiring board because you are replacing wires with copper conductors. At that stage of the system that is the second level packaged products, it is called wiring boards. Now, the printed circuit board terminology is used normally, when the printed wiring board is stuffed with components and interconnected or soldered. It is basically an assembly. So, you might also here the term called printed circuit board assembly, PCBA; this is also used in common parlance. There are different types of printed wiring boards, which we are going to see at a later stage and there also, this is called a second level package. So, the printed wiring board is a second level package and the device or the chip that goes for packaging, which is called the first level package.

Now our focus is simultaneously on two levels; the first level packaging and the second level packaging. Then, I might also use the terms called organic, to denote a different type of a printed wiring board and an inorganic substrate typically a ceramic substrate will be used. You will be slowly introduced into these type of terminologies from now on, you can also call this is as plastic.

So this is the kind of first level information I wanted to give you today before we move with the second chapter.

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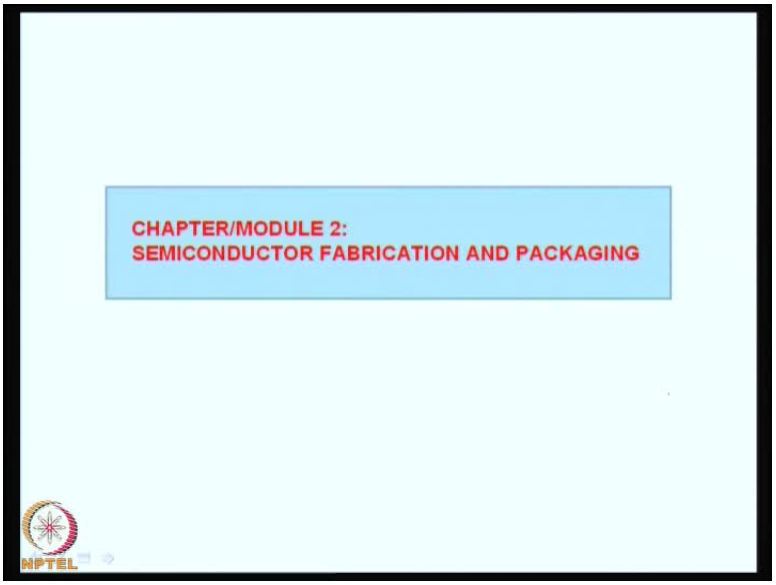

Now the second chapter is titled, Semiconductor Fabrication and Packaging. So, what we are now going to do is, although this is not part of the packaging that is the fabrication of the semiconductor or the die, but still, it becomes incomplete if you go to first level packaging directly. We would like to spend some time, on looking at how a semiconductor fabrication process has evolved and what goes into the manufacturing of an intergraded circuit or a known good die and from that die how packaging is carried out.

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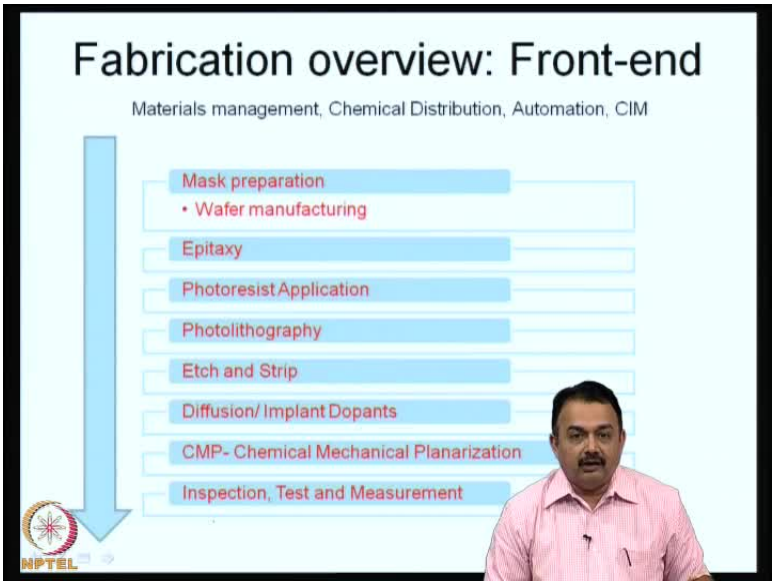

Now, if you look at this slide, what I have given here is the process steps for Fabrication over view, for a front end process of an IC manufacturing. There are two sections to semiconductor fabrication; the first one known as a front end processing.

Here, if you look at the end of the process flow, we are ready with the manufactured die; and the starting point is wafer. So, in an industry, I talked to you about the cost of semiconductor manufacturing setup; it is about 2.7 billion dollars today, globally; very expensive in the sense that, after the setup of the semiconductor fabricating unit, you have to maintain it periodically, because we are going to do this process in a clean room, which is free of dust. If you want to maintain a semiconductor fab under clean room conditions, that is where most of the expense or running cost go into.

In this fabrication setup, you have to know a lot about materials management; what is the starting material? what are the chemicals that are required to process the starting material

into a final product that is known as the die, that is tested and certified. There will be a lot of automation and there will be computer integrated manufacturing, right from the start to the finish.

We look at the steps one by one. The first thing is, if you want to prepare a die, prior to this some CAD work is been done; you call it as a VLSI CAD and out of this, a mask is produced, that is a design depicting the interconnections is generated, from the CAD output. That is a technology file that you get from CAD.

You may have different layers to be generated in the semiconductor fabrication process; for each of these layers, a conductor layer or a via, you require a separate mask. So, the mask is the starting point for the die manufacture. What is a mask? A mask is basically what you call as a photo tool.

Typically, this is done on a glass base for semiconductor manufacturing, but in the case of a printed wiring board manufacturing, we do not use glass; we use some other plastic material or film, a normal photographic film. The mask is prepared; this is typically not part of the semiconductor fabrication; there are agencies or bureaus that give you the mask. This mask is taken now, into the wafer manufacturing section.

As you know we are now going to start from this kind of a wafer; and from these you are going to get singulated dies like this.

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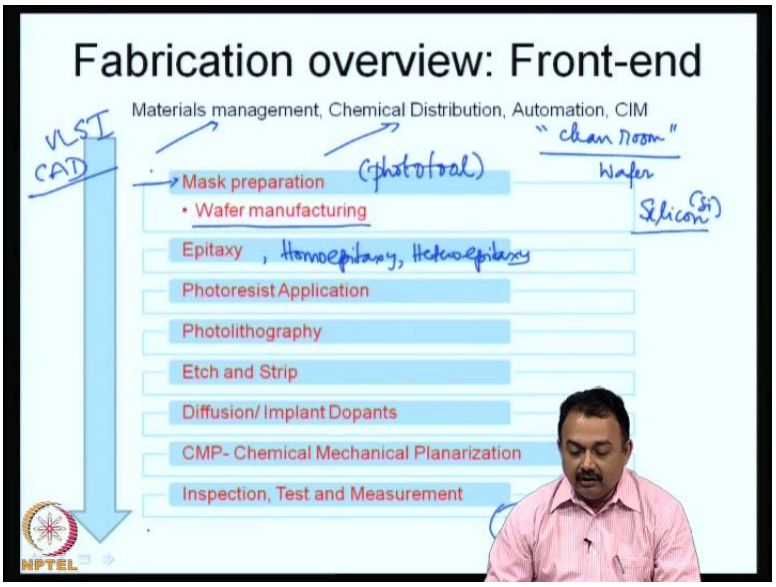

The first process is, you must know what type of material are going to start with; let us assume, we are going to start with silicon. Silicon is the starting material. The first process is known as epitaxy; epitaxy is basically formation of a pure mono crystalline film on another mono crystalline layer of silicon. The reason why we do this, in-situ, we are going to prepare freshly formed crystalline silicon layers; the purity will be very high; and if you are using compound semiconductors, then this process also becomes very useful. You can grow epitaxy layers and epitaxy comes in different types; you can have homoepitaxy or heteroepitaxy.

Now, heteroepitaxy is very important for compound semiconductors like gallium arsenide. Normally for silicon, you will use another silicon layer, that is typically of very small thicknesses; and from that the gate manufacturing process will start.

Homoepitaxy and heteroepitaxy are the common types of epitaxial processes; basically, it is an oxidation process; and it is also very important to get very pure layers of silicon.

After epitaxy, there will be an oxidation process. To get a good conversion of silicon to silicon oxide, we do an epitaxy process, to get pure mono crystalline film on the wafer. The wafer is initially well cleaned, so that it is free from any of the impurities; remember, the starting point to the endpoint, the entire process is done in a clean room. I will talk about clean room requirements very shortly.

The next step is photo resist application. Photo resist is a material that is used to aid the transfer of image from your mask onto the substrate. Without that, you cannot transfer your image from the mask, which basically a glass substrate, on which the pattern is generated; and this has to go to the silicon wafer layer.

We have to use a photo resist. Photo resist comes in different types; it can be wet photo resist or a dry film photo resist; or it can be a positive photo resist or a negative photo resist. Probably, this not a right time to discuss the different types of the photo resist, we will have a separate chapter on that. But, suffice it is to know that photo resist will be a very important material; and the thickness of the photo resist and the type of photo resist that is used for a particular process has to be well defined by the manufacturing company at the start.

As you know, I talked about Moore's law much earlier; and the difficulties that we are experiencing now a days to match the Moore's law prediction is probably because there is some limitation on the materials that are used in the photo resist. Because the thickness has to reduce for lower line widths and the imaging technology, which is the next step here, the photolithography has to match the types of photo resist that we are using. A combination of these two; the type of photo resist and the photolithography process together would generate more number of cells on the silicon wafer and therefore, the density or the silicon efficiency will be very high.

Currently, the industry uses a wet process for photo resist application; and there will be a dry imaging process that fallows the wet process of application of a photo resist; and therefore, the resolution that is got from the photo resist is very important in defining the yield rate from every wafer.

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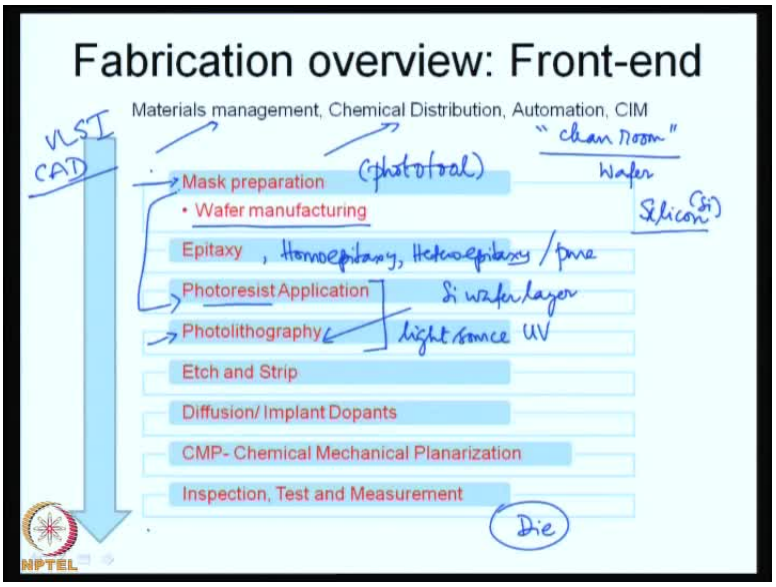

After the photo resist is applied and it is cured, then we use a photolithography, using the mask that we have generated for a particular layer. Once the mask is kept on the substrate, which is applied with the photo resist material, then you apply a light source. Photolithography involves using a light source, typically UV; so, in the spectrum of light, we are going to use the wavelength of UV light to selectively activate the photo resist material; some of the areas have protected by the mask, some of the areas are not protected; therefore, those areas which are exposed to UV light will get physically

changed and therefore, they are also going to react with certain chemicals during the process of developing.

The next step - photolithography also encloses step called developing, which will now define the image that you want to generate. This is a very important step; defining your image on the substrate using photolithography will be a very important steps in the transfer of the image and therefore, the yield rates are very critical at this point.

Now, the success, yeild rates as I said, depends on the light source that we are using, because as we go down the thicknesses of the photo resist and also as the line which go smaller and smaller, there is a demand for high resolution from the light source that can give us the required line widths, with less error, acceptable errors. Therefore, people are looking at new materials for UV light. For example, Excimer UV light sources are being used; UV laser; krypton fluoride is one of the material that is used to get the source for UV light.

If we want greater progress, for example, we are now working at 22 nanometers and you want to go to 11 nanometers for example, and then beyond. Then, we will see some kind of a limitations caused by the light source; therefore, new technologies will have to be looked at. I talked about disruptive technology the other day; therefore, disruptive technologies which can change the entire scenario for the front end processing could be electron beam lithography; it can be x ray lithography; or it can be extreme UV light lithography; or ion projection lithography and so on so. These are techniques that are now being researched; it is not yet into the manufacturing scenario; but, we can expect these technologies and equipments are going to be expensive in these areas, but we will see original equipment manufacturers coming up with solutions for better resolution.

Once the image has been formed, you are now going to remove the unwanted material by etching and then strip off the photo resist which has protected your conductor areas or transistor areas. The next step is going to be diffusion. You are going to introduce new material that can provide better electron mobility, other than the host material that is silicon. You are going to improve the properties of the semiconductor.

Our dopants will change the electrical behavior and conductivity, which is what we are looking for, as far as the electrical circuit is concerned. Therefore, lot of new materials

are being used as implants or dopants; typically, you can use phosphorous, you can use Boron, Potassium, Copper, Arsenic, etcetera.

You have to look at which material you need to use, based on the electron mobility properties and so on. After that, once the interconnections are done; depending upon how many conductive layers you are going to image, for a particular design; then we do what is known as a CMP process: Chemical Mechanical Planarization, to remove the excess plated material from the surface of the wafer.

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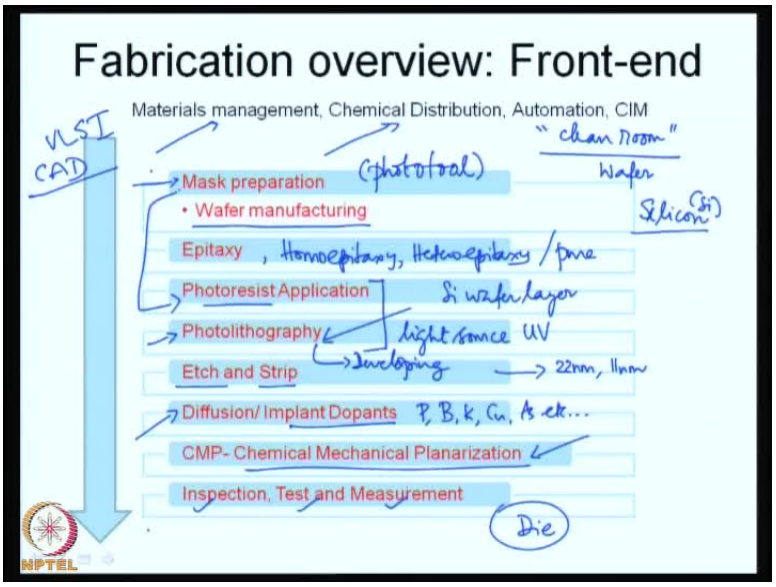

That is again, a very important process to remove nanometer material; and therefore, giving you the final configuration that is required. So, inspection at every stage of these processes, which I have mentioned, is very important. You have to qualify at every stage. Finally, the wafer is inspected and electrical test is done and certain measurements pertaining to the nets that are generated in the design have to be verified. This gives you a complete picture about what processes you can expect in the front end processes.

Now, we will go to the back end process, which is titled, Test, Assembly and Packaging. Once the wafer is ready, with all the definitions of line width and the number of cells or number of dies generated on that; basically, you cannot do any wastage on this material. So, product planning is very important. Now, we have to see a process, how we can singulate it into these kind of individual dies and then package it. Here again materials management is very important; automation is a key factor; computer integrated

manufacturing is the key word. The wafer is tested; the wafer with the dies are tested electrically, typically, for shorts and opens and connectivities. After that dicing is done; here, you are now going to singulate.

You are going to singulate each die from the wafer. Dicing is a very important step, because care has to be taken that you do not damage the adjacent dies. Each die, singulated die is very important in calculating the yield percentage of the entire process.

After that, die bonding is done. The die or the known-good die has to be mounted on to a substrate that can hold the die. That is known as die bonding; typically we use an adhesive and place the die on a substrate; and then it is bonded and cured. That is a separate process by itself, to make the die sit on a particular substrate like this; and then you do an attachment.

After that, wire bonding is done; the wire here represents the first level interconnect. Because the IO pads or the bond pads on the way on the die is now getting connected to lead frames of the package.

So this is a very important step, where, for example, if I can draw a die here and I am going to draw a substrate, on which the die is mounted; and this substrates have got lead frames across; now, there are bond pads on the die. From here, we are going to establish a connection. This is called a wire bond; the wire bond usually is gold or aluminium; sometimes, copper is also used. So, this is gold, aluminium or copper. Wire bond typically represents more than eighty percent of the first level interconnects, today. If you open up any package; again, I am going to show you this package which you have seen last time; if you are going to rip up this package and see, you will see the basic die that is mounted on this substrate; and then as you see here at the end of the edges there are lead frames. What you expect if you open up and see is a wire bond, connecting the die bond pad to the lead frame edges, at the periphery. That is how the fist level interconnections are done.

I have opened up, I have cut a chip here; and if you can closely look at this chip, you will see the die and the wire bond inter connect going to the lead frame. This is a very important activity in the back-end process of the semiconductor manufacturing.

We will spend a lot of time when we talk about fist level connection choices, about wire bond. Once the wire bonding is done, a preliminary test is done to see if the wire bonds are well connected and then we do what is known as an encapsulation; or this is also known as protection; basically, we protect this entire die with the plastic package.

As you have seen in this sample here, the black material that you see is a plastic over mold; so, this is also known as a molding process.

The wire bonds are now protected and the lead frames come out from this die; and they connect to the external world. Now, this particular component will go to a printed wiring board or a printed circuit board; and then the second level inter connections will take place.

The second level interconnections are basically your solder connections. I hope u get a clear understanding about what is a first level interconnect and what is a second level interconnect. I repeat the first level interconnect is what you see here in this slide, where after the die is singulated, you do a wire bonding using gold or aluminum and the second level interconnect is when; in this example, as you can see here; the die, in this case, it is a unpackaged die, but in this example, if you see here which I place closely, there is a packaged die, which is interconnected on to the printed wiring board, which is the second level package.

Finally, for every process you have to do a test and burn-In. In some cases, the entire die or the package is sent for a burn-In test. There are certain specifications and it has to undergo thermal cycling, so that it can be qualified as a good package.

This is done for every package that comes out into the market. That is the kind of reliability assurance that we get from the manufacturer, about the testing process.

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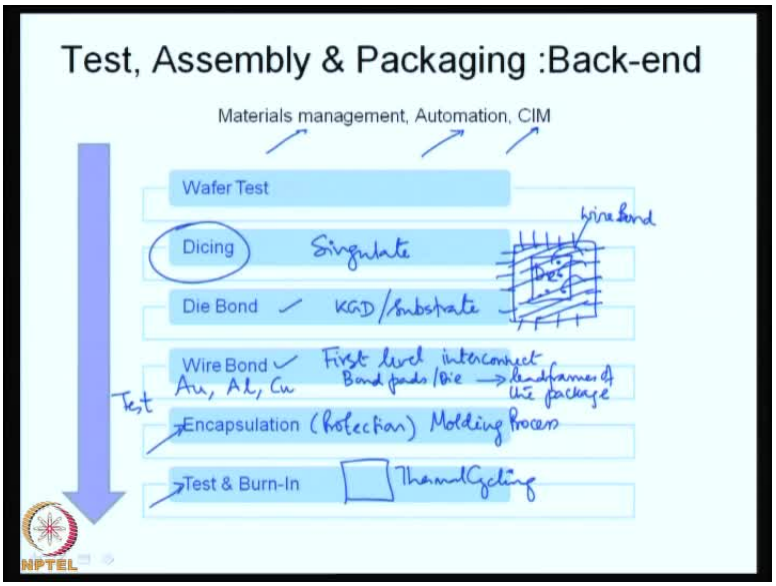

I hope you are clear with these 2 processes, The first one is the front end process and the second one is the back end process.

Before we go further, I will give some basics; I would like to describe the entire semiconductor process in detail, with the help of a video tutorial; and also some photograph illustrations, before that some basics.

Semiconductor has got resistivity lying between that of a conductor and insulator; all of you are aware of that. It establishes its conduction properties through complex quantum mechanical behavior, with a periodic array of semiconductor atoms.

The resistivity is proportional to free carrier density; and this can be changed widely by doping different atomic species. Doping becomes a very important process; selecting the dopant again becomes a critical thing to define the carrier density; and to define the electron mobility that you can improve upon, compared to basic silicon. Some dopants establish electron carrier density, so you can call it as n-type semiconductors and some establish hole carrier density, you can call them as p-type. I think all of you are aware of this basic classification of semiconductors.

Electric fields, when the material is subjected to electric field, they enable electric switching between conducting state and a non conducting state. The group 4 elements, if look at the periodic table, in that you have group 4 elements – Germanium, silicon,

Carbon and tin. Silicon is the most commonly used material for semiconductors and it is also abundant on earth. If you can look at this table here, silicon abundance is very large, almost 28 percent where as other materials like Gallium, Arsenic, Germanium, Cadmium and Indium are very low.

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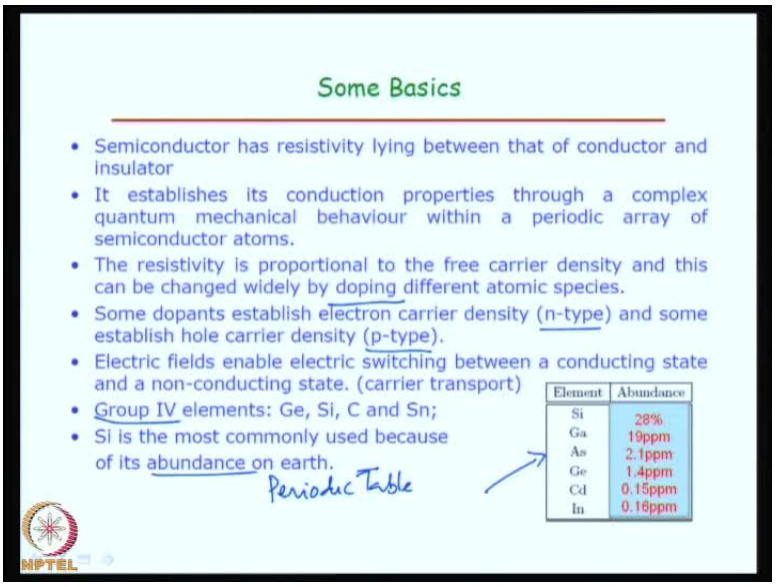

If you are going to use compound semiconductors, you will be using some of the other materials that I have listed here.

Now, briefly, if you look at the formation of semiconductor crystals, this is a group 4 element, silicon; and what I have depicted here is the outer shell electron configuration. So, it has 4 electrons in the outer shell. If you look at the electron arrangement here, for silicon, it forms covalent bonds; you require an octet, so, sharing of electrons is done by silicon to another silicon atom; that is how you get the eight electron complete octet.

All of you aware of this basic electronic configuration of elements in the periodic table. In this case, for example, as you can see here, silicon, it has got a 2, 8, 4 configuration 2 inner; then the second one has 8 electrons; and the outer one has 4 electrons. Therefore, it enables covalent bonding.

Now, if you look at group 3 and group 4 for example, Gallium and Arsenic; this has got 3 electrons in the outer shell; and this has got 5. This is a very good instance of an octet

formation for a covalent bond, by sharing; so you can see the order of 3, 5; 3, 5 here; and therefore, the octet completion takes place by 8 electron sharing.

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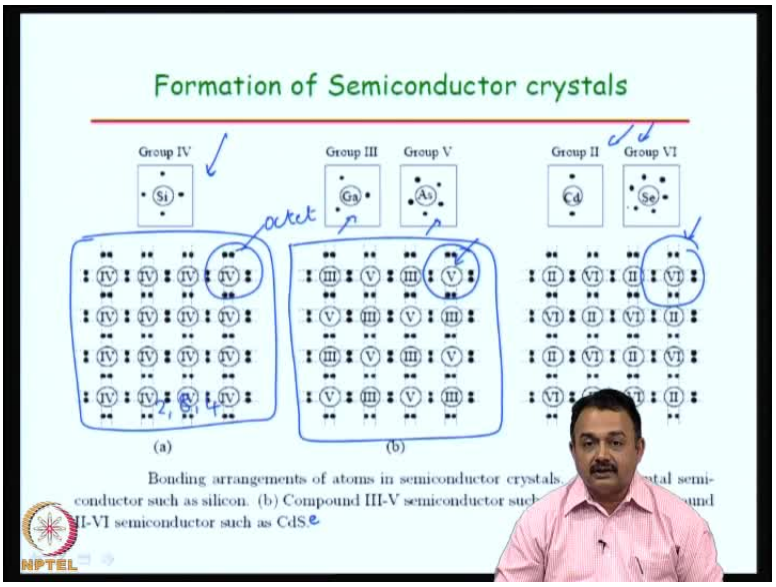

This is how group 3 group 5 semiconductors are formed, compound semiconductors; and group 2 and group 6, cadmium selenide; this picture shows again, an octet 8 electrons complete shell; and this is the good example of covalent bonding in semiconductors.

This picture shows you bonding arrangements of atoms in semiconductor crystals - first one is for the elemental semiconductor like silicon; and the second one is compound semiconductor belonging to group 3 in the periodic table and group 5 in the periodic table such as gallium arsenide; and the third one compound semiconductor formed cadmium solenoid using group 2 and group 6 elements.

The bonding requirements, for example, I will give you an example, group 4 semiconductor, silicon is a group 4 material, now, if you look at substitutes from, lets say group 4 itself, the requirement is that, if you take a group 3 acceptor, that means it should accept 1 electron to mimic silicon; where as group 5 donor it will forfeit or give away 1 electron to mimic silicon.

These are the requirements for bonding in a group 4 semiconductor. Group 3 to group 5 semiconductor; if you take the case of gallium, group 3; then substitutes in group 3 will

be a group 2 acceptor, which will accept 1 electron to mimic gallium; and group 4 donor forfeits 1 electrons to mimic gallium.

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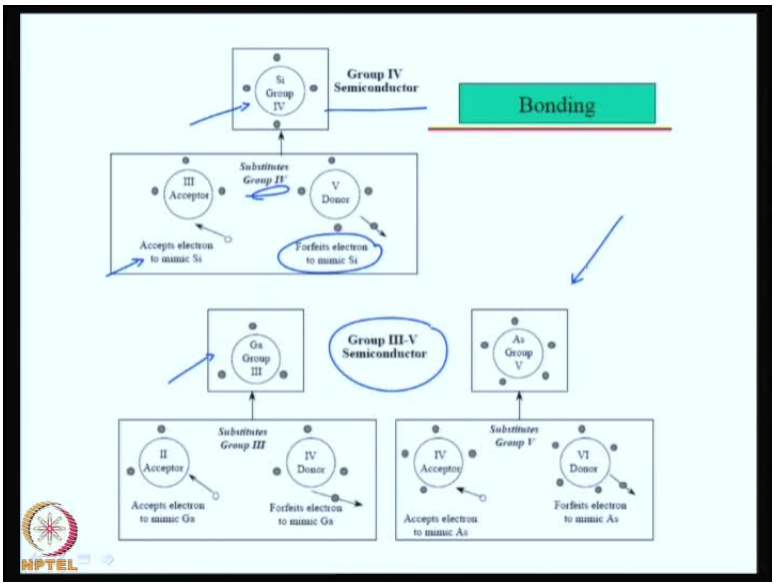

Similarly, for arsenic and other substitutes from group 4 and group 6. If these conditions are met, then compound semiconductor bonding is explained, this is how it happens. That is some other basics; now, if you look at the process, everything starts with sand, basic sand material or you can call it more specifically quartz is the starting point, but basic sand, quart sand, which is silicon dioxide here, reacts with carbon at high temperatures to form silicon and carbon monoxide.

The question is how much purity of silicon can we get. For semiconductor manufacturing, you require a very high purity: 99.9999... there should be totally eleven nines. That is the kind of purity that one looks for, as a starting material for the semiconductor process. Quartz sand is the starting material; it is converted to silicon; and that silicon is purified by repeated recrystallization process, to get very high purity of silicon; nothing below that is accepted as a starting material for the process.

Now, very briefly, if you look at this particular slide, we start with silicon as an ingot material; from there the wafers are generated; this is an ingot material - a rod of a pure silicon and here, you have the silicon wafer; then the wafer processing takes place, including oxidation, imaging, patterning, etching; and then the processed wafer is now

ready for die attach. which I explained; then comes a wire bonding; and then encapsulating the IC in a plastic package. to define the final package format.

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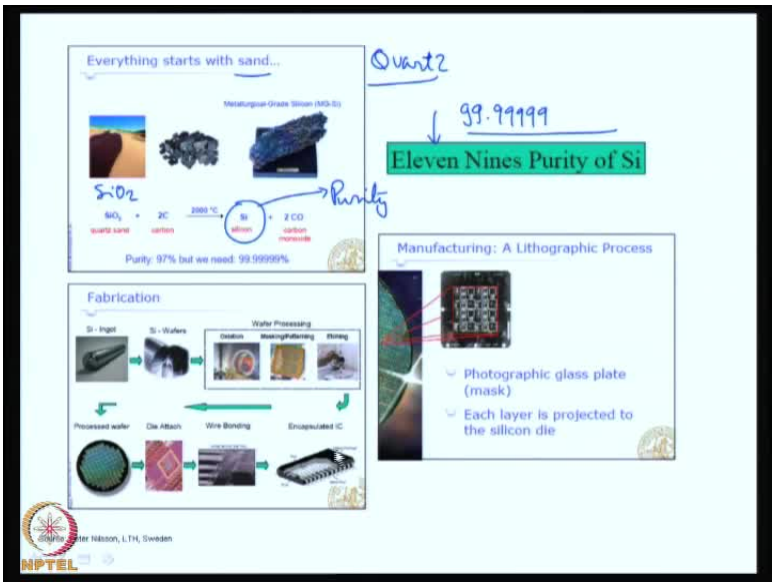

The lithographic process to define the image, again, becomes very important. Each layer is projected to the silicon die, from a master copy or a mask; and as I told you before, a glass plate is used as the mask, for the imaging process. You can see in this figure, the various cells that I defined in the wafer; each one represents one die; and then, these are the dies, after they are diced from the main wafer. Intel uses different wafer sizes and today, Intel is using 32 nanometer for its current microprocessor technology.

The various sizes of wafers are dependent on the number of dies that have to be generated; today, we are working at 300 millimeters; 450 millimeter technology is also well established. As the wafer sizes increase, you are expected to get more yield out of it; and more dies coming out from the fabrication process. But at the same time, the die size can also increase, because you are increasing the density of the interconnections.

Normally, when you use a photolithography process, the image sometime is twice, 4 times or 6 times more than the actual size of the die. So, a stepper process is used to reduce the image that is falling onto the wafer; in that way, a good collimation is done and good resolution can be established, instead of using a direct 1 is to 1 image. UV light or any other light source goes through the mask that is shown here, then it goes through

the lens which projects it and collimates it on to the wafer, where the photo resist is ready there, to accept the image; and that is transformed physically and chemically.

Of all the processes, the step down photolithography stepping process is also very important. Any semiconductor manufacturing, it need not be emphasized, that you have to give a lot of attention to clean room utility and you have to monitor the level of cleanliness, in the clean room regularly, every half hour. There are certain standards to maintain the clean room conditions in large industry.

Now, why are we worried about clean room if there are dust particles in the air? If a person is entering the lab or the factory, he carries with him a lot of dust from the hair, from the cloths, footwear and so on. So, you have to define the type of clothing; so, clean room clothing becomes very important. Normally, you take an air shower, before you enter the lab, to remove all the dust from your hair and the cloth and so on.

Now, why are we worried about clean room? Because, we are working with lower line widths. For example, class 1 - it is a classification; it says that we can have only 1 particle per cubic feet and that 1 particle should be equal to or greater than 0.5 micron is only allowed. If you say your clean room is class 1, that means you are monitoring and you are specifying that your clean room will have only 1 particle per cubic feet of the size of 0.5 micron. That is a very tough standard to maintain always. So class 1 will be very expensive to maintain.

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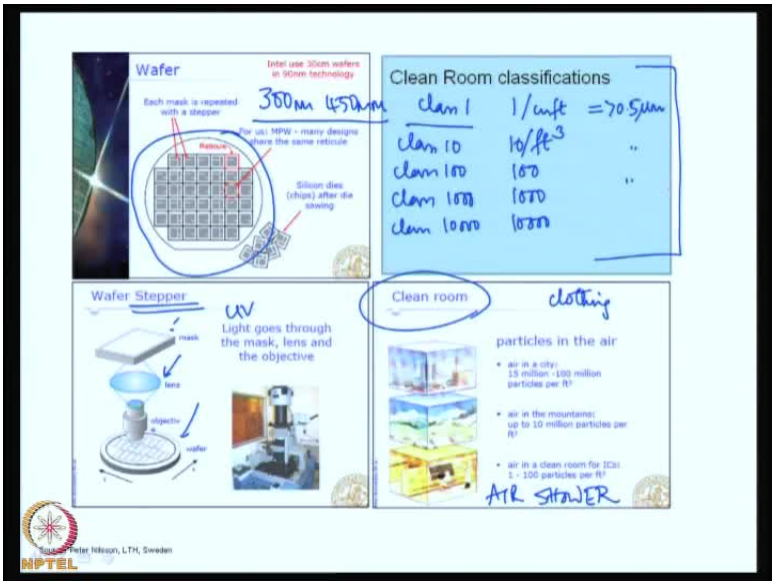

Then comes class 10; that means you can allow ten particles of the same dimensions, per cubic feet. Then comes the next classification class 100, where 100 particles per cubic feet of the size 0.5 micron, equal to or greater than, is allowed; then comes class 1000 that means 1000 particle; then class 10000 - 10000 particles; beyond that, it is not a clean room for certain areas in the semiconductor manufacturing. In semiconductor manufacturing, you can also define, for different sections of the equipment processing, different classes, but for imaging, especially the photolithography, you need to have class 10 or class 1 clean room.

So the cost of wafer fab is one side of the coin; the other side is how to maintain your clean room regularly; because, any dust getting in to the wafer fab processing is going to damage the entire yield equations.

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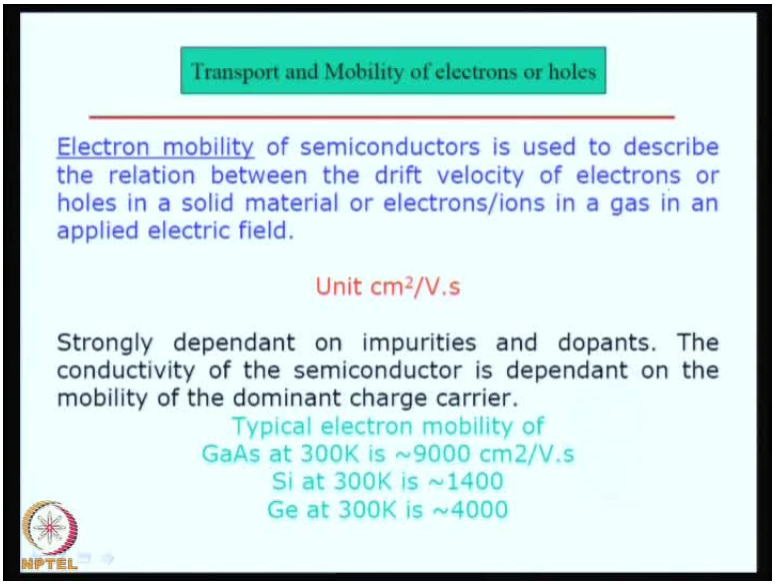

Now, I talked about transport and mobility of electrons or holes. Electron mobility of semiconductors is used to describe the relationship between the drift velocity of electrons or holes in a solid material or electrons or ions in a gas in an applied electric field; the unit is centimeter squared per volt per second; and it is strongly dependent on the type of impurities and dopants, you are going to add. Typical, electron mobility for Gallium Arsenide is around 9000; and for silicon at 300K is around 1400; Germanium at 300K is around 4000.

You are going to look at this physical property, when you are looking at the use of different compound semiconductors of silicon. Making the wafer, a seed crystal is suspended in a molten bath of silicon; so, the starting process is you have a molten bath of silicon in which a seed crystal of pure silicon is now suspended; and then it is slowly pulled up at a very small rate; it cannot be very fast because, you are now growing the single crystal; and it is slowly pulled up and it goes in to an ingot of this type, as you see here in this picture.

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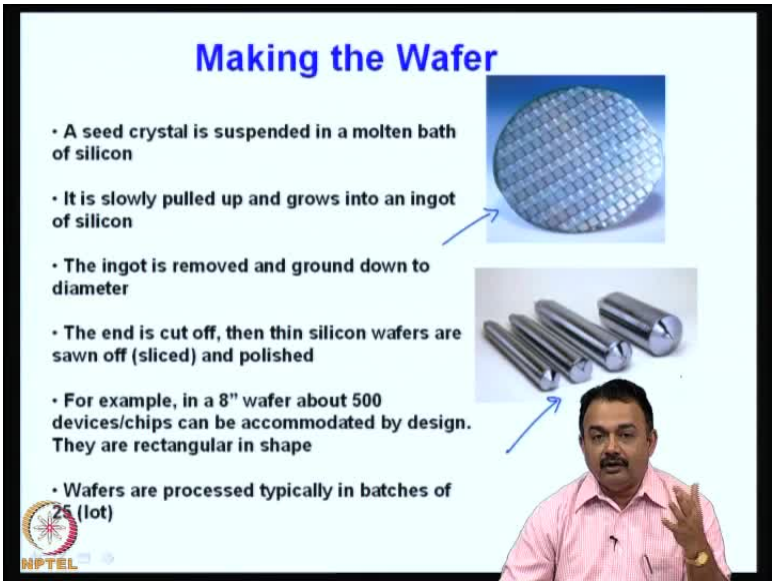

This ingot can be very large and finally, after you have got the desired length of the ingot, the ingot is removed and it is ground to whatever diameters you require, whether it is 300 mm or 450 mm. For example, in a 8 inch wafer, about 500 devices or chips can be accommodated by your intelligent design; and the all of these dies are rectangular in shape.

Wafers are processed typically, in batches of 25; you call it as a lot. Wafer Terminology: if you look at a wafer like this, which I have shown as an example, some of the sections are marked here; here, this (Refer Slide Time: 44:40) is known as a chip, a die, a microchip or a bar; then 2 are the scribe lines; as you see here these lines are very important to singulate the dies; you use these lines to singulate; and these lines are very important because you have to dice the wafer only along these scribe lines; you cannot

move away from these lines; so, these will have a certain thickness and your dicing equipment has to slice only along the scribe lines.

Then, you have engineering test die, this is normally used for testing electrical test on the wafer; instead of doing the test on all the pieces, there will be some test areas, which you can quickly, using automated test equipment, you can do the electrical test. Then you have what is known as the edge die; in edge die, always, there is a loss. So, this design by basic design, you must not have too much of edge dies, because you going to lose the capturing of the design on the wafer.

Then comes the crystal planes; you can see here, this is cross section showing you, what is the arrangement of the silicon crystals in this particular wafer; and that is one of the reasons why the lines are drawn, the scribe lines are drawn along the crystal lattices so that there is no breakage of the crystals, leading to a crack in the entire wafer; and this is known as the wafer flat.

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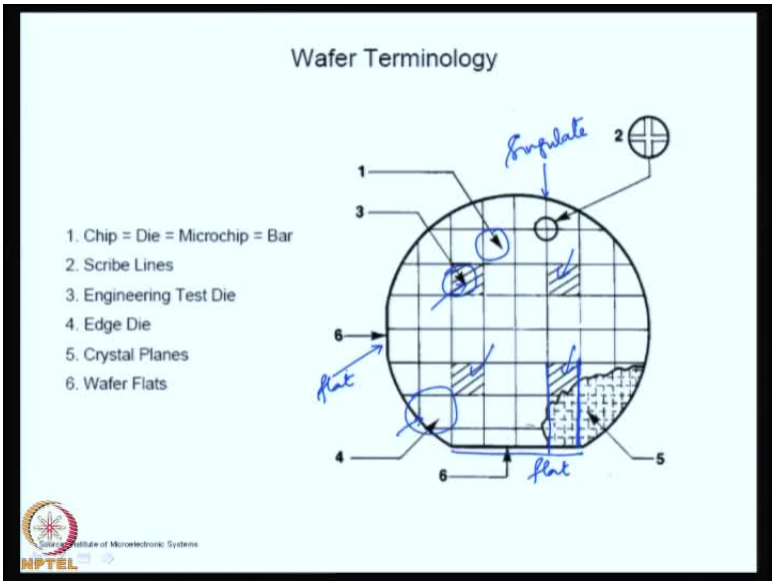

This (Refer Slide Time: 46:23) is also a wafer flat. If you look at any wafer, here, as you see there will be a section where it is flat. The flat indicates a lot of things; first of all, if you have a flat like this, this indicates that it is a p-type material and the arrangement here is a 111 type; and similarly, wafers can have secondary flats; for example, this a secondary flat and this is the primary flat.

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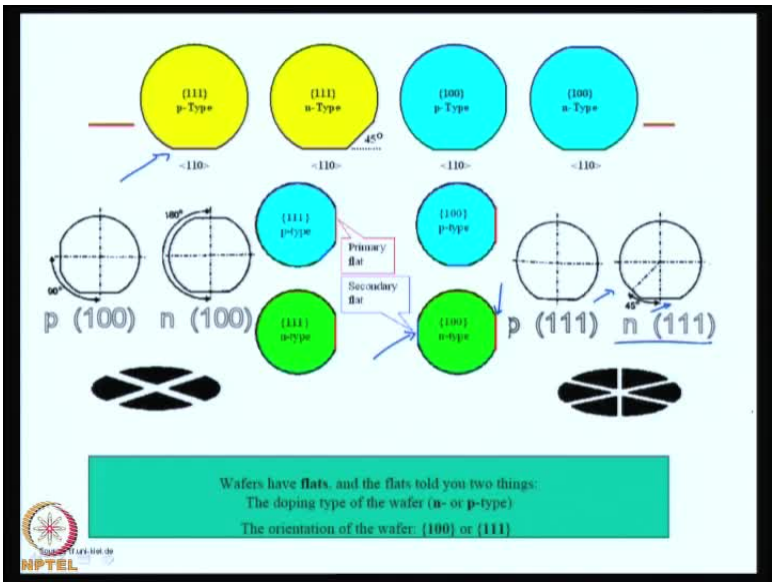

The primary flat is larger than the secondary flat; it also gives certain information. For example, if you have a flat like this; the primary flat and the secondary flat like this, then it denotes that it is a n-type 111 crystal arrangement. So, why is this required? Because, the technicians working in the semiconductor fab may not be really be aware of what material or what crystal arrangement you are going to use; so, you have to go by these kind of notations called wafer flats; and these also come in handy during the scribing, the cutting process. Because you have to cut along the crystal lattices, without disturbing the crystal structure; and breaking the wafer, so wafer flat arrangements give you a lot of information about what type of material is used.

Wafer processing involves lot of processes; wet cleaning; then comes the photolithography process; then comes ion implantation or doping, which we have seen, which we are going to embed into the certain regions of the silicon wafer, either to increase or to decrease the conductivity, the mobility, charge carrying capability; then you have dry etching or wet etching, depending upon what material you are using; you can also have plasma etching or plasma ashing; then there are thermal treatments like annealing, as you know annealing is a thermal process, that is used to change the properties of the material; you can have Rapid annealing or Furnace annealing and then thermal oxidation, so all of these can be at different temperatures, depending on the materials that you are using.

Now, you can deposit metals or conductors, using Chemical Vapor Deposition, where a reaction between materials can deposit certain required chemical vapors, which can sit on the surface of the host material.

Then you have Physical Vapor Deposition, again at different conditions; then you can have Molecular Beam Epitaxy; you can also do electroplating or electrochemical deposition.

The thickness for each of these will be different. So, the choice depends on what kind of thickness you want to do. Then you have Chemical Mechanical Planarization, which is again called polishing, in simple terms.

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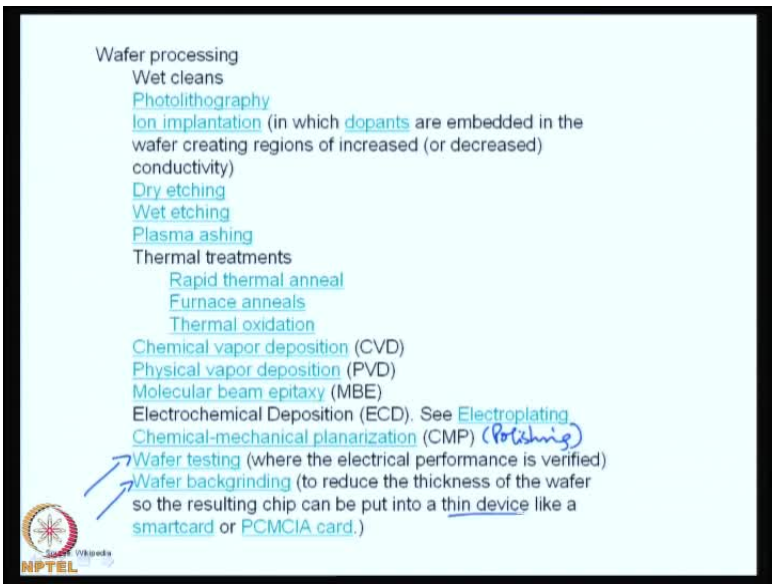

This is basically called polishing of the wafer, once the entire process or buildup is done and finally comes wafer testing and backgrinding, to reduce the thickness of the wafer, because the wafer starting thickness is very high; and you have to reduce the thickness as much as possible, so that you get a high density substrate. So, you have to reduce the thickness of the wafer and the resulting chip will be small and it can be put in to a thin device and packaged efficiently.

The back end process will involve processes like die preparation; wafer mounting; die cutting; IC packaging; die attachment like IC bonding, wire bonding, which includes subsections or processes like thermosonic bonding, flip chip attachment, tab bonding -

TAB is known as tape automated bonding; then IC encapsulation using baking or plating or simply molding and it is laser marked for identification or marking the component and finally, Trim form; and test and then it goes for packing.

That completes the steps, that are required for IC manufacturing. There are two types of packaging, as I said earlier, one is known as a plastic; the other is ceramic packaging. plastic or ceramic packaging involves mounting the die; connecting the die to the pins on the lead frames, on the package; then sealing it, after testing. The tiny wires are used to connect pad to the pins; in the old days, wires are attached by hand, but now, you have high end multipurpose and high speed machines to perform the task; so, this is typically wire bonding.

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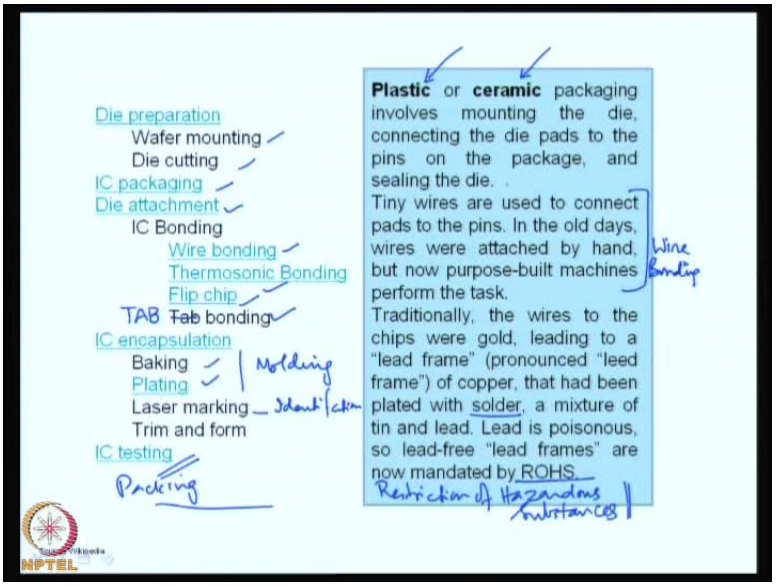

The wires to the chips are typically gold and they are connected to the lead frame, but now other materials are also being used; and then the lead frames finally, in the second level of packaging, they get attached using solder material; earlier tin lead was used; but today because of health hazards post by lead, we are now using lead free attachment and this is mandated by ROHS; ROHS means restriction of hazardous substances.

This is the path way; now, the semiconductor manufacturing processes started, if you look at the chronology or the history, today, we are comfortably sitting at 22 nanometers; our earlier generation technologies are 32 and 45; this is still not in the large scale manufacturing, but at the research level. Intel has brought out processorsr in each of

these segments; and you can see we have started with 10 micron in 1971 to something like 130 nanometers; 0.18 technology was very popular in those days; and then we have 0.13 by year 2000 and today, we are targeting 11 nanometers by 2015.

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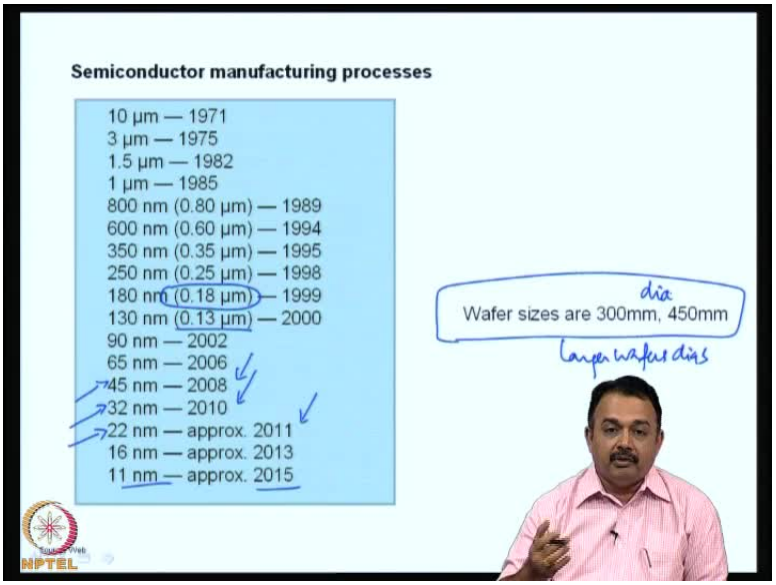

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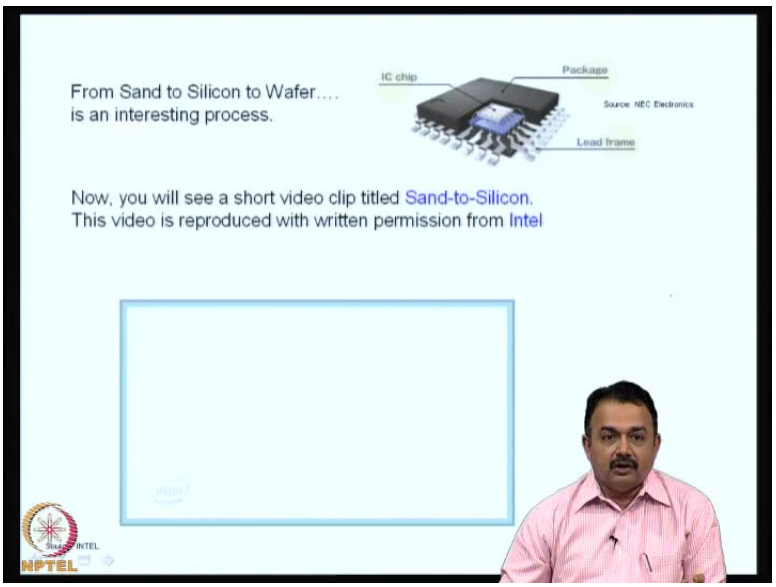

That is the kind of growth that we have seen and wafer sizes, I mentioned, time and again, we are going into larger wafer diameters; this is the diameter of the wafer, so that you can accommodate more chips.

We are now coming from sand to silicon to wafer; that is the entire process, What I want to show now, is a short video clip that is titled sand to silicon, produced by Intel and this is now being played here with permission from Intel.

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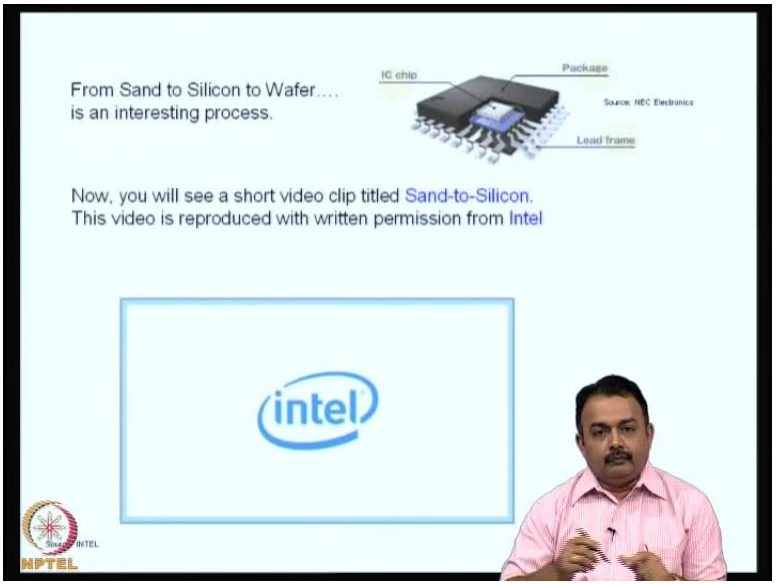

As you have seen here, this is an excellent video, which tries to impress upon us, how the utilization starts from using sand to manufacturing high grade, electronic grade pure silicon; and then that is converted into a wafer; and from the wafer how a singulated die like this, a single die is formed; and you can see in this picture here, very clearly, how the wire bonds connect from the bond patch of the die to the lead frames and this is the package.

So, in this class, we have covered, to look at the what a front end process is; and what a back end process is; we have tried to list the process steps; and we are now seen what a package will look like in the inside; so, in the next class, I will give you a detailed description of the entire process steps, that we have try to list today; and we have seen what goes next, after fabrication; we will see the packaging aspects.

Thank you.