An Introduction to Electronics Systems Packaging
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Module No. # 10
Lecture No. # 42
Exclusive chapter wise summary

This is the conclusive chapter or module on this NPTEL video course on electronics systems packaging. So far, we have seen various modules and lectures in those modules covering various aspects of electronic systems packaging.

We have covered a wide variety of topics starting from the basic semiconductor fabrication to system level issues. This is basically sensitizing all the participants in this course to the rudimentary topics of electronic systems packaging that looks very essential for the industry today.

As we have seen over the lectures that there are a wide variety of topics that can be covered in electronic systems packaging because this is multi disciplinary in nature. What we will now do is to quickly recap the various topics that we have covered and summarize the takeaways from each of these topics and conclude this final lecture.

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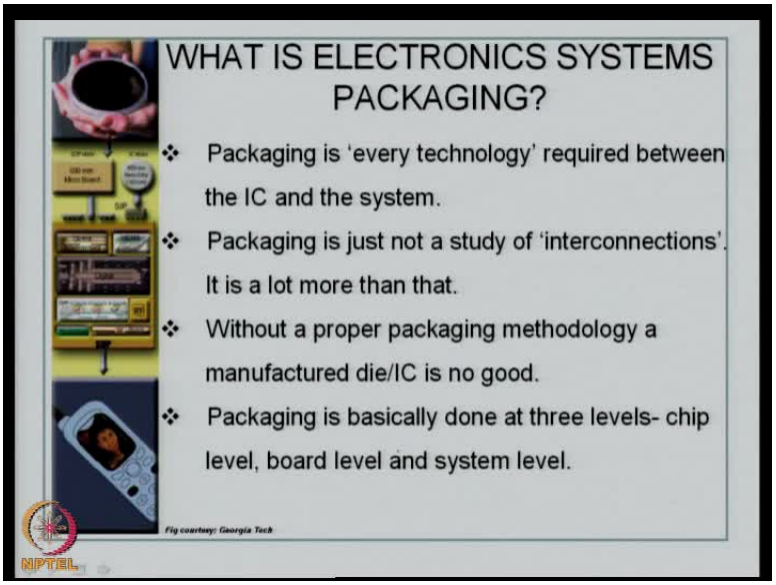

Firstly, in the beginning, we have tried to define what is electronics systems packaging; if you recall, packaging is every technology required between the IC and the system.

Packaging is just not a study of interconnections; it is much more than that and we have tried to look into the various technologies that dominates from the IC level to the system level. We have also seen the importance of various packaging methodologies and concluded that without a proper packaging methodology, a manufactured die or an IC is no good.

Therefore, packaging is basically done at three levels: chip level, board level and system level. We have seen in the beginning that it is very difficult to pinpoint and write a definition for packaging because we have to cover various technologies that are required between the IC and the system.

As a beginner, you would have seen that packaging is just not about copper interconnections, because we need talk about various levels of packaging - the IC level, the board level, and the system level; it is much more than just a copper interconnects. The performance of these interconnects are dependent on various factors - material issues, process issues, and so on, besides electrical and thermal issues being of prime importance in the reliability of an electronic product.

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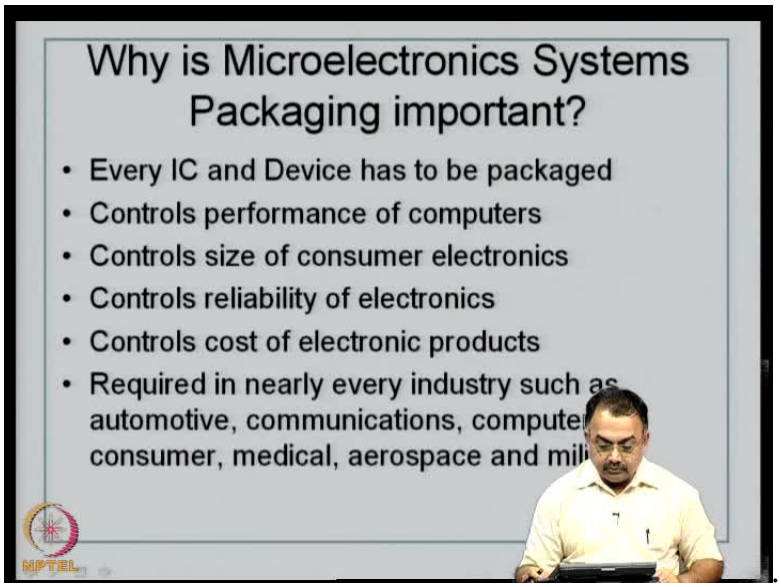

If you want to look back and try to see what we have digested in terms of the material in the initial lectures, we have tried to define what is microelectronic systems packaging and why is microelectronic systems packaging important. The important points that are covered here in the slide are that every IC and device has to be packaged.

Now packaging in some sense, controls the performance of systems, computers for example, small systems, handheld products, large systems like servers and various power electronics systems which are large in size, but where packaging also plays very important role in terms of choice of components, the device assembly, and so on.

Packaging controls the size of the consumer products, which is very true today; as you are witnessing major evolutions in terms of new products that are seen in the market today and technology revolution in terms of miniaturization, feature size diminishing, and host of new materials being used even in the consumer electronics arena.

Reliability of packaging is very important and together with the choice of materials, the right and appropriate material, we have to as designers, look at cost of electronic products, because when you look at product design at the industry level, you have to meet the satisfaction of the end customer in terms of reliability and at the same time cost effectiveness. Packaging is a requirement in every industry today such as automotive, communications, computer industry, consumer, electronic goods, medical equipments, aerospace, strategic, and military sectors.

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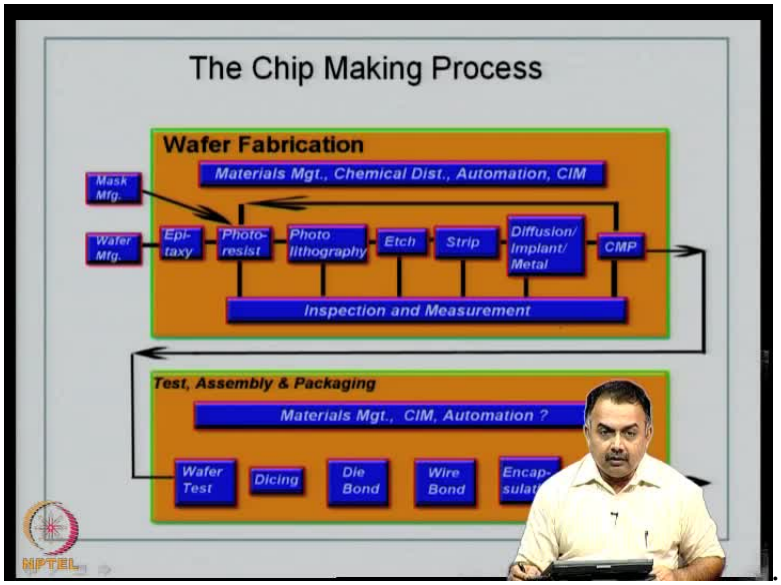

You would recall this slide, which we discussed about the semiconductor manufacturing process of the chip. Although this segment in-exclusively does not belong to the electronic systems packaging concept, but when we talk about IC packaging, it is always better to know the IC manufacturing process sequences including the materials and the equipment issues that are associated with wafer fabrication, because there is always a great technology change happening every two years or every five years in terms of packaging technologies that are being available for the end customer. Therefore, we will talk about wafer fabrication, which is the front-end process and we have seen how issues like the size of the wafer and the dimensions or the technology, line width that is being used by the designers for the chip manufacturing becomes very critical.

You can see the front-end process starts with the mask manufacturing and then the wafer from the ingots being sliced to the required dimensions and then the allied processes like selection of the photoresist material, the photolithography process as such which is the most challenging part in the front-end process, then comes the diffusion or implanting dopens into the structure of the base material like silicon or other compound semiconductors and then finally, getting the wafer done after the required doping process and the planer assertion process, inspection and measurement, and then comes the test assembly and packaging the back-end process which finally, results in the first level interconnect typically a wire bonding process and then getting a known good die KGD as you are now aware of.

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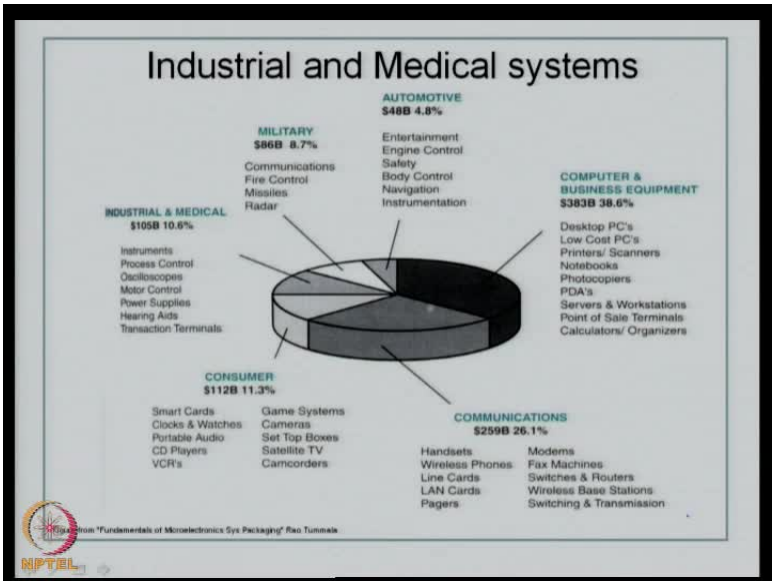

The industrial and medical systems or product packaging in general, involves various sectors. The major component could be computer and business equipment, then comes the communications systems engineering, then comes the consumer and industrial and medical systems, military and automotive being the other areas where the products go into a large consideration about electronics packaging systems design involving electrical and thermal.

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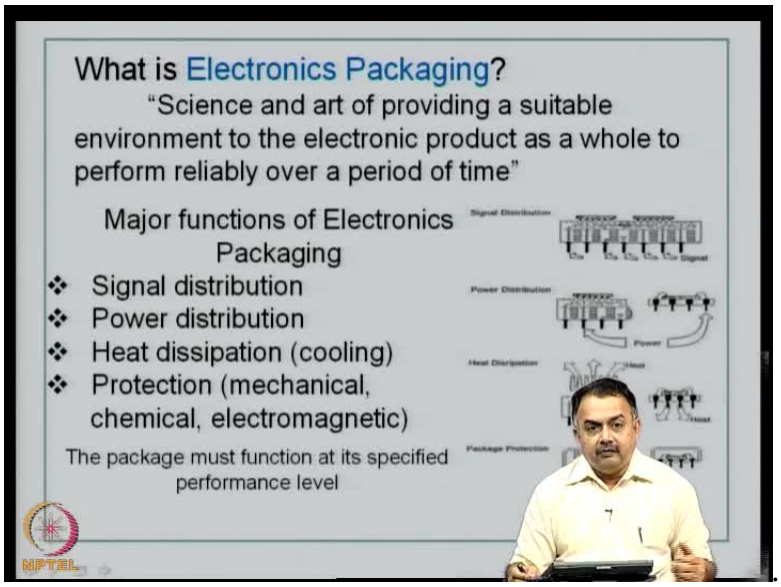

We try to summarize what is electronics packaging and we define in such a way that it is understood by the various multidisciplinary groups that work in packaging; science and art of providing a suitable environment to the electronic product as a whole to perform reliably over a period of time. This could involve design issues, because if you look at an electronic product, it starts with design, electrical test, fabrication then comes both fabrication, assembly reliability measurements, and so on.

The major functions of electronic packaging are signal distribution, power distribution, heat dissipation, that is cooling issues of electronic equipment, protection, mechanical chemical and electromagnetic and the package must function at its specified performance level. So, this take away from this slide is that it is difficult to find a definition for electronics packaging in a text book, but if you look at the product from the product stand point, we are interested in the reliability of a product and therefore, providing the

required impact on the product would mean you have to consider various issues from design to fabrication to assembly and then test.

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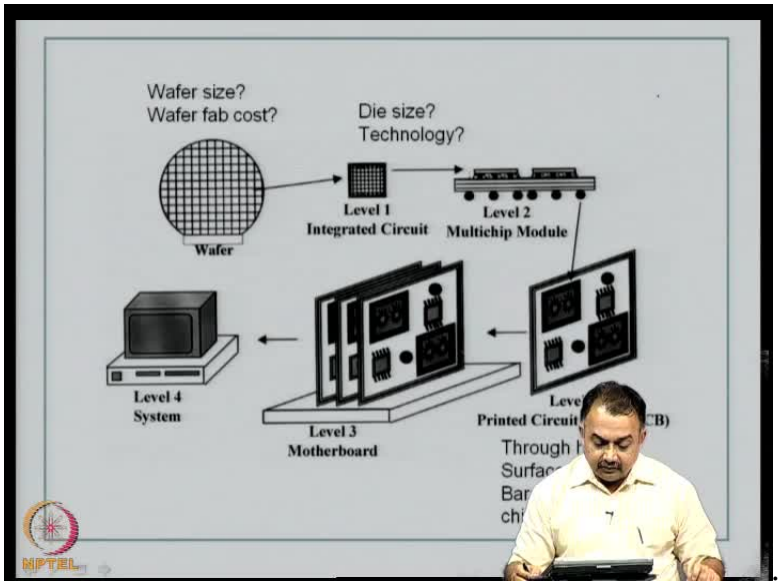

This picture in the initial lectures would have introduced you to the levels of packaging and level one involves chip level interconnects, level two involves board level interconnects and level three would be the system level. If you dig into the subareas then you try to define level one as integrated circuit then you have the starting wafer material, you have the multichip module coming out of the single chip modules that are being generated at the first level. Then comes the Printed Circuit Board, many Printed Circuit Boards can be assembled on a mother board and these are the daughter boards and this is again the level three packaging. Then you have the system level packaging, but typically broadly, you can talk about chip level, board level, and system level technologies.

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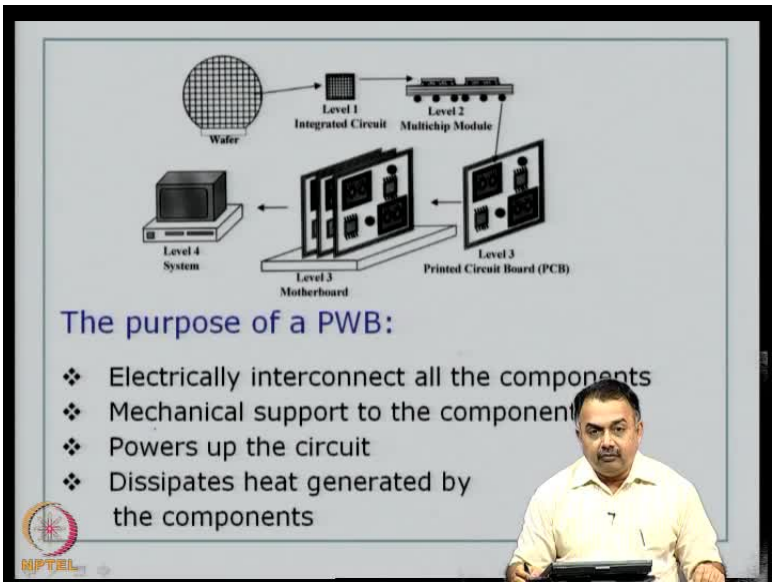

We have focused a lot in this course on Printed Wiring Boards which is the second major level of packaging that we can consider, because today Printed Wiring Boards themselves can be called as systems, because they perform system functions. It could be analog, digital, or it could be mixed signal high bandwidth. There are other issues like EMI, EMC built on the substrate and making it compatible with various operational frequencies and so on.

So, the purpose of a Printed Wiring Board is to electrically interconnect all the components. Mechanical support to the components is provided by the PWB, it powers up the circuit and dissipates heat generated by the components; accordingly the materials have to be selected.

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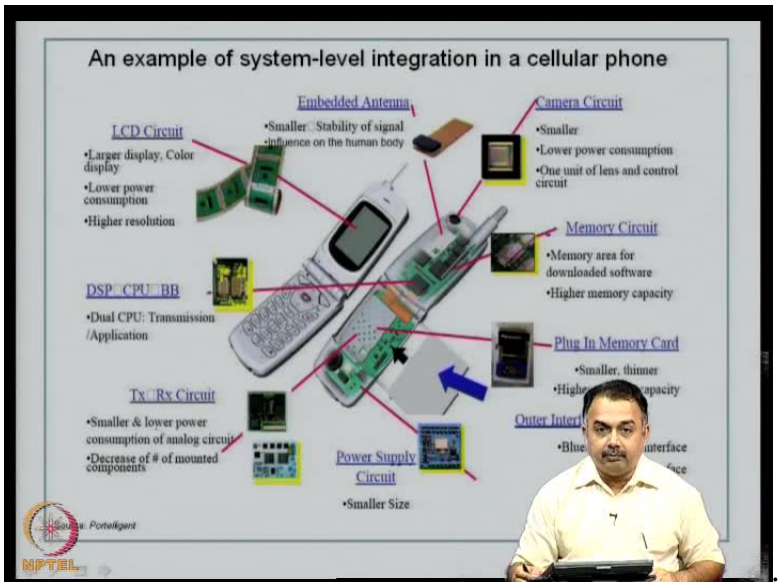

Now, this would be an example of system level integration in a hand held product. A miniaturized product that is globally very sensitive in terms of market upheaval and so on, the mobile phone, because the percentage of mobile users across the globe is very high. Therefore, features like the size, the shape, the color, including the mechanical packaging aspects, and the cost become integral to the mobile phone industry.

This picture will give you the kind of complexity involved in the system level integration in a cellular phone. There are various segments as you can see, there is for example, the camera circuit, the memory circuit, plug in memory card, outer interface circuit, power supply to the system, transmitter receiver circuit very important and all of these critical areas require lot of design considerations in terms of package choice, simulation from the electrical stand point as well as thermal.

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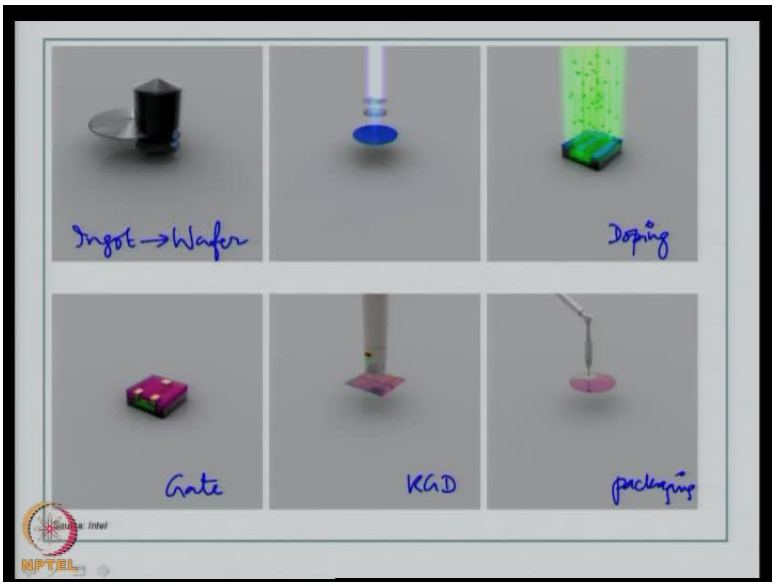

This is basically a quick bird's eye view of how we started with the wafer or an ingot to get a wafer and then the doping process to get the required electrical functions, and then formation of the gate and the metal plating that is required at the gate. Then comes the testing to qualify the die as a known good die and then comes the packaging. So, this is in this six pictures trying to present in a nutshell the front-end to the back-end process.

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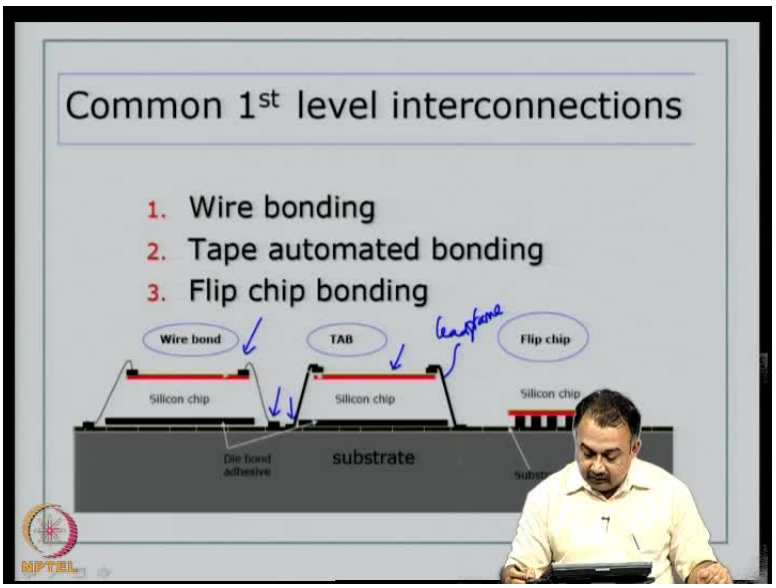

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We have seen what the first level interconnections are, they are wire bonding, tape automated bonding, and flip chip bonding. You know what is a wire bond; there will be gold or aluminum wires that will connect the bond pad on the die to the bond pad on the substrate.

Similarly, you will have lead frames in a tape automated bond that will be available on a plastic polyimide tape and then you have the die coming here and aligning with a first level bonding or inner lead bonding and then you have a outer lead bonding here, that will complete the first level interconnect. Flip chip is very current, although it was invented by IBM way back in 1963, the usage of flip chip today in terms of being part of a BGA or a CSP is highly market sensitive, there are large volumes for flip chip manufacturing and usage. Here you can see a flip chip illustration where the solder bump in the die is placed on the substrate, registered properly and this is the bare die and then the first level interconnection is done by thermo compression bonding or by reflow process.

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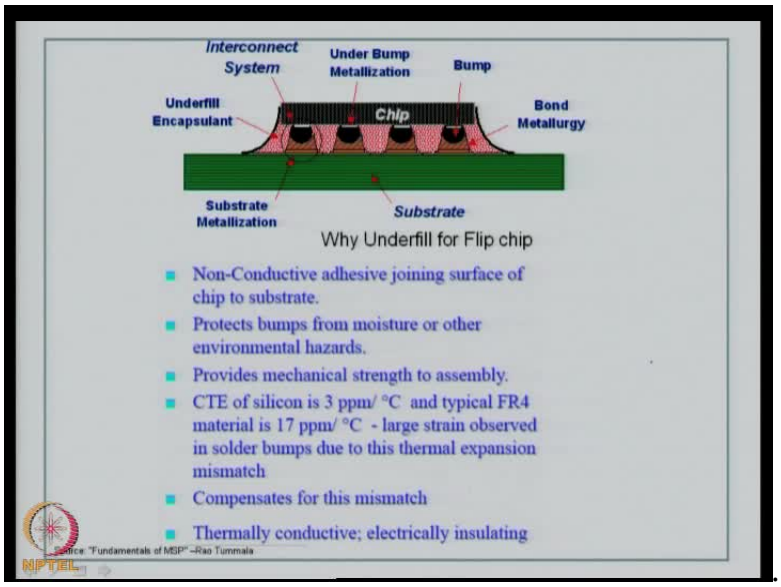

So, these are the common first level interconnections. Once again I want to emphasize here that flip chip is being used in many packages today we have seen that and how substrate and the solder material that are being used for the bump formation become very critical in the functioning of the flip chip in a package. A flip chip can be used without a

package directly on a board or a flip chip can be part of a BGA system which is a plastic packaged or it could be ceramic packaged.

So, you can see a figure here, where there is a die, and then there is a bump and you have underfill encapsulant being used in the space between the die and the substrate. So, this is a substrate, it could be an FR4 or FR5 material depending upon the specifications of your product and then underfill encapsulant is used, when you use a bare die on a board to prevent the thermal mismatch between the silicon die and the organic substrate; so that the reliability is increased.

In our course, we have emphasized the use of flip chip today in current products and design. Underfill becomes a very important material for researchers and the volumes are increasing in terms of usage. Underfill is basically a nonconductive adhesive joining surface of chip to substrate; it protects the bumps from moisture or other environmental hazards, provides mechanical strength to the assembly, and then it takes care of the CTE mismatch that I talked about between the silicon die and the organic substrate. It is thermally conductive, takes care of the heat issues and electrically insulating.

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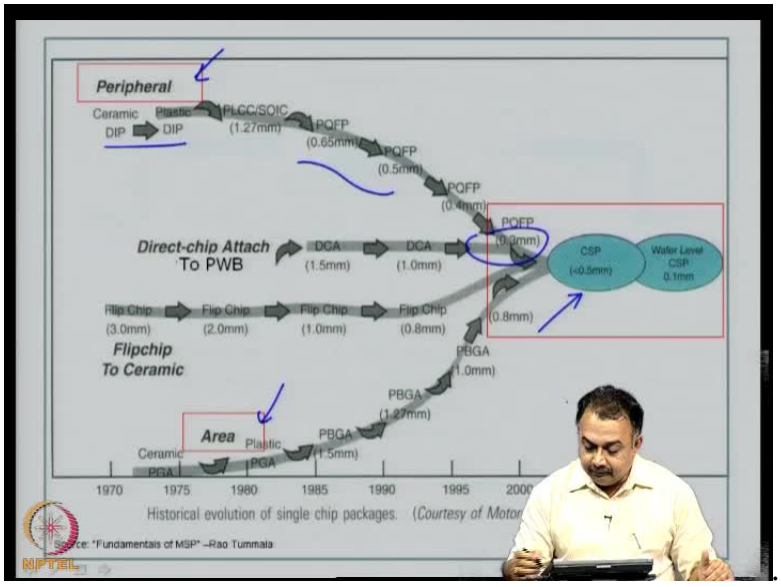

If you look at the growth or evolution of packages, we have spent a large amount of time in looking at the various packages in this particular course. We talked about peripheral packages and we also talked about area array packages. These are the different varieties of packages that are still available in the market. We started with the DIP package, we

have moved to QFPs and then you can look at the pitch, it is about 0.3 mm convergence. If you look at other technologies area array plastic technologies, BGA, plastic BGA, and then we now have what is known as a chip size or chip scale package technology and then the wafer level CSP where the pitch is 0.5 mm or less. So, a CSP can be done at the wafer level which means that you can package the die and then singulated later from the wafer compared to the conventional process of singulating the die and then packaging the individual die.

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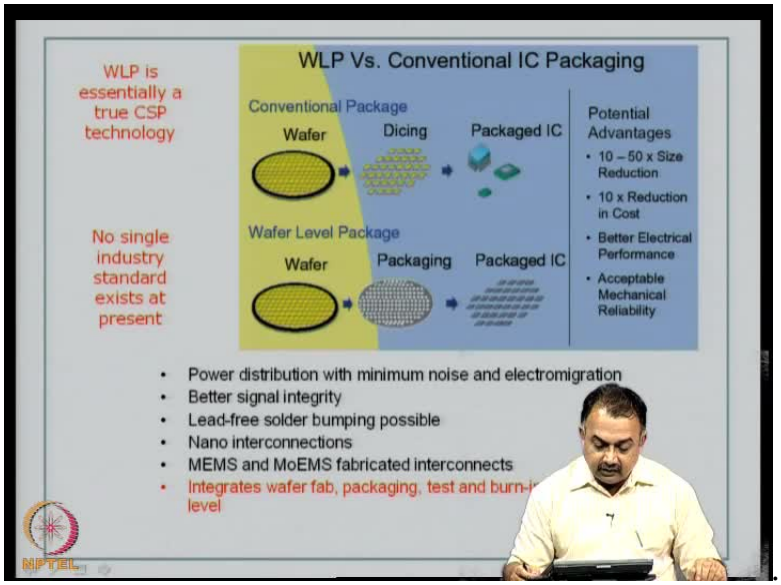

As you can see in this picture here, a conventional package, we have the wafer then the dicing is done and then it is packaged individually, whereas the wafer level the packaging is done at the wafer and then the packaged dies are than singulated. This is one of the most current technology, the wafer level packaging or wafer level CSP technologies, and there are a lot of benefits as you have seen; better signal integrity, lead-free solder bumping, possible nano interconnections, and then integrating this process for the fabrication of a MEMS devices and interconnects.

Although the volumes are less, it is definitely a big step towards nano interconnections and small devices.

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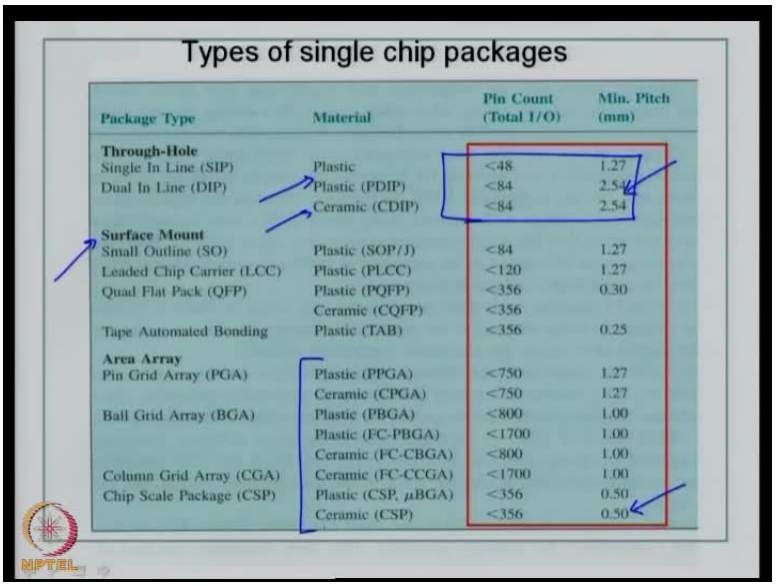

This is a glossary of the single chip packages that we have seen. We have seen a host of through-hole components like SIP, single in line package, DIP, dual in line package, and you have plastic packages or ceramic packages you have a look at the pin count and the pitch. Initially the pitch has been very high 2.54 mm and then today we are talking about 0.5 mm or less in the case of CSPs.

Then, comes the other classification of surface mount devices; you have various classifications like small outline package, leaded chip carrier, quad flat packs, and so on . In the area array package, you have a pin grid array and then the ball grid array package then the column grid array and chip size package. You have different varieties of BGA packages that could be used based on your application and electrical requirement.

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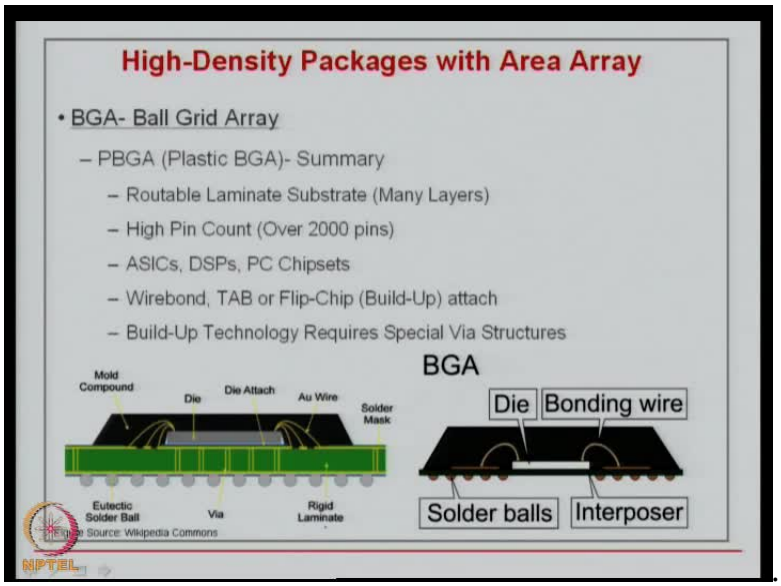

BGA is the work cause of the industry as I have mentioned. You can build high density designs or system level Printed Wiring Boards with BGAs. The volumes of manufacturing for BGA are very high. Plastic BGA again is highly used by the industry today. Typically you will see a multilayer organic substrate with high pin count and they could be used in the functionalities like digital signal processors, chip sets, and so on. You could have BGAs in terms of wire bond, TAB, or flip chip. I have emphasized in the module on Printed Circuit Board technology that the build up technologies is highly essential for these kinds of high density packages.

Here again, I have presented to you the cross section of a BGA, where you could see the high density interconnect substrate, HDI and then you have BGA solder balls, this is a BGA solder ball and then the various components like the encapsulant and so on.

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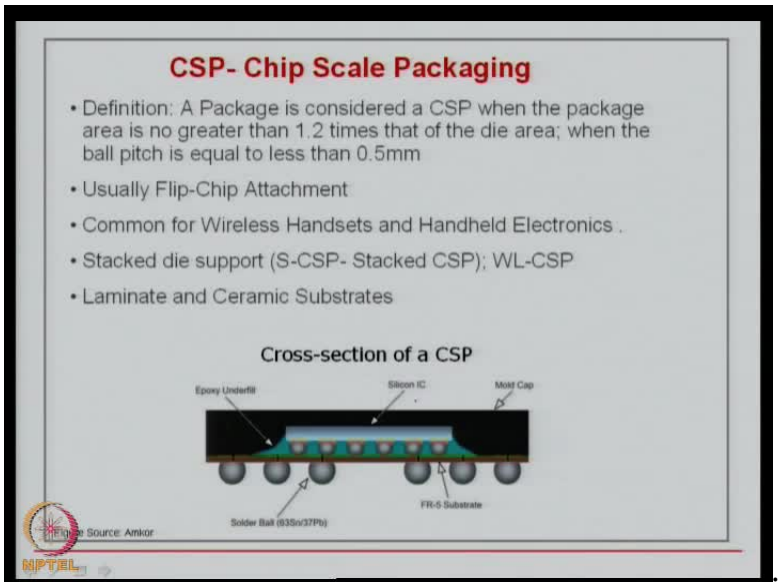

Coming back, chip size packaging or chip scale packaging is basically when the package area is no greater than 1.2 times that of the die area, when the ball pitch is equal to or less than 0.5 mm. Usually it is a flip chip attachment and you could work with laminate or ceramic substrates.

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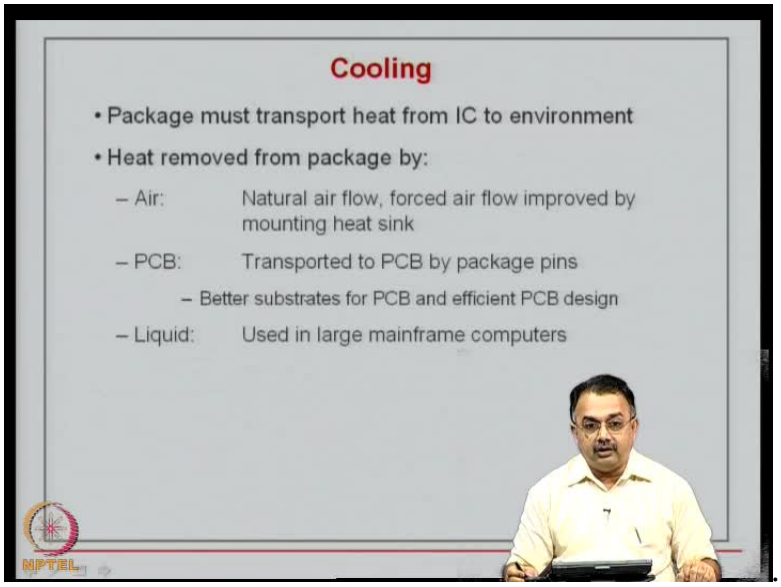

Cooling is a very important issue and basically a package must transport heat from the IC to the environment. That is the main concern of packaging in terms of a thermal design. The heat removed from the package is basically by air, natural air flow or a forced air

flow improved by mounting a heat sink on top of the package or attaching a fan on the Printed Circuit Board to remove the air quickly from the surface of the device.

So, in heat sinks also you could have various configurations of heat sink basically to increase the surface area of the heat sink. Use the appropriate material like aluminum or modified oxides of aluminum and then try to provide large surface area to remove the heat from the surface of the die or the package. The PCB material itself could be used if chosen correctly, a material to remove heat from the package, the solder joint to the external environment. So, as a designer, you must be able to understand the properties of PCB materials for efficient PCB design involving thermal issues. But in the case of large systems, a few companies have even attempted liquid cooling although it is going to be pretty expensive.

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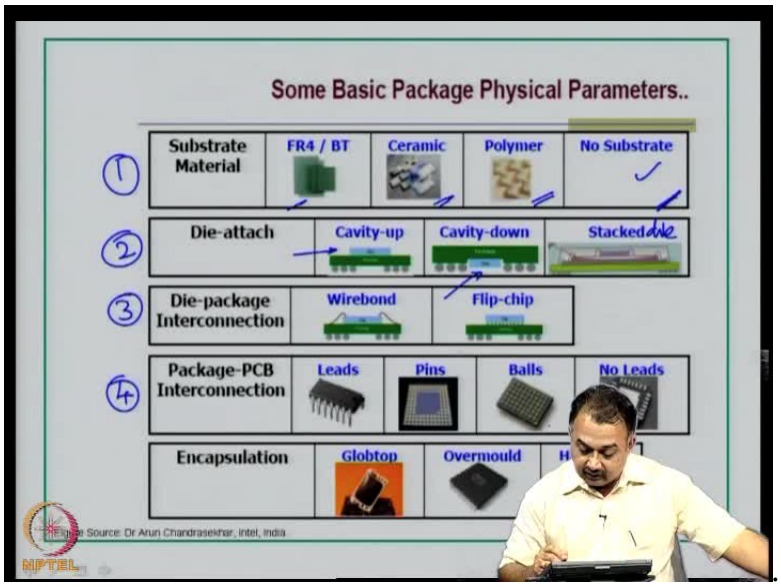

Basically as far as the packages are concerned, you are interested in the following parameters: the first one is the substrate material, you could use organic here, FR4 or a BT epoxy, ceramic, polymer material or no substrate in the case of a resin package where you do not typically have a lead frame or something like that to hold the die.

Then you have the die attach material; in the case of a no substrate typically, if you take a dip package, you will have a base substrate with a lead frame but then you can avoid these using a organic resin molded type of a fabrication. In the case of a die attach material or process, you could have a cavity up process where you can see the die here

the configuration or a cavity down, accordingly the substrate is fabricated so that you can provide avenues for cavity down attachment of the die and then you could have a stacked die configuration.

Then the other issue is die to package interconnection; it could be a wire bond or a flip chip. TAB is less common. The volumes are less. Then you have package to PCB interconnection where you could have leads or pins like a PGA, balls like a BGA, or a CSP or no leads typically QFN kind of a package. Then the other issues encapsulation, whether you are going to use a Globtop epoxy material, Overmould that package formation or Hermetic sealing which is required for certain applications.

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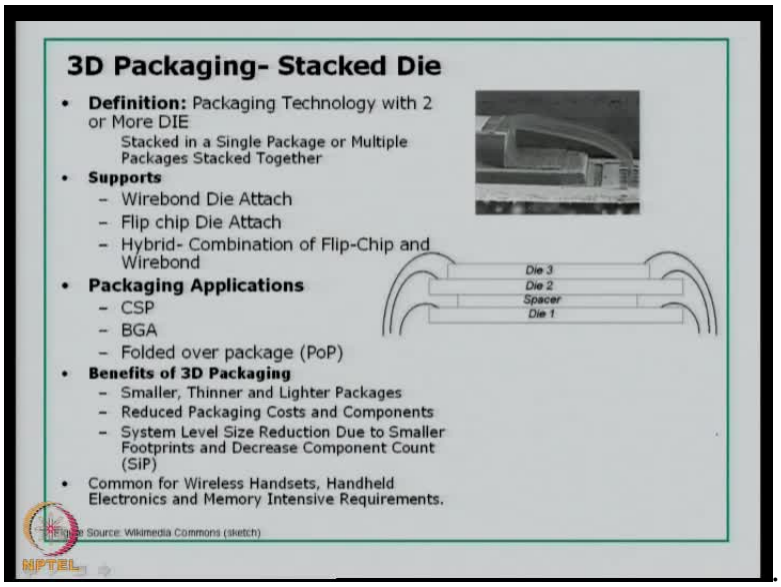

The current issue is 3 D packaging or stacked die information to improve the IO count in a smaller area and vertically integrating large number of die. It could be different functionalities built on a single substrate or platform and then interconnected along the periphery between various dies and then they could have a common package. Typically you could have single chip module, multichip packages stacked together but stacked in a single package. It supports wire bond, flip chip die attachment, and you could have a hybrid combination of flip chip and wire bond as we have seen in the lectures, various illustration, and photographs.

Packaging applications - It could be used for CSP, a stacked CSP, or a stacked BGA, or a package on package, or folded over package and these are highly integrated so that they are used in hand-held products, wireless handsets and so on.

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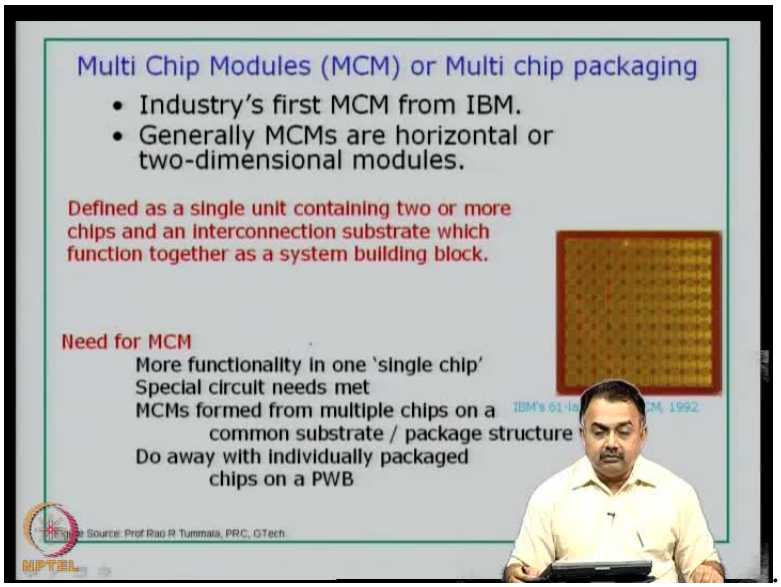

We have also talked about multichip modules as compared to single chip modules. Here on a common substrate, you have various die mounted and interconnected and then they function together as a system building block. So, the IOs also will be large in the case of multi chip module and the requirement is that you could mount this just like a single chip module on a system level Printed Wiring Board or a ceramic substrate as the case maybe and special circuit requirements can be met by integrating large number of die on the same substrate. Ideally, you could do away with the various single chip modules or packages. The individual dies can be different functionalities also.

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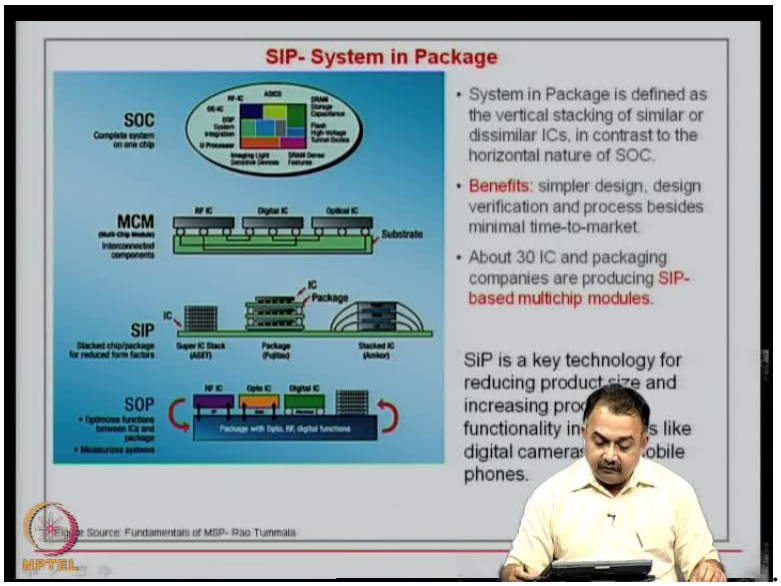

The other concept we have seen is a System in Package, which is defined as a vertical stacking of similar or dissimilar ICs in contrast to the horizontal nature of a system on a chip or a multichip module again which is requiring more area on the substrate. We talk about vertical stacking in a system in package. About thirty IC and packaging companies are producing SIP modules.

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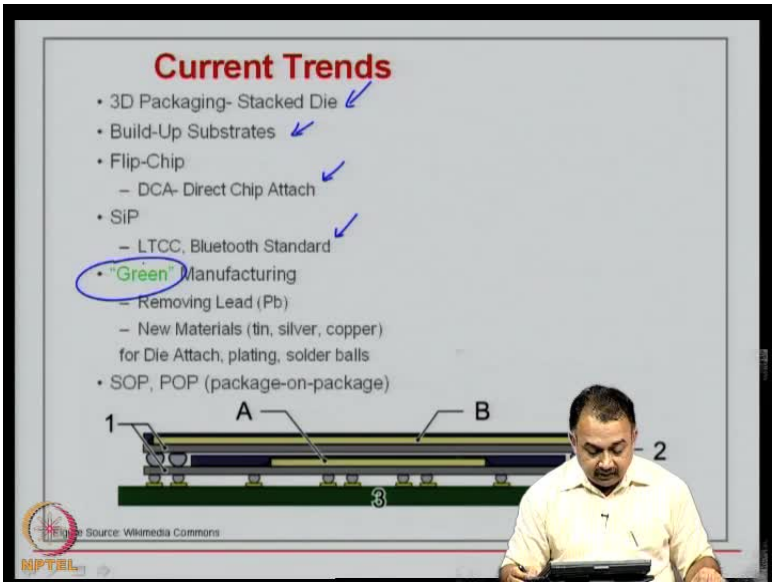

To summarize, the initial chapters - current trends is 3 D packaging, build up substrates, flip chip, direct chip attach, System in Package, and towards the end of this course we

talked about green manufacturing. So, as a designer, you should also think about removing lead from your assembly and try to use new materials, look for new concepts in plating or die attach materials and so on.

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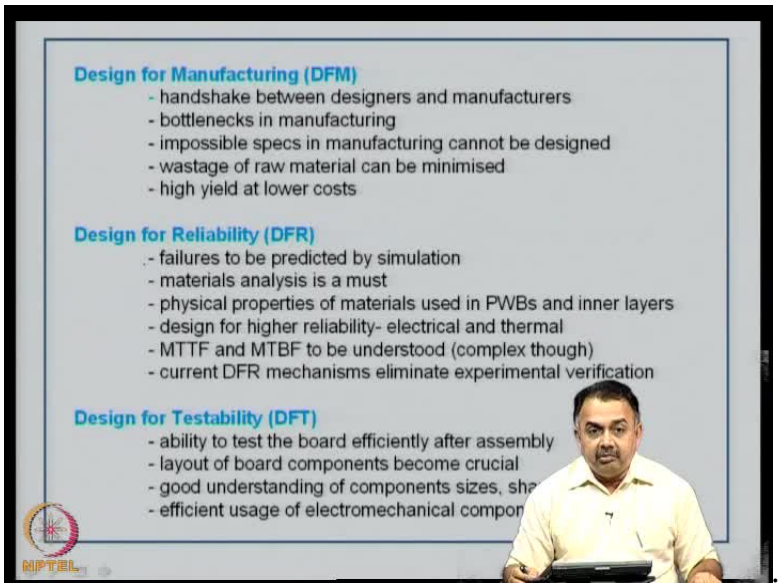

Remember these three important terms: design for manufacturing, design for reliability, and design for testability. During the CAD section of this video course, I have highlighted the importance of these terms. Why do you require a good handshake between the designers and the manufacturers? If you do not have a proper understanding at the design stage itself about the manufacturing issues, you are now going to end up with bottlenecks in manufacturing, some times impossible specs would be sent to the manufacturer which cannot be designed and that is going to eat up the cost of the evolution of a product. Reliability again related to various things right from the product conceptualization, material analysis that goes into the end product, how the materials will behave in different conditions electrical and thermal included and then comes the point of testability. Your design is no good, if you do not have a layout that is testable. The type of packages that you are choosing is key to defining this concept of design for testability

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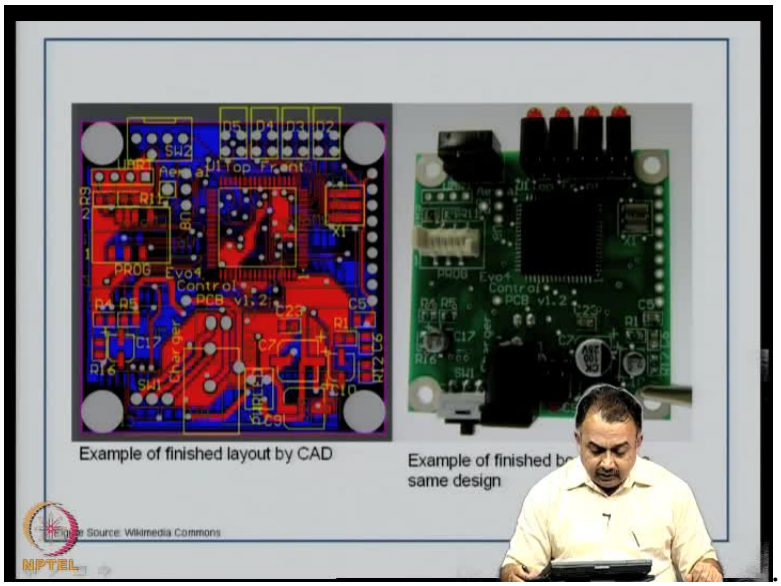

Here I have a picture of a finished layout from a CAD process. A very simple double-sided structure. You can see how a board is made from this particular design using various Printed Circuit Board processes. I have tried to highlight to you the importance of the various segments in a CAD program. Whatever be the CAD program that you are using, you have to look at optimizing various operations in CAD; you may be using a through-hole technology or a surface mount technology. Look at various issues that are available in your CAD, the library management, and then the various optimization issues, like via optimization, routing optimization, various design parameters that need to be set and so on.

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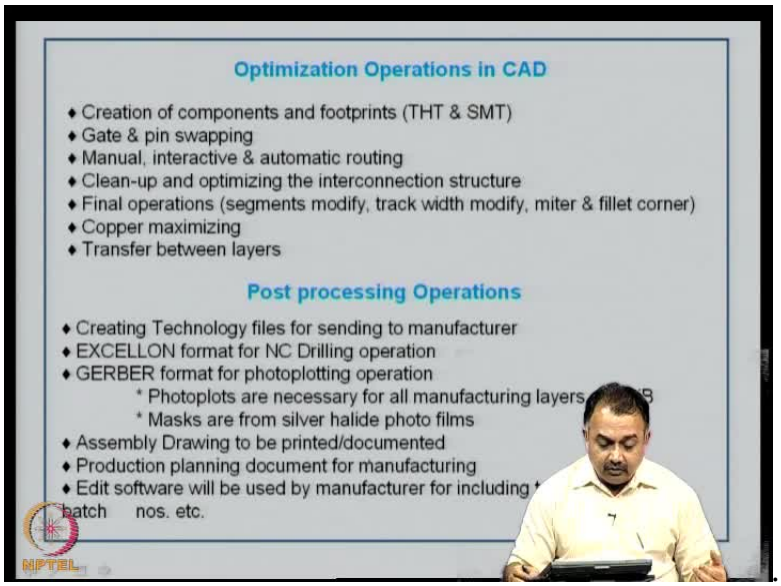

Also spend a lot of time and how you are going to generate post processing files for fabrication and assembly. This is an example of schematic, which is now converted to a final Gerber file electrical layer which is key to being sent for the fabrication of the system level Printed Wiring Board. Your system level Printed Wiring Board could be 2 layers or 16 layers or 32 layers and for each of these layers, you have to have the required Gerber file for electrical, solder mask, legend print, and various other issues like ground vias and so on.

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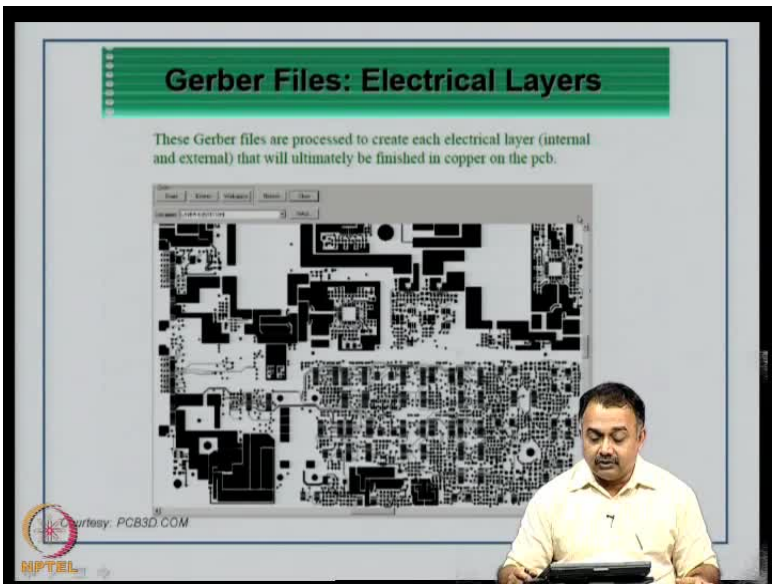

Mask fabrication or photo tool making is a key area in defining the reliability of your system. Very briefly we have seen subtractive process in the manufacturing, where etching is the key process, how well you define or remove copper, then we talked about plating as a major step in adding copper to for example, creating a micro via layer using electroless plating followed by electroplating and then you have a semi additive process.

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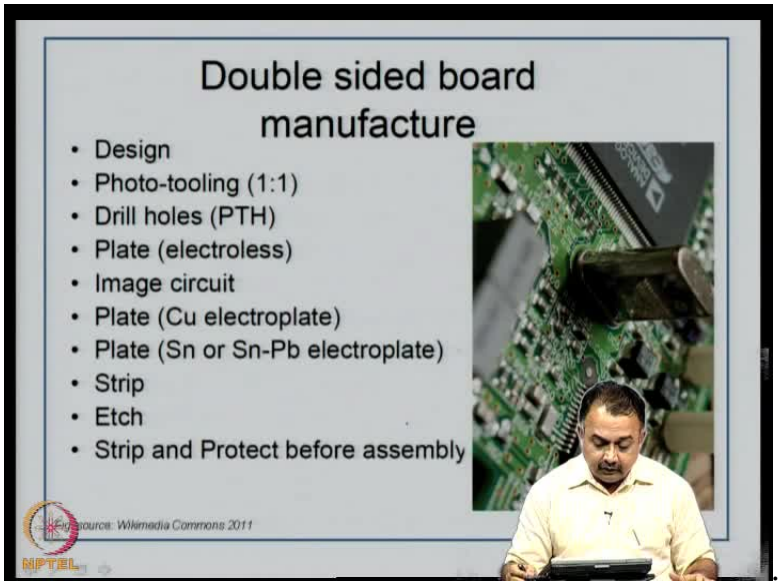

This is the process flow chart of a double-sided manufacture, starting from the design to the emphasis on electroless plating followed by electroplating, protecting the copper and so on. We have also seen how multi layer boards can be made using laminated multi layer structures, where you stack separately made layers, double sided and then stack them into a mono block in a multi layer press and then build the number of layers and finally, interconnect the top and bottom layer to get what is known as a conventional method of making multi layer boards.

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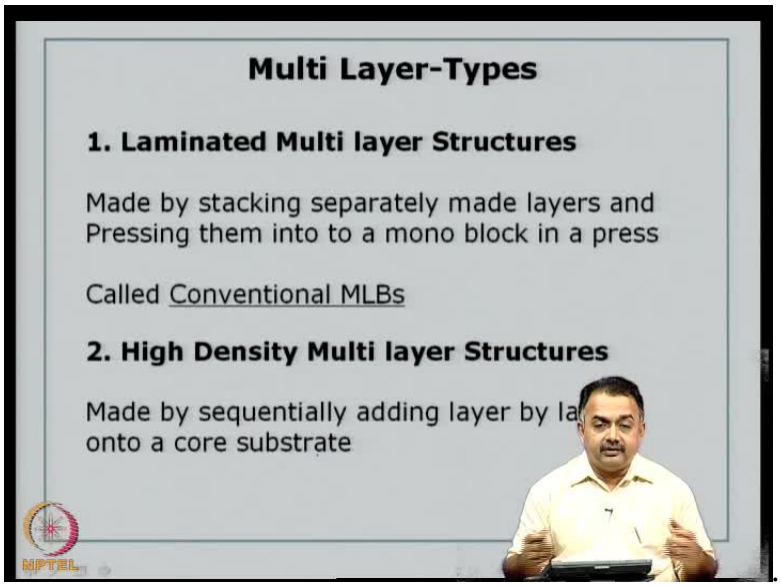

Then you have what is known as the HDI manufacturing process, where sequentially you add layer by layer onto a core substrate. The arrangement could be asymmetric, that means you could have two built-up layers on top one at the bottom and then typically it is done by building step by step various layers by the semi addictive process or a fully additive process where high density designs can be incorporated.

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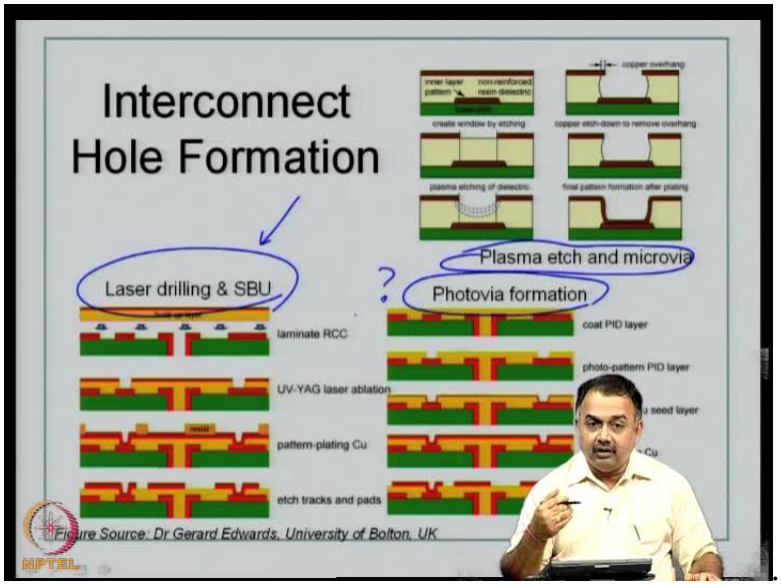

The methods of formation of via become very critical in building your HDI board. We have seen different methods, more easy is the photo via formation by photolithography,

and then comes the laser drilling methodology which is now being practiced by many industries which has become affordable compared to ten years ago. Then you have the plasma etch to create a micro via process. To me, the most common and cost effective today is laser drilling. There are limitations with photo via process, in terms of the micro via sizes that could be generated, essentially because of the light source intensity, then the type of photoresist material that is now available for such a process.

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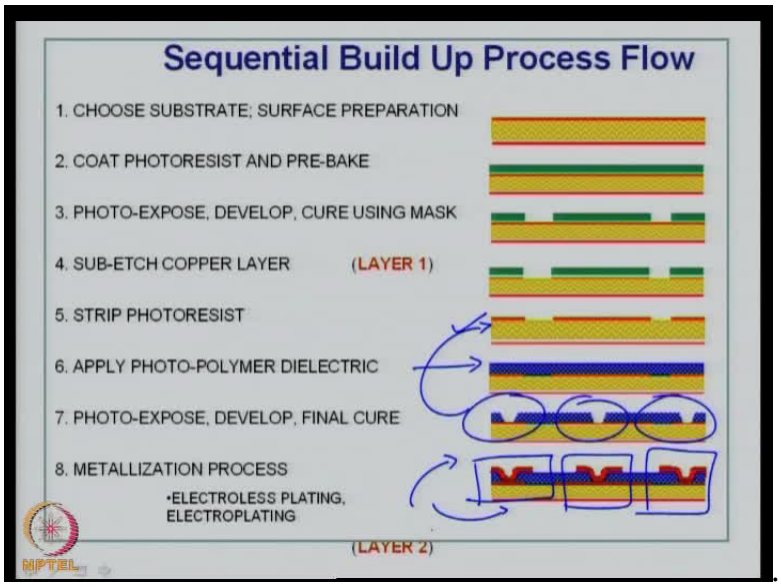

Today you have equipments available in the market to drill a micro via without a mask directly on to a substrate photoresist. This is the summary of a sequential build up process where you can see quickly at a glance, how you can coat a dielectric of your choice on to an already existing board and then build microvias structures which can be used to interconnect to your earlier build up layer. Then, you can do metallization of the individual microvias. This is a parallel process, so, the volumes in manufacturing yield could be very high and then you can build additional layers of the top or at the bottom to increase the number of layers.

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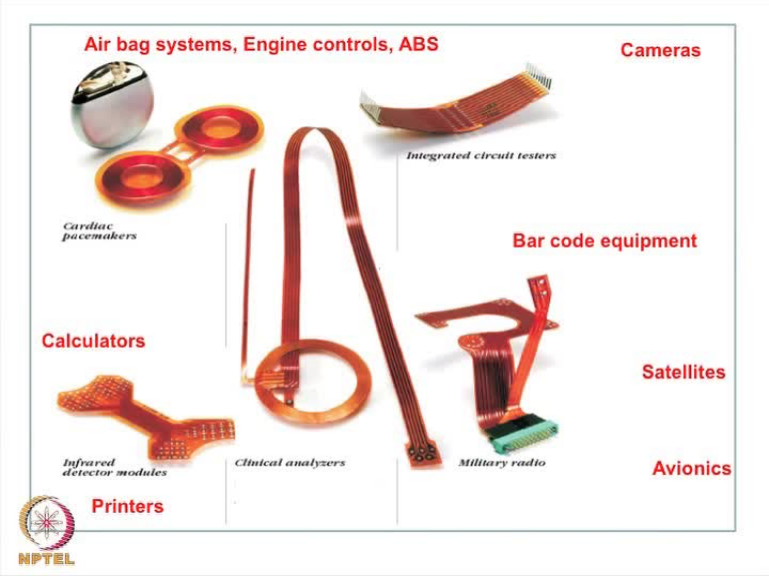

Having seen the PCB technology, we also saw what is a flux circuit. Flux circuit volumes definitely are larger, but the concentration of this segment is limited to certain areas precision areas like medical electronics, aero space, engine controls, and cameras which is highly in the handheld equipment segment. We have covered some of the important areas in flux circuits - the design, requirement for flux circuits, the fabrication sequences and methodologies for flux circuits, and some issues like what should be the bend radii for a multilayer flux or single sided flux and so on. Later, we have moved into the surface mount device technology or surface mount assembly technology.

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The summary from SMT processes is that you are going to attach components to the system level Printed Wiring Board that you have built and there could be a situation where we are going to look at various component types - it could be a through-hole component, a surface mount device, or it could be an advanced package like a BGA, CSP, or a QFN and so on.

What are methods to assemble them? Typically and very generally you have to dispense a media material that will hold your component in place. So, component placement comes next, typically using a pick and place equipment. Then the media is soft cured or fully cured depending upon the assembly process or the soldering process that follow, and then comes the important step that is the soldering or the attachment or joining of the components using solder material.

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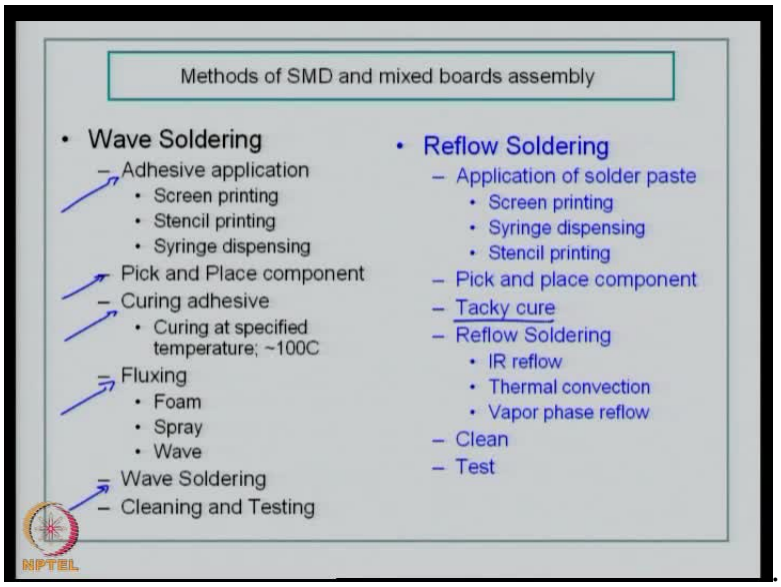

Then, cleaning of the joints and then testing. Wave soldering is a technology where you are going to add solder from a molten bath, which contains solder material. Various solder materials, tin lead typically all that usage of a tin lead is diminishing as you know. Here, the summary is, adhesive application, pick and place the component, cure the adhesive which holds the component and then use of flux and then wave solder. In the reflow soldering process, application of solder paste is the first step, either by screen printing syringe or stencil printing, then follows the pick and place methodology of the component ,tacky cure to hold the component using the adhesive that is there in the

solder paste, reflow soldering by either infrared reflow, thermal convection, hot air vapor phase reflow, and followed by clean and test.

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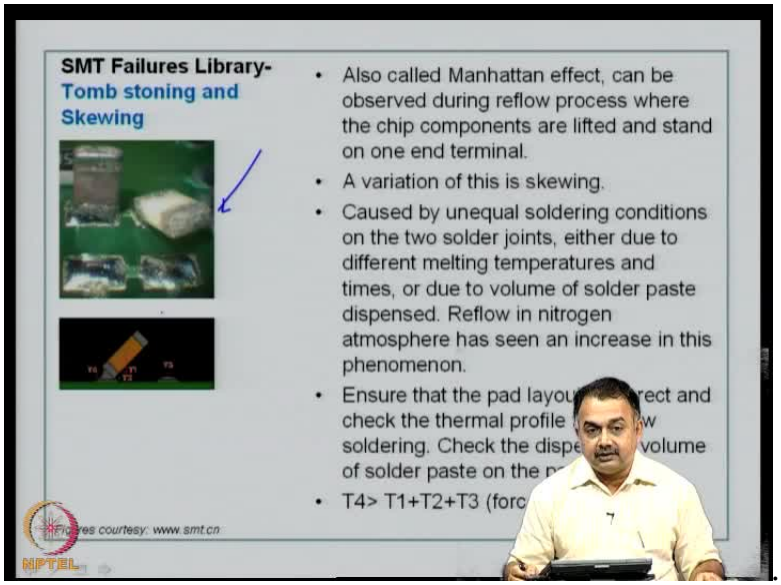

We have spent a lot of time on the various issues that the soldering process could be phased - in terms of the individual processes like pick and place or the application of the solder paste, whether it is by stencil syringe dispensing and so on. We listed the kind of failures that one can expect. I am trying to highlight or recap some two or three important failures that could be observed during SMT assembly; the first one is the tomb stoning or the skewing. We have seen an exhaustive list of the failures library in that particular module.

This is basically to highlight the light-weight of the components like your chip components that can have problems during reflow soldering, especially because the temperatures could be unequal at the different sides that you are seeing here in this picture of the chip component or the material not being pure in terms of the components and then the volume of the material that you have dispensed also could be unequal. The other important issue is the atmosphere in which the reflow soldering process has taken place either in air or in nitrogen atmosphere.

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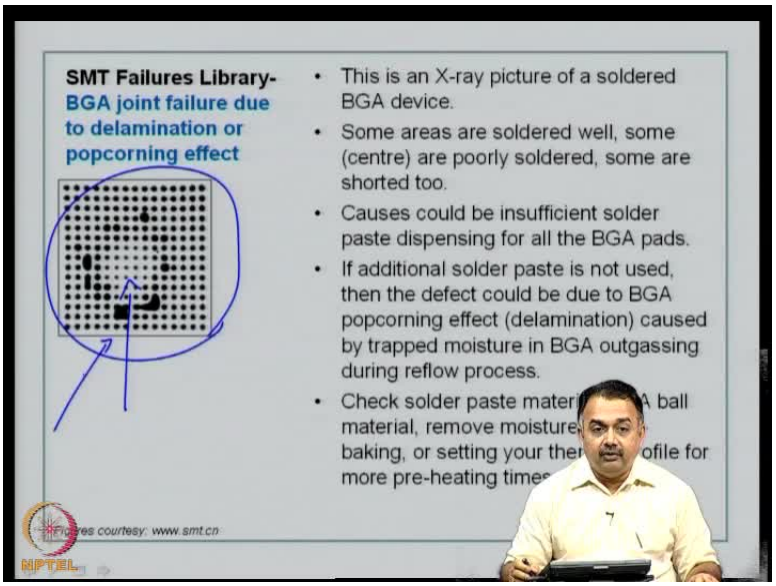

Because BGA is being used in a large numbers today, failures are bound to happen during assembly of BGAs. So, look for failures especially the popcorning effect or the delamination and also because the dies attachment of the BGA, the solder ball attachment cannot be viewed by the normal microscopes, you have to use X-Ray micrograph and see whether there is a die crack or a popcorning effect or simply important issues like unequal solder paste dispensing, creating in for example, the areas that you see here in the middle where you are not sure whether it is a wet joint or a reliability joint because of low solder paste volume that has been dispensed. Inspection of BGA during assembly becomes very important; look for these defects and qualify your BGA attachment process.

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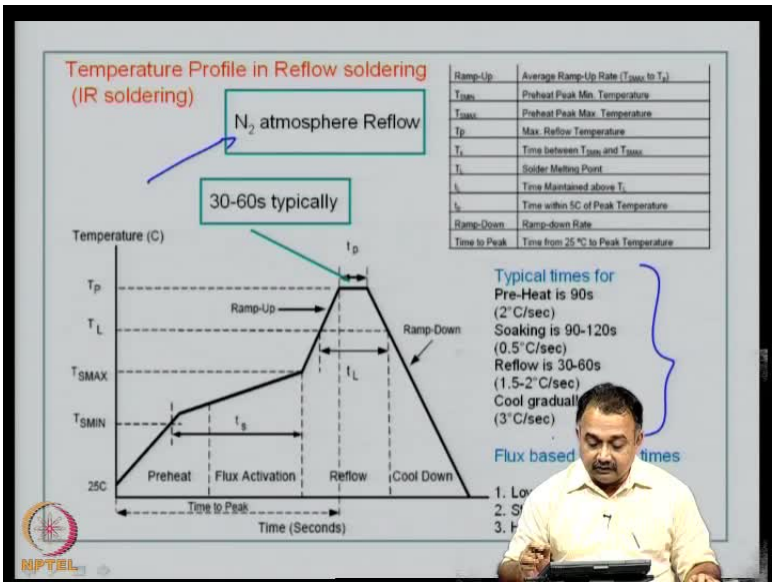

The soldering process is complex; we have seen the issues like temperature profile setting which is a major task, when you setup a reflow equipment for a particular batch of BGA assembly or surface mount assembly. So, you might use a different substrate for different batches. Look at the TG of the substrate. Look at the solder paste melting point and then set your thermal profile accordingly. Also, have an idea about what temperature you are going to work with. There are various zones as we have seen pre heat, soaking, reflow, and so on. Involve yourself for a large amount of time in setting the thermal profile correctly by doing a number of trial and error runs and then if it is a large volume manufacturing you have to maintain these standards and also the same setup materials for the entire product.

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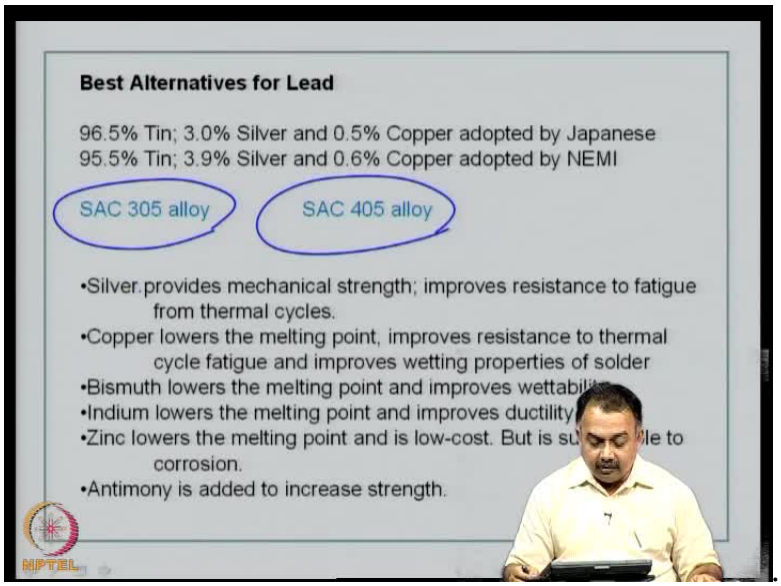

The alternatives for lead is very important; because lead is being phased out we are looking at lead-free electronics, tin is a problem because of viscous and therefore, alternatives for lead could be simply SAC 305 alloy, or SAC 405 alloy. Typically large percentage of tin is used with a small percentage of a silver and copper. The reason for adding silver we have seen, it provides a better mechanical strength, improves resistance to fatigue from thermal cycles, copper lowers the melting point, improves the resistance to thermal cycle fatigue, and improves the wetting properties. There are other materials also available.

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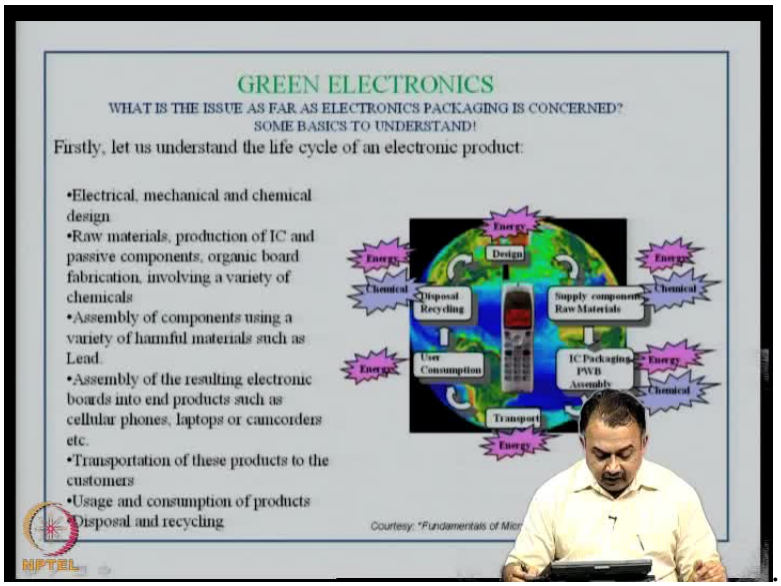

Major problem in the electronic industry today is green electronics. As designers and as fabricators, you have to get involved in contributing a bit to the green environment. Whether it is design or supply of components and raw materials, IC packaging, IC assembly board fabrication and so on.

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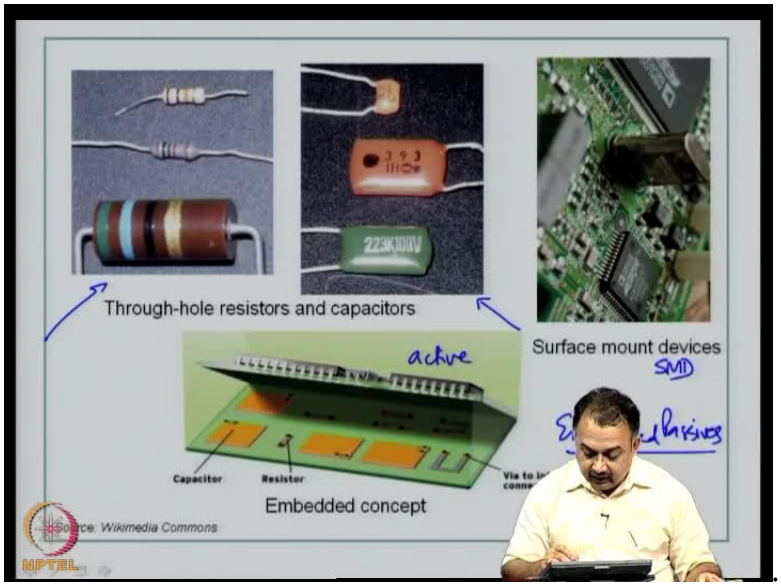

We have to look at the right usage of materials. Then the other development in packaging systems packaging, which I have highlighted towards the end of this course is the concept of embedded passives. We have seen what through-hole resisters are and

then what these capacitors are then we also seen what a surface mount device could mean in a re-engineering a product.

Surface mount device and through-hole component have different assembly technologies that needs to be considered in your design. Therefore, if you are using a hybrid mixture of through-hole and surface mount devices, look at your assembly process very carefully so that your board is not subjected to thermal shock unreasonably, because you are going to end up with reliability issues from the board side as well as the component side.

Now, to overcome these kind of issues, the embedded passives came in a big way and we have spent some time on looking at the fundamentals of embedded resisters, embedded capacitors, the basic equations that govern resistors, resistivity, heat resistivity, and the basic equation governing capacitances. If you look at this illustration here, what you are basically seeing is active devices on an organic substrate and then the inner layers are used for resisters and capacitors and then you have the microvias being used to typically connect various layers of a multilayer organic substrate.

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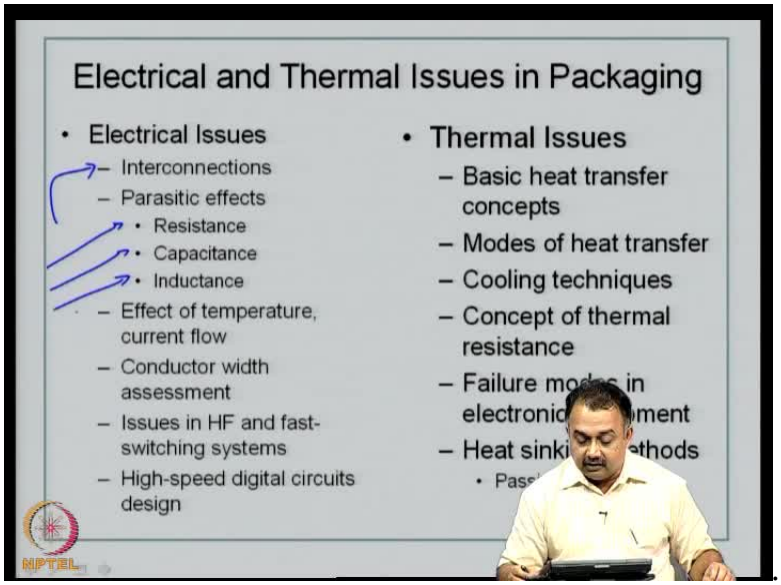

The electrical and thermal issues have been covered in this core sub packaging. What are the electrical issues that have been reviewed? We have looked at basic interconnections, copper interconnections in a Printed Wiring Board. We are not discussing interconnections at the chip level, the VLSI issues; we are looking at copper interconnections between components, between various devices on a system level

Printed Wiring Board. What are the issues considering the line width or the copper width that is being use for various segments; it could be a ground line, a signal line, a power supply line, therefore, what are the considerations as a designer you have to take care of the interconnections at design stage.

Once your schematic is ready, you are going to spend a lot of time on understanding or simulating the parasitic effects that could be there on your system level Printed Wiring Board like R, C and L and then the effect of temperature on the system, the current flow, conductor width assessment for a ground plane, a signal line, and so on. How do you calculate them? What are the basics for calculating, we have seen, and issues in high frequency and fast switching systems, high speed digital circuit design briefly.

Thermal issues, the basic key transfer concepts that is required for a very general understanding of any product. How is heat dissipated from the die to the external environment ambient, modes of heat transfer, conduction, convection, and radiation cooling techniques, concept of thermal resistance in a circuit, failure modes expected in an electronic equipment and heat sinking methods, whether it is a passive or a active methodology.

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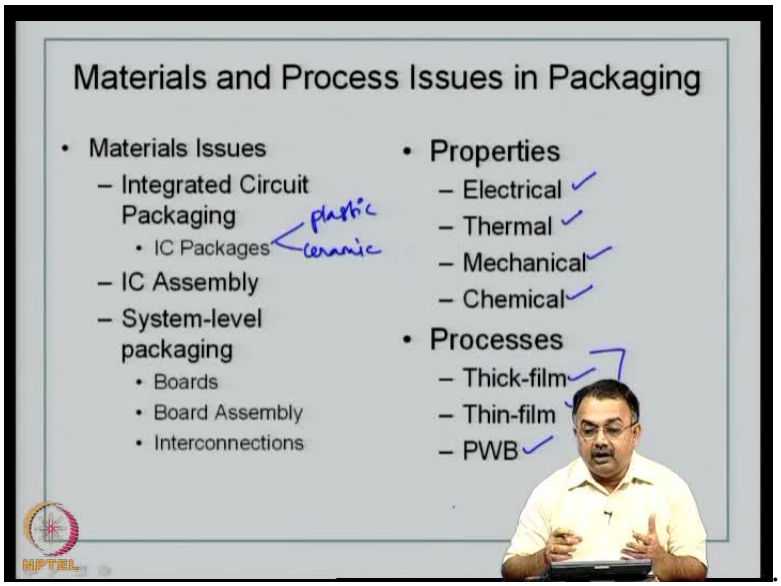

We have seen briefly, materials and process issues in packaging like the choice of materials in various segments starting from the IC packaging or the materials used in the IC package itself, whether it is a plastic package or a ceramic package, a host of

materials that are being practiced today and what are the end properties of these packages. Various materials used in I C assembly.

Then we talked about system level packaging that is the boards, board substrate. We talked about the interconnections using solder material, board assembly using lead-free material, and so on, properties of prime importance to a designer. What you should consider should be electrical issues, thermal issues, mechanical and chemical all are very important for a designer. Processes - thick film, thin film and PWB technologies need to be understood, if you want to consider different choices for different application areas. A very cost effective one would be your Printed Wiring Board, but if you are going to build systems, where cost is not of the prime concern, then you can look at alternatives like a thick film or a thin film process.

Thick film would be using some kind of a hybrid circuitry where you are going to embed conductors, resisters, capacitors, and so on; then co-fire them at different temperatures like LTCC process or a HTCC process.

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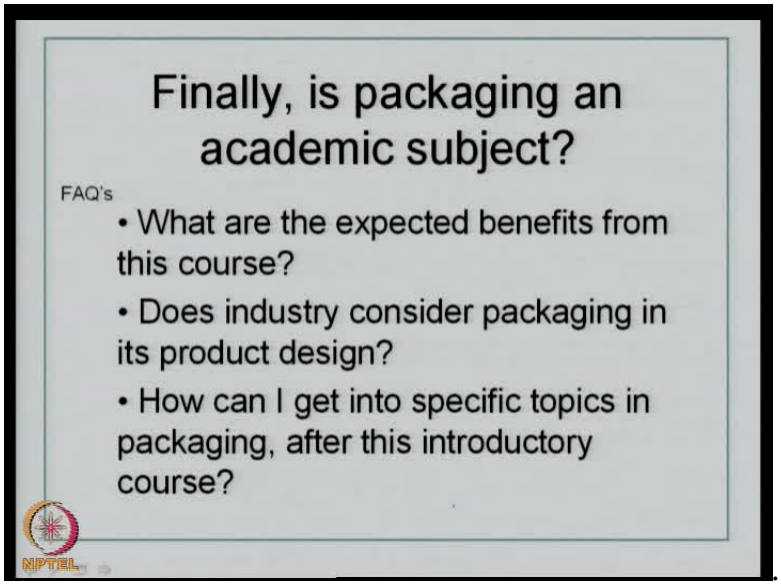

Finally, having seen all these topics, the time has come to ask this question - is packaging an academic subject? What are the levels at which packaging should be taught as an academic subject? Earlier it was believed that packaging is a component that is required to be learnt by the engineer in the industry and industry engineers were being trained in various aspects of packaging and that took a lot of time; but today it has been

realized that packaging needs to be taught to engineers at a very early stage, typically at the undergraduate level and that is one of the reasons why this course is being aimed for the undergraduate students in the in the country. Therefore, we are looking at universities to adopt electronic systems packaging for undergraduate students midway during their course; so that they can think about a career in electronic systems packaging. It could be electrical, thermal; it could be basic electrical design issues or manufacturing issues and so on once they finish their graduation.

The frequently asked questions are the questions that you might want to ask at this stage is - Is packaging an academic subject? Yes, the way the trend is, the way the requirement even at the university level where students design very complex systems; you are required to look at packaging and need to understand the various components in all the three levels of packaging. The benefits from this course - what is expected are that the undergraduate students as well as the graduate students would be sensitized to the various segments in this large multidisciplinary area of packaging. Once you get in to the industry, it will be very easy for you to adapt yourself to the industry in whatever field you are working with. The extension of this course could be either you can attend a workshop or a training specializing in certain specific topics in packaging and then once you enter the industry, you will definitely be involved in product design and there you can implement the packaging aspects very effectively.

The other question is - how do I get into specific topics in packaging after this introductory course? In the beginning, I have given you a lot of reference books that talk about system level packaging; there are lot of handbooks especially the system on package, handbooks that are being available in the libraries today. So, you can easily pickup your specific topic that you would need to and then explore the specific topic in detail.

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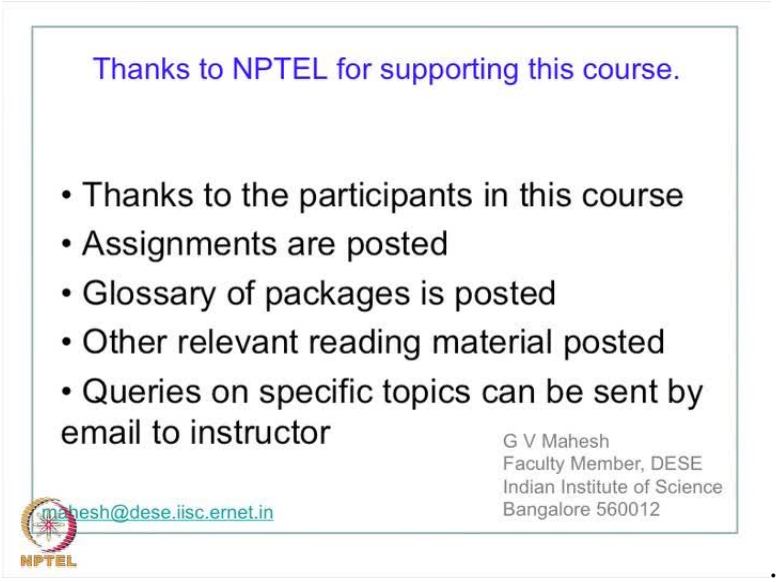

Finally, I would like to thank NPTEL, this national level course that supports education in a very large size, in terms of the number of people going through this web course. I would like to thank NPTEL for supporting this course for the undergraduate students and graduate students. I would like to thank the participants in this course who have gone through these entire lecture modules and gone through the various quizzes and the assignments and the questions that are given in this particular web course. So, for your benefit in this video course, you can go through various assignments that have been posted, specific to the various segments in this web course, and other relevant documents like glossary of packages, which is a very good companion of all the types of packages, the abbreviations and the acronyms are being listed. You can go through that.

Other relevant reading material like reference textbooks and so on are also listed which can be extended by you for increasing your understanding in this particular topic. If you have any enquiries on specific topics, it can be emailed to me at the email given here. I wish to thank all the participants once again and I would like to wish you all the best in your future endeavors. I hope you can apply packaging somewhere either in academics, research, or in the industry that you will be getting into. Thank you.