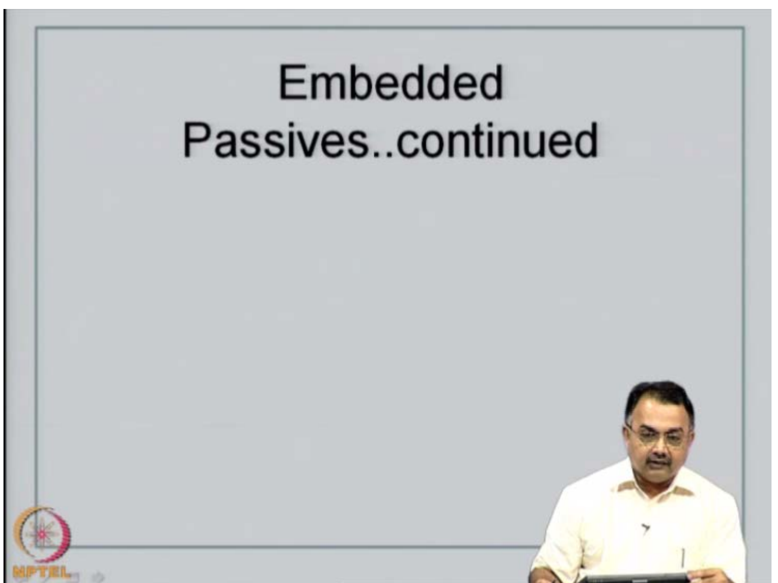
An Introduction to Electronics Systems Packaging

Prof. G. V. Mahesh
Department of Electronic Systems Engineering
Indian Institute of Science, Bangalore

Module No. # 09
Lecture No. # 41
Embedded capacitors
Processes for embedding capacitors
Case study examples
Summary of materials in packaging

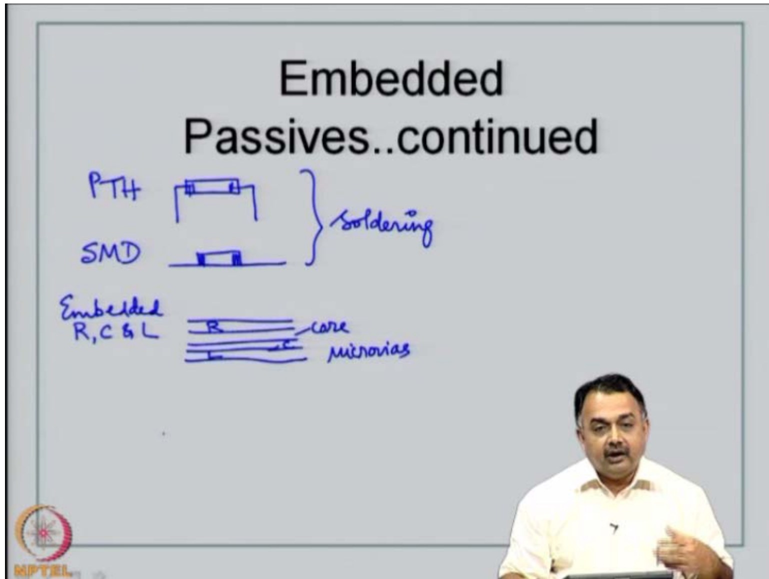
.

(Refer Slide Time: 00:44)



We will continue with this module on embedded passives technology. It is also known as embedded components technology. This is going to be a very important technology in the current few years from now on, because this is a growing technology and there are still many groups that are working with embedded passives. As far as industry is concerned, as I mentioned in the last lecture, people are still working with new designs on how to create embedded passives; that is embedded resistors, embedded capacitors and embedded inductors into their design.

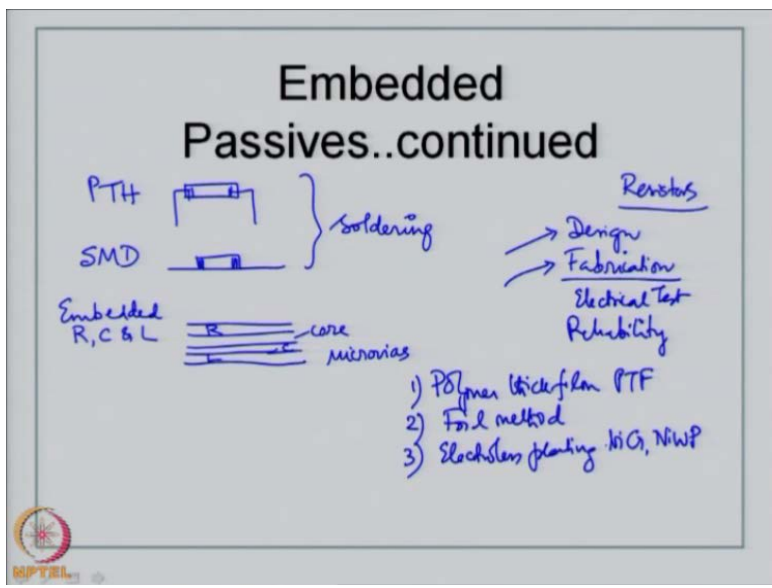
(Reference Slide Time: 00:44)



Ultimately, the fruit of these exercises is to get a Printed Wiring Board. A system level Printed Wiring Board - that is highly miniaturized - has got a very high density in terms of components. At the same time, we are also looking at how well the electrical performance and thermal management issues are being taken care of, when we use or employ embedded passives.

What I will do right now is take you into a quick recap of what we have seen in the last class, in this embedded passive components technology. All of you were and are familiar with plated through-hole components; that is, you have resistors that have leads and these can get into a system level Printed Wiring Board. Then we talked about surface mount devices. Typically, if you have the surface of the board here, then you will have these passive devices mounted on the surface of the board. The soldering methodologies for plated through-hole component and surface mount devices are different. We have seen that. So, the issue is soldering problems and reliability issues associated with each of these technologies.

(Reference Slide Time: 00:44)



Now we are talking about embedded components; that is R C and L, which means if you have a system level Printed Wiring Board and then if you have a core of the Printed Wiring Board designated, you can embed R into one of the layers and C and L respectively and connect them to the copper interconnects through microvias. So, the key to this technology is what kind of geometries or feature sizes you can work with in embedded resistors capacitors and inductors. How they can improve in the production or fabrication of high density, high performance system level Printed Wiring Boards?

Then we talked about resistors - embedded resistors - and we have seen the key issues for working with embedded resistors; that is, the design is a major issue. Then we talked about fabrication issues then the other points that are of due importance for resistors are the electrical test and reliability issues. So, in terms of resistors and capacitors, we are going to see embedded capacitors in a bit from now.

What we have seen in the last lecture is the design library for resistors, how the resistors patterns are generated, how you can create them and maintain your own library in your CAD system. As I mentioned in the last class that there are no set standards as far as the library modules in the CAD system for resistors and capacitors embedded.

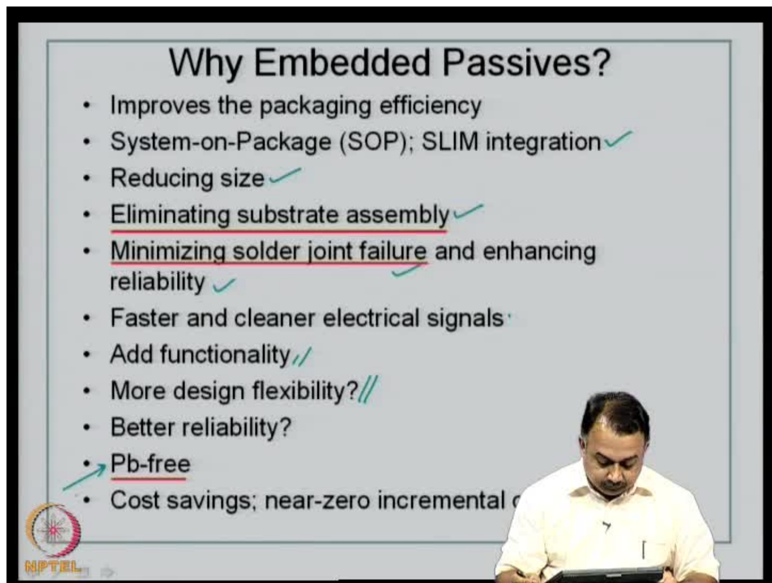
So, you as a designer need to know how well you can exploit your design knowledge into integrating these devices to fabrication of these devices into the system level Printed Wiring Board compatible format. So that is what we saw in the last class, the different methods of fabrication of resistors. As you can recollect, you can fabricate resistors by

polymer thick film or PTF as you can call it, then the second one is the foil method, how you can laminate resistor foils with the Printed Wiring Board dielectric material and finally, electro less platting as a key methodology to plate resistor materials like nichrome or nickel tungsten phosphorous and so on. We have also seen the materials used in each of these methods to create embedded passives.

Now the other important issue is that if you use embedded resistors, you are able to integrate into a system and package format, which is the current technology today to miniaturize system level Printed Wiring Boards. We also talked about system level integrated module based on organic substrates. I do not have to emphasis here that organic substrates are very cost effective and you have to always look at building embedded passives in an organic substrate.

Now if you recall, I also talked about hybrid circuits in the last class, where hybrid technology has been known much earlier and especially the thick films circuits talked about screen printing thick films of resistors, copper conductive paste or capacitors or inductors and then co-firing them using LTCC process or HTCC process and then realizing modules including multichip modules.

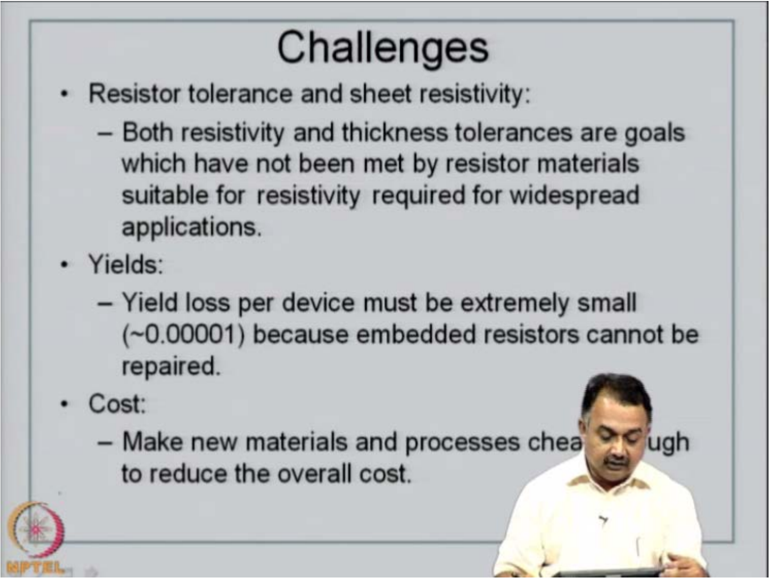
(Refer Slide Time: 08:00)



So with this background, we will continue with today's class. I will just borrow this slide once again from the previous lecture to highlight again the importance of embedded passives and to help you recollect. The highlight is, it improves the packaging efficiency.

There is no doubt about it, provided you provide a high-end design that is manufactureable; that is testable; and that is reliable. Just now I talked about SOPs, SLIM integration, then we have to aim at reducing the size of the components, it eliminates the substrate assembly all together. So, if you have for example, 100 percent embedded passives or 95 percent embedded passives in your design, you can do away with most of the soldering or joining methods and thereby reducing the risk of failure arising out of solder joints.

(Refer Slide Time: 08:00)

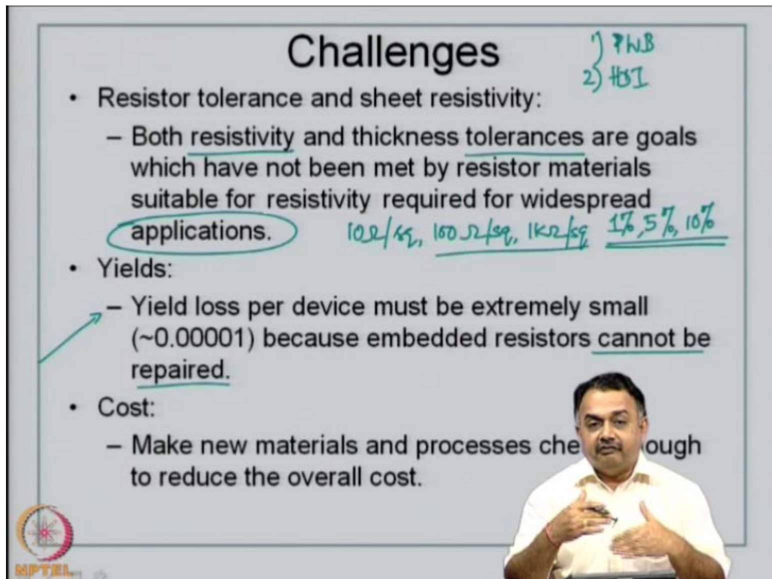


Minimizing solder joints failure and enhancing reliability and then in terms of electrical performance, it can be faster and cleaner, adding functionality to the board and then more design flexibility in terms of tolerances and values, although on the negative part of why we need not go into embedded passives is that more and more surface mount devices are available in lower profiles or formats and the important key issue is it is lead-free. Now the challenges that we face with the embedded resistor process.

Firstly, you must understand the PWB process technology to work with embedded resistors because invariably you have to work with organic build up. Basically first is, as a designer please understand what a PWB process sequences are and in terms of the high density interconnect technologies, what are the buildup technology that can be used and to enhance performance what are various dielectrics that are being used in the buildup of

the high density inter connect because you can take advantage of nicely integrating the resistor process with these technologies.

(Refer Slide Time: 08:00)



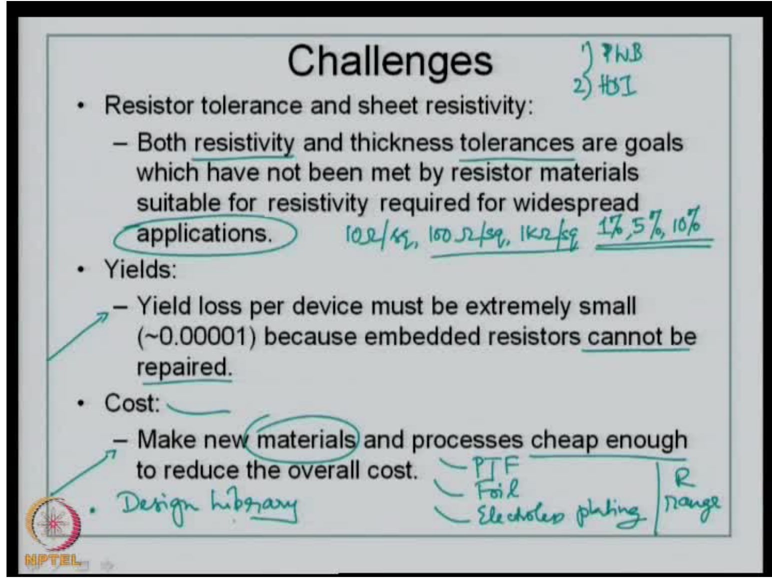
So the challenge firstly is how can you maintain the resistor tolerance as compared to devices that are available in the market today with specific values and specific tolerances that are mentioned? When we say tolerances in terms of resistances, can you fabricate a material with 1 percent tolerance or 5 percent tolerance or 10 percent tolerance that is acceptable in your product is the key question before a designer and this has to be translated into discussions with the manufacturer who can manufacture embedded resistors.

So both resistivity when we say resistivity, it is the sheet resistivity, so typically what kind of material that you are going to use, is it going to be 10 ohms per square or 100 ohms per square or is it 1 k ohms per square or are you going to use a set of different materials for different layers to achieve a range of resistances that are required for your design.

In terms of challenge currently as far as embedded resistors are concerned, these two are very important, sheet resistivity in terms of choosing the right material and the process. Can you get a specific set of resistor values using polymer thick film? Can you get it by electroless plating? These are issues that need to be discussed with the manufacturer and

the goals which have not been met by resistor materials suitable for resistivity required for widespread applications.

(Refer Slide Time: 08:00)

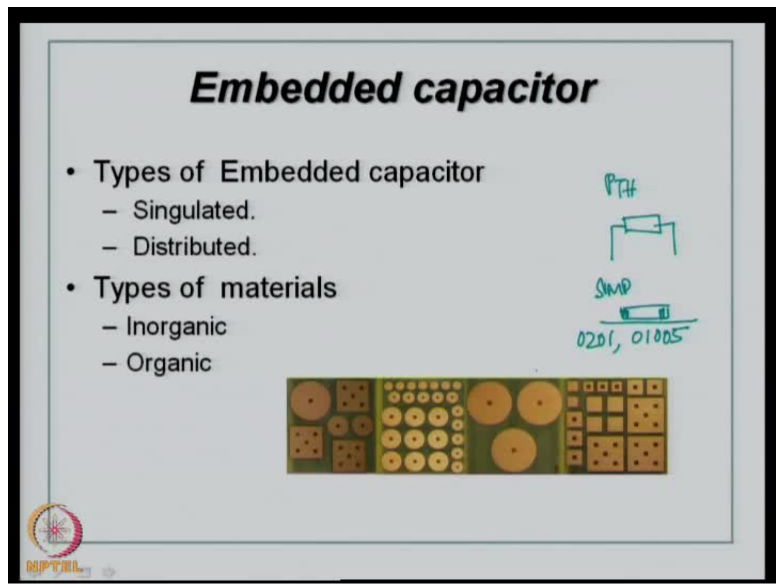


So, basically you have to look at applications and then accordingly decide on your design. As far as the manufacturing aspects are concerned, yield is a major issue. When you work with surface mount devices or plated through-hole components, you should be prepared to replace and repair these devices if they end of with failures. But here repairing is going to be very difficult; because embedded resistors in some sense cannot be repaired at all, if the inner layers containing the resistors are built and sequentially laminated with your signal layers. So, yield loss per device must be extremely small because the repairing part of it is very remote in the case of embedded resistors. Cost wise, cost is an issue that is influenced by the kind of materials that you use in embedded resistors. So the process should be cost effective, cheap enough to reduce the overall cost.

Are you going to look at a more cost effective polymer thick film process or is it going to be a foil method which could be slightly expensive compared to a polymer thick film process or more precise in terms of thickness, electroless plating. So, it depends on the material that depends on the resistor range that you are going to work with and how we can employ these methodologies suitable for a particular customer in terms of whether it is a medium dense board, high dense board and so on.

So remember three challenges still exist today for embedded resistors: one is the resistor tolerance and sheet resistivity interrelated, yield issues as far as production is concerned, cost effectiveness. Finally, I would like to add here one more important point, which is your understanding of the design library. How effectively you can build a design library, understanding your knowledge with process issues translated back to creating geometries that could effectively be used for feature designs.

(Refer Slide Time: 15:35)

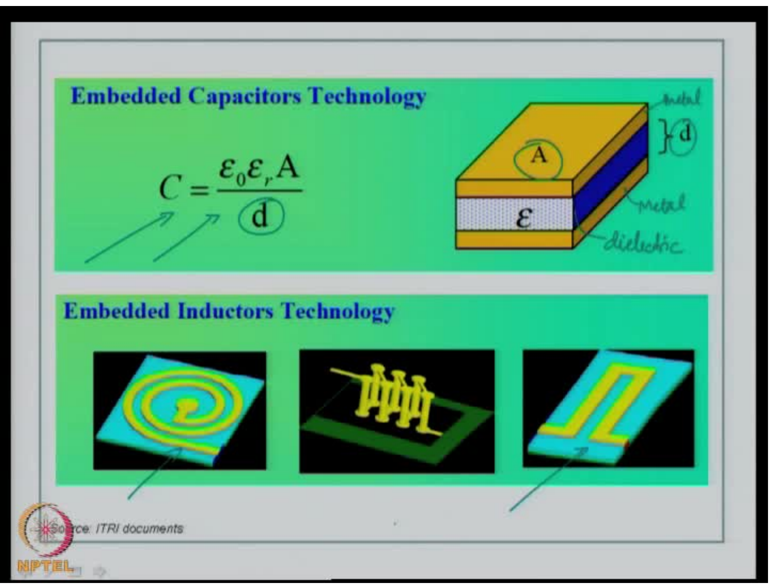


Now we will move into the next topic in embedded passive components - that is embedded capacitors. What are the types of embedded capacitors that can be designed, fabricated and tested? The first one is singulated capacitors; the second one is distributed capacitors. What are the types of materials that could be used? Inorganic materials and organic materials. Now unlike resistors, capacitors need to be understood in a much better fashion because the applications are varied, the requirements are also varied, and you have also a host of materials that you can employ to realize capacitors.

As you know in the plated through-hole capacitors, the materials are fabricated by thick film technology and same is the case with SMD capacitors. So, they are actually co-fired and trimmed to their required tolerances that you require and then the good part of using these devices are that today you have equipments that can handle miniaturized surface mount capacitors.

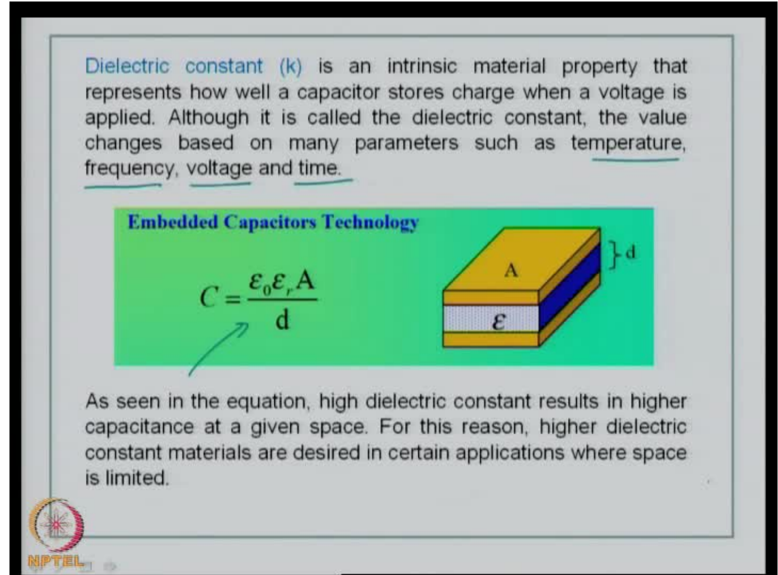
How we do go about working with embedded capacitors when there is already a challenge in terms of availability of low formats or small formats of SMD devices especially 01005 or 0201, already a well-known standard?

(Refer Slide Time: 17:33)



Now let us have a look at some of the basis for designing embedded capacitors and inductors. We will not deal with too much of inductors in this particular lecture; rather I will focus more on capacitors. But the technology of creating each of these is very similar so that is the reason why I brought this illustration here, in this particulars slide. The embedded capacitor technology is based typically on the well-known equation; all of you are aware of this, capacitance is related to the dielectric constant of the material and the area of the capacitor material and then the thickness. Typically you have a sandwiched structure like this where you have the metal plate, then here again you have a metal plate then in between you have the dielectric material of specific dielectric constant, so d is the thickness of this, is a key component in deciding the capacitance and then you have also the area of the material. So area of the conductor material, the thickness of the dielectric and the volume of the material used as the capacitors material and the sandwiched structure and based on this equation, you can play around with creating different geometries that can provide different values of capacitances.

(Refer Slide Time: 20:03)



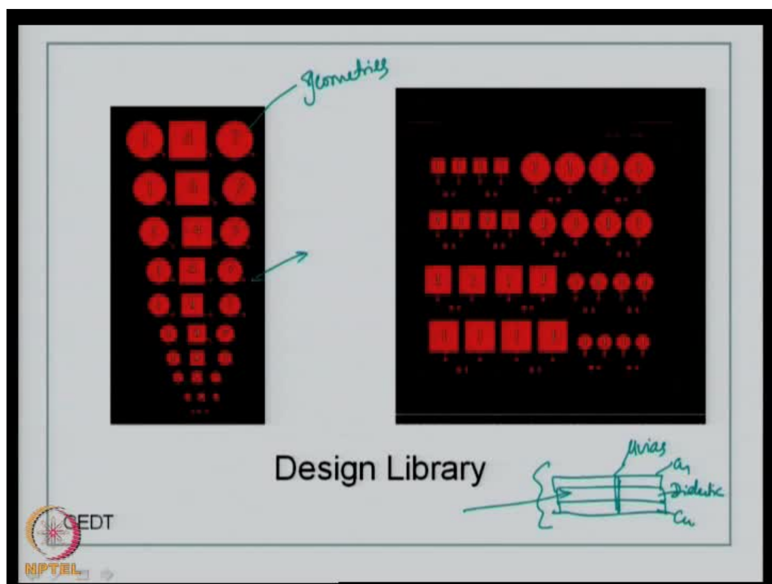
Similarly, inductors can be created on Printed Wiring Board substrates. Typically you can create different geometries spiral and so on, bar type or miaering types of inductors. These can be simply created by a printed etch method of the design that you require. So, embedded resistors, capacitors and inductors can be judiciously employed in your PWB design itself.

So, we will slightly dig deep into the factors deciding the values of the capacitors. Dielectric constant is very important. It is an intrinsic material property that represents how well a capacitor stores charge when a voltage is applied along the area of the material. Although it is called the dielectric constant, the value changes based on many parameters such as temperature, the frequency of operation, voltage applied, and time of interaction.

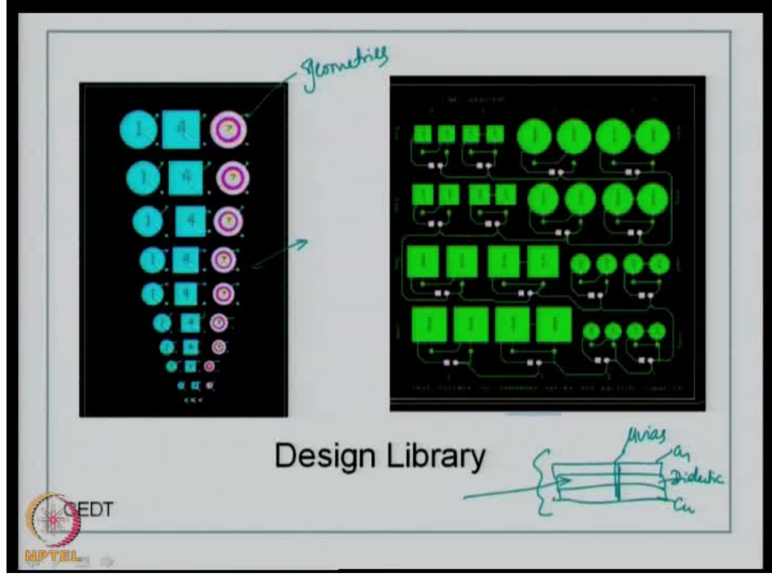
As seen in this equation above, the dielectric constant, high dielectric constant results in higher capacitances. So, if you want to have for example, using a sequential build up technology and employ different embedded capacitor in the buildup one above the core and one below the core, you can very judiciously use different capacitor materials to get different ranges or values, one of the top and one of the bottom interconnected and these capacitors can be interconnected to the signal layers, the ground plains and to the core by microvias

That is the advantage of using embedded technology. So for this reason, higher dielectric constant materials are decided in certain applications where space is limited. So, the use of embedded capacitors will be highlighted, if you can work with smaller geometry and reduce the size overall or the profile of these capacitors and area of these capacitors can be reduced in the entire build up to such an extent where it will be high performance, high dielectric constant materials being used in these cases.

(Refer Slide Time: 22:07)

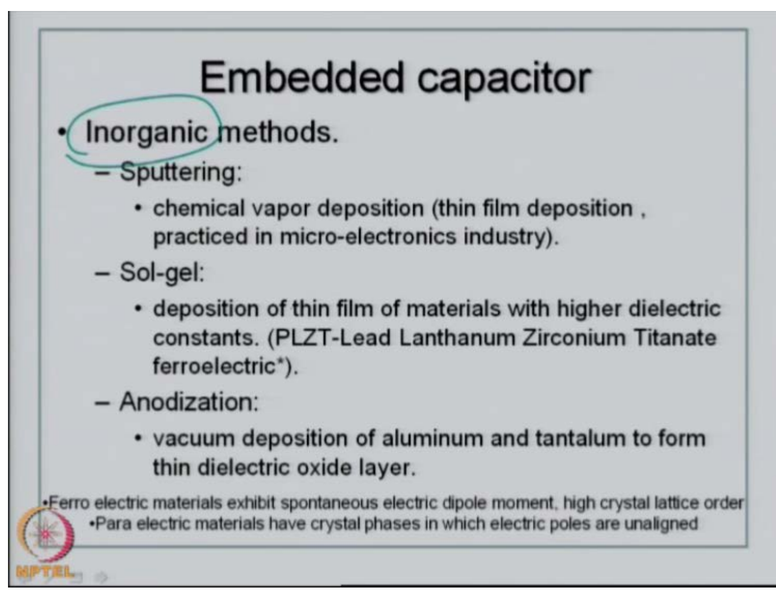


(Refer Slide Time: 23:30)



Now the other issue what I am showing up is, how you can build a design library similar to the resistors that we talked about. We talked about how resistor library can be built by using bar type resistors or miaering ring type resistor shapes in geometries. Here in the case of capacitors, what we have demonstrated here is basically to show you a set of geometries that could be utilized in creating capacitors.

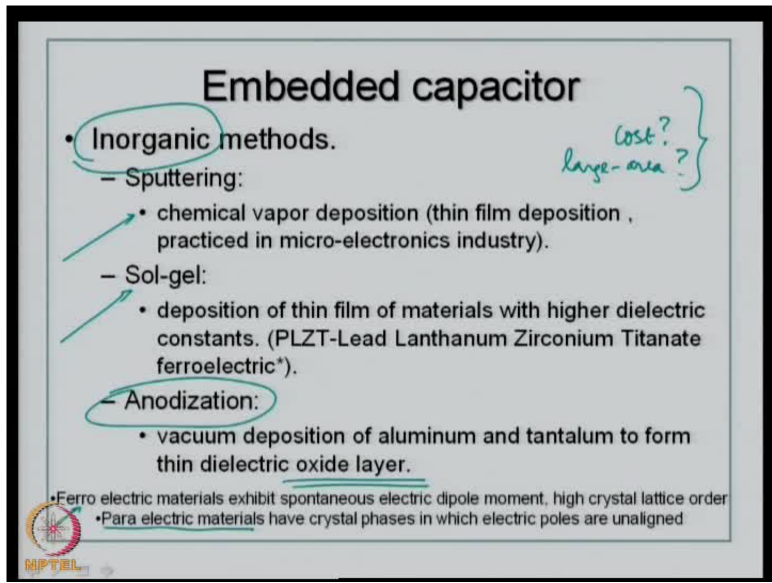
(Reference Slide Time: 25:22)



We have a circular geometry square and you can also see there is a microvia interconnect that could be seen here. Basically you are looking at metal layer and then a sandwiched material which is the dielectric that we are talking about and again the other copper layer. So, this kind of structures can be created on your Printed Wiring Board. Choose that right appropriate dielectric constant for this thickness of dielectric that you intend and then you can inter connect them using microvias. As you can see, this is the top layer of the design, if I can go back and you see this is the bottom plate m then in the build up you have dielectric material overlapping these particular structures and then you will have a foil or added copper to the dielectric material and these will be interconnected through microvias for testing.

So these geometries will behave as a capacitor. Now, the area is very important and then the value of the dielectric constant in terms of the material used is also important. This is the test port that you are seeing here demonstrating series and parallel capacitances for various geometries and then these kind of geometries can be explored for your design.

(Refer Slide Time: 25:22)



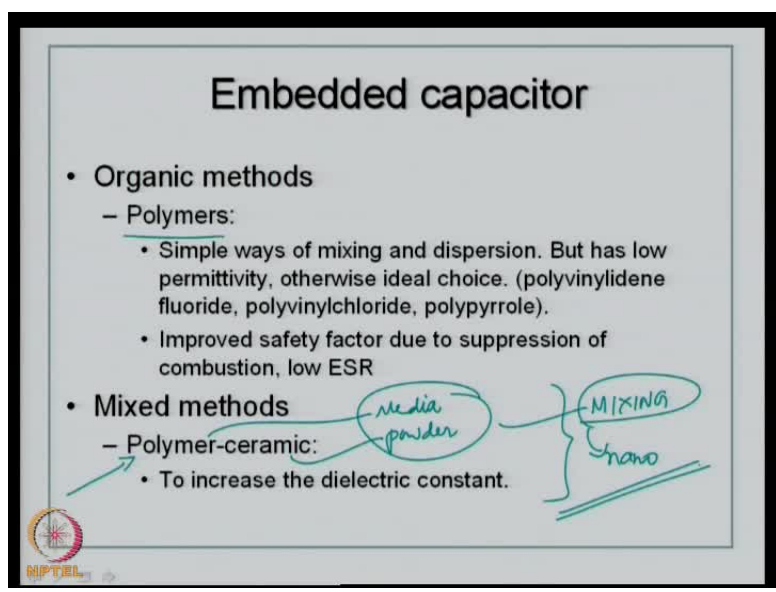
Now briefly we look at the process details for embedded capacitors. I am not going to spend too much time on how such designs can be created. Just as we talked about in resistors, it is up to the designer to play around with the knowledge of the material available in the process and then decide on the geometry that you require. So, the key here is take away from the previous slide is that decide on geometries that can best fit with lower area occupied in the Printed Wiring Board. But it should be possible to produce high capacitances with high dielectric constant materials.

Firstly in terms of process, we could have inorganic methods typically sputtering using chemical vapor deposition, thin film deposition practiced in microelectronics industry. It could be easily adopted into the fabrication methodology. Ideally these are suited for small areas; not really suited for large area fabrication that you would see in the Printed Wiring Board arena.

Then the second one is, the Sol-gel method where you can deposit thin film of high dielectric constant material using Sol-gel methodology that is well known in the materials field. There are different materials that could be used. It could be for example, lead, lanthanum, zirconium, titanate, ferroelectric material. Today in this field, we have seen the use of ferroelectric materials and para-electric materials that exhibit different properties based on the crystal structure.

Then, the other method is anodization that is very typical of aluminum; vacuum deposition of aluminum and tantalum to form thin dielectric oxide layers that can produce capacitance values based on your requirement. So, these are the inorganic methods again very good for prototyping, very good for small area products. But the one important thing that we have talked about is this really suited for large area manufacturing? Cost is an issue, so large area and cost are definitely issues that might weigh down against inorganic methods.

(Refer Slide Time: 25:22)



The other one that is kind of more familiar with many of the manufacturing industry is that use of polymers and the use of polymer ceramic method technologies. For example, if I can focus on the polymer ceramic method which is known as the mixed method, you take a polymer as a media and then take these ceramic powders with specific dielectric constants and then you can mix them together to get a very good homogeneous mixture and these can be applied by let us say spin coating. Typically more in favor spin coating other coating methodologies to an organic substrate that contains the bottom plate typically copper of a Printed Wiring Board and then on this polymer ceramic cured material, you can either laminate a foil, a capacitor foil or you can deposit copper by electroless plating followed by electro plating methodologies.

So this looks like very familiar and high possibility of integrating with the Printed Wiring Board technology. Now we will talk about using organic polymers. The

advantage of this method is, simple ways of mixing and dispersing the material but has low permittivity, otherwise it an ideal choice like polyvinylidene fluoride, PVC, polypyrroles etcetera, improved safety factory due to suppression of combustion and low equivalent series resistances values.

So using polymers could be a solution in terms of large area manufacturing, but if you want to synthesize your own capacitor, the polymer ceramic method is highly advantageous method because you know the dielectric constant of the polymer material that you are using and then you can also formulate ceramic powders based on the dielectric constant and then your design that requires these values and then the key issue is the mixing to get homogeneous mixture, a good dispersion of the ceramic powders. You could also use nano materials to make it as nano composite formulations synthesis and then this could establish very high capacitance values for high performance Printed Wiring Boards.

(Refer Slide Time: 30:21)

Material	Dielectric constant	Dissipation factor (%)	TCC (ppm/°C)
Teflon	2.0	0.02	-100
BCB	2.7	0.1	N/A
Polycarbonate	3.1	0.1	N/A
SiO_2	3.7	0.03	<100
Epoxies	3 – 6	0.4 – 0.7	N/A
SiO	5.1	0.01	~200
Al_2O_3	9	0.4 – 1	390
Ta_2O_5 (amorohous)	24	0.2 – 1	200
$BaTiO_3$ (tetragonal)	~1000	5	Highly variable

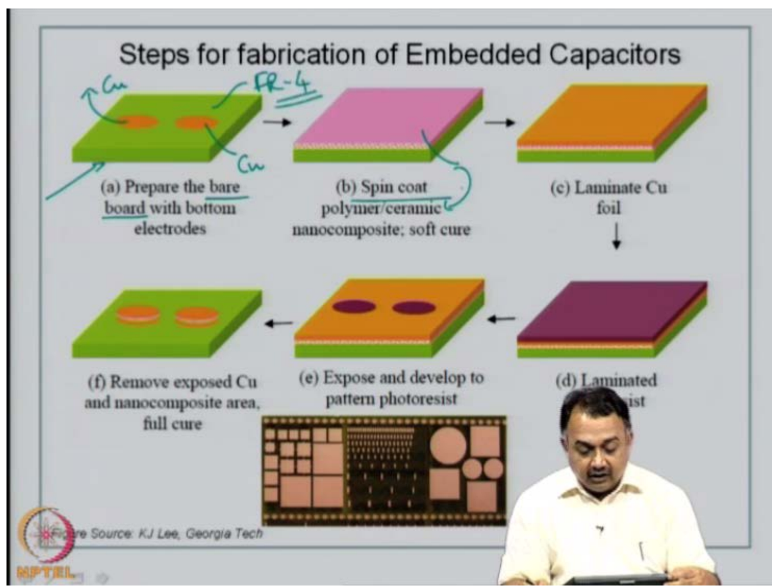
- A wide range of capacitance from 1pF to many uF is needed for various applications.
- For filtering and termination relatively low capacitance of 1pF to 200pF is required.
- For decoupling and energy storage the range is a few nF to a few uF.

Now what I have given here is a list of materials in terms of substrates and the capacitors materials that could be used in this industry. The issues here are dielectric constant, important factor dissipation factor, and TCC temperature coefficient of capacitance. Teflon, you can see the values of dielectric constant benzocyclo butane 2.7, polycarbonates silica epoxies well known in the PCB industry and then we have this alumina powder, tantalum oxide, barium titanate much used in the capacitor industry.

There could be a other composite materials or inclusions in barium titanate like trancium could be added so barium trancium titanate so that you can synthesize or varied properties by adding new elements.

So, the wide range of capacitances from 1 pica farad to many micro farads is needed for various applications. You have to dig into various substrate materials and the binding material as well as the oxides that you are required to the filler material that yare required to vary the property to suit your applications. Now filtering and termination capacitors typically require low capacitance of one pica farad to 200 pica farad. So, accordingly you can synthesize. Then for decoupling and energy storage, the range of capacitances varies from a few nano farad. So with trial and error, you can in fact vary the properties by varying material usage.

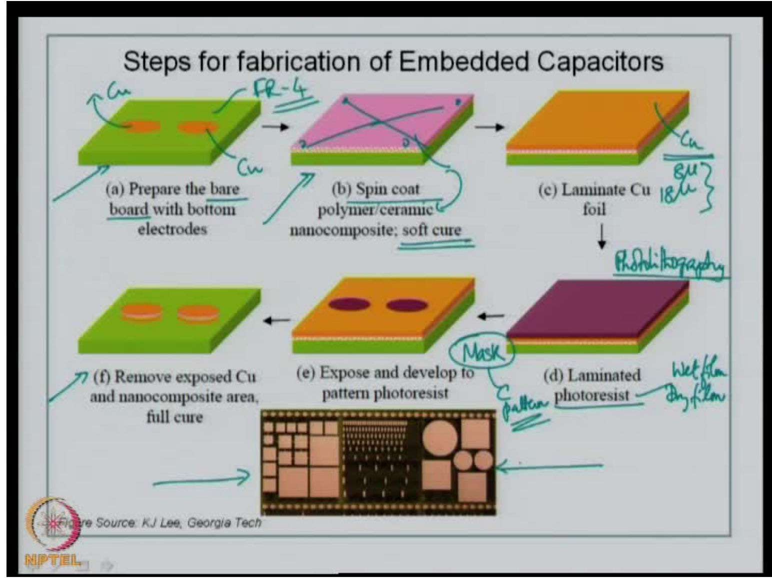
(Refer Slide Time: 33:28)



I will step into illustration of embedded capacitors that could be prototyped and this could also be useful in large area. Take a bare board, this is a typical Printed Wiring Board with the bottom electrodes. This is the copper and this typically could be your FR4 material glass epoxy composite material. Now you can typically do a subtractive process to get these patterns. This is the bottom plate copper and typically you can do printed etch method by using photolithography, then do a spin coating of the polymer ceramic nano composite material you can see here in pink shade, this is the polymer

ceramic material you could also use nano powders . The key here is the right choice in terms of volume of the binding media and then the ceramic powders.

(Reference Slide Time: 33:28)



So there should be good flow. It should be easily used in methods like spin coating and I want to emphasis here that spin coating for areas like 12 inches by 12 inches seen very ideal and you can get a very uniform thickness. So, thickness of this stage is very important. If you talk about different areas on the board, you would like to have equal thicknesses on the board.

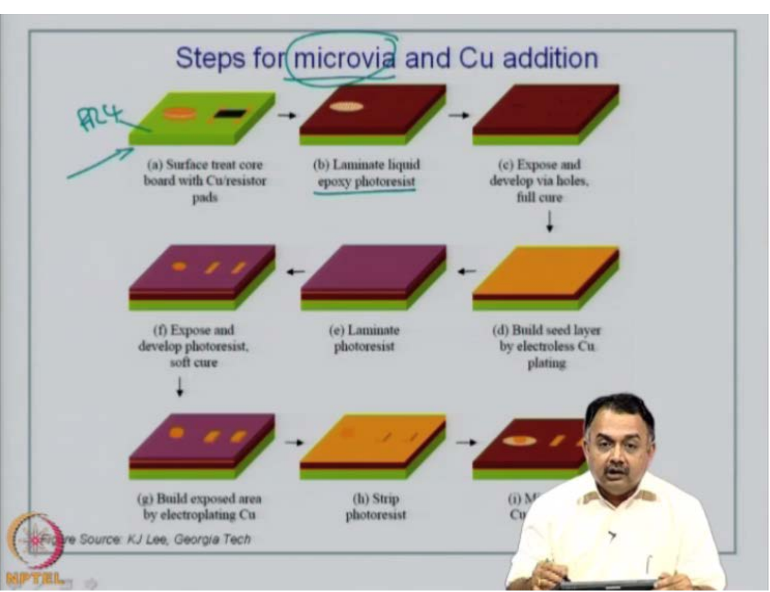
Typically, by setting the properties of the spin coating equipment, you can get very even thicknesses across the board. Then you can laminate a copper foil, after this, this is soft cured. You cannot do a full cure because you need to laminate a copper foil, so you can work with temperatures and pressures that are suitable for this kind of a system and then use a copper foil. The thickness again is determined based on your design. It could be 8 microns or 18 microns depending upon your design requirement and it also depends on the thickness that you have taken for the bottom plate of copper.

It is now processed. You have to realize a design like this that you see in picture f, so for that you go ahead with photolithography which you are now familiar with in the PCB process. So you can see that this process is a highly integrated with PWB process. You can laminate a photoresist, you can use typically a wet film or a dry film photoresist

material and then this now goes for exposure to UV light using a mask. So, let me write here that, suitable mask is very important. The mask defines the capacitor pattern.

Now using a right mask, you expose and develop to pattern the photoresist using a suitable developer and then once you remove the photoresist after the allied processes in between, you will now get a sandwiched pattern of the two metal plates with the capacitor material in between. So, what you have seen here in the picture is typical as a result of this process of using PWB methodology, photolithography using FR4 substrate and a simple mask containing the capacitor patterns used for patterning your top and bottom plates of the capacitors.

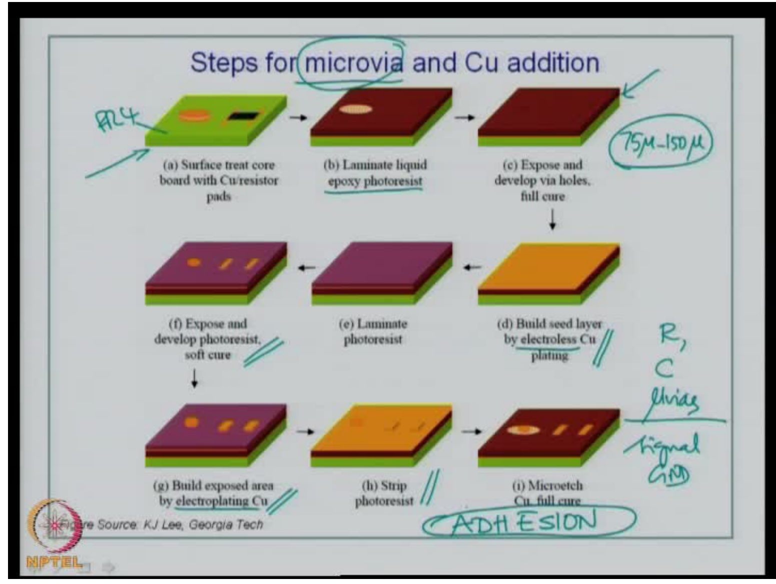
(Refer Slide Time: 37:58)



Now let me recap when you build these kinds of structures definitely you require to test them. You require to test these capacitors before it is actually sent to the next process stage. So, even in your design, you would like to connect your capacitors to other layers as I said before and for that you require to generate microvias.

So let us see how you integrate microvia process with the capacitor process. You can see here that this particular slide here shows the capacitor material and a resistor material that as been generated and formed on an FR4 substrate then apply liquid epoxy photoresist right and then expose and develop the via holes and fully curing.

(Reference Slide Time: 40:34)



Now you have to interconnect these via holes or make it conductive by means of first electroless copper plating then laminating again the photoresist exposing and developing the photoresist and with a soft cure process. Then finally, you can build the thickness of copper by using electro plating copper. Then the strip of the required photoresist that not required of this stage because all the patterning is complete. Now you micro etch. Remove the unwanted copper and then fully cure the board. This will result in the microvia connection for subsequent layers. So, you can highly integrate this particular embedded resistor and capacitor process with the SBU technology that I talked about in one of the earlier module that is the PWB technology module.

So anywhere on the board, you can design R you can design C you can create microvias and you can connect them to signal plains or your ground plains and your active devices. So we are talking here about the microvias of the order of 75 microns to 150 microns. These structures are very essential and you need to have very good resist material that can be used. For example, this step is very crucial to create microvia structures followed by a very crucial step of electroless plating and then the buildup thickness by electro plating process.

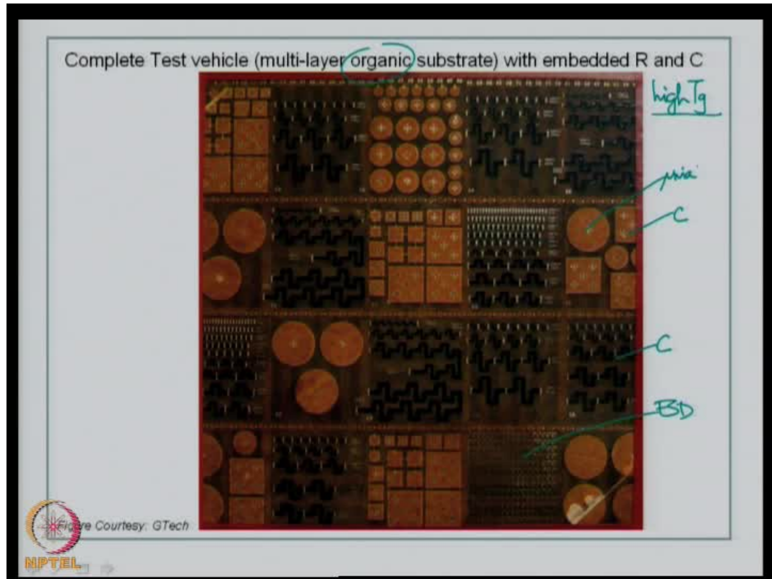
Now in the entire process the previous process of fabrication and this particular step I would like to mention a very key issue. The issue is adhesion. Adhesion of the dielectric material with the copper is a key issue in terms of reliability. So, at every stage whether it is embedded resistor formation or capacitor formation, please have a look at the peel strength issues that always is related to reliability between dielectric material and the

copper. So, adhesion is also very key in terms of microvia reliability because if there is a change in property during thermal cycling of the dielectric material, if there is a shrinkage of the material then the entire structure microvia structure will cave in resulting in failure.

(Refer Slide Time: 40:56)

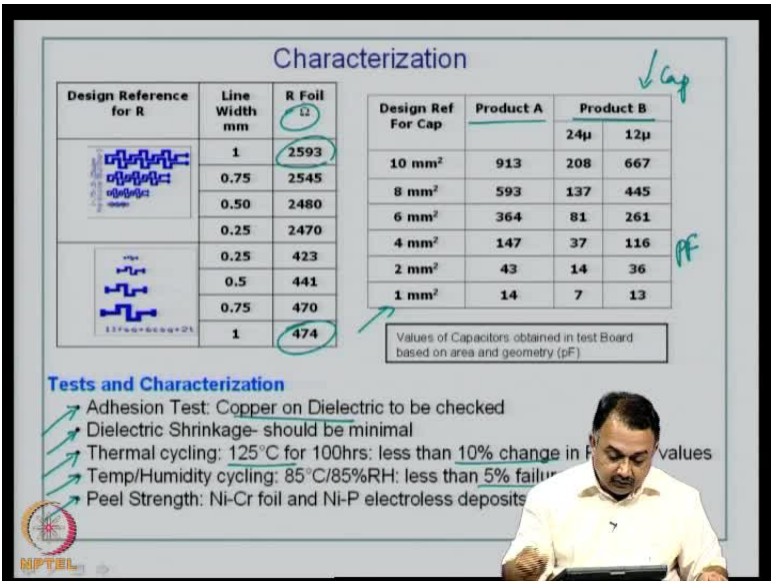
This is a picture of embedded capacitors that have been successfully fabricated in CEDT using various geometries using FR4 as a substrate and you can see the test points for this particular test board and the microvia. You can also generate initially plated through-hole interconnects for testing.

(Refer Slide Time: 41:22)



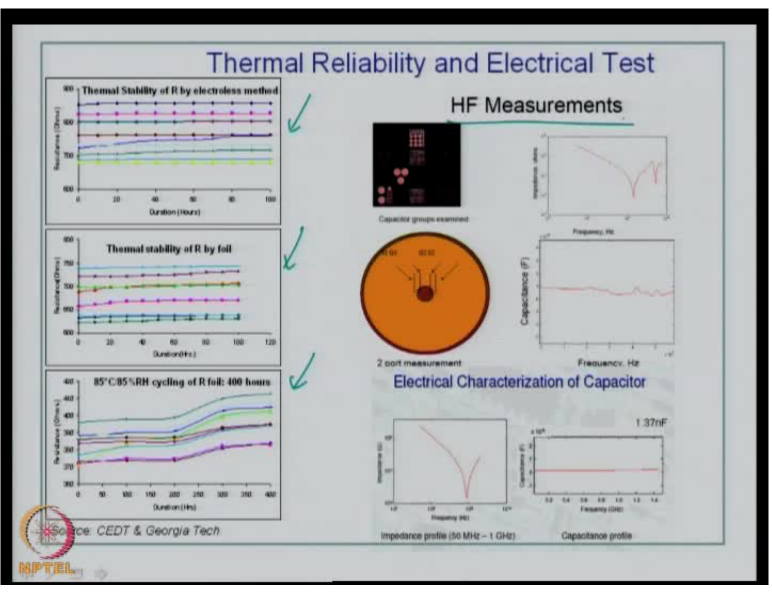
Now this is a complete test vehicle picture that you are seeing on organic substrate. The key here is a organic substrate. Ttypically you want use high Tg organic substrate with embedded R and C. You can see these are all capacitors, you can see resistors by polymer thick film method and this is the pattern for ESD electrical static discharge testing and you can also have a look at the microvia structures here in the capacitor you can see the microvia structure suitable for testing your capacitors and interconnecting them.

(Refer Slide Time: 42:06)



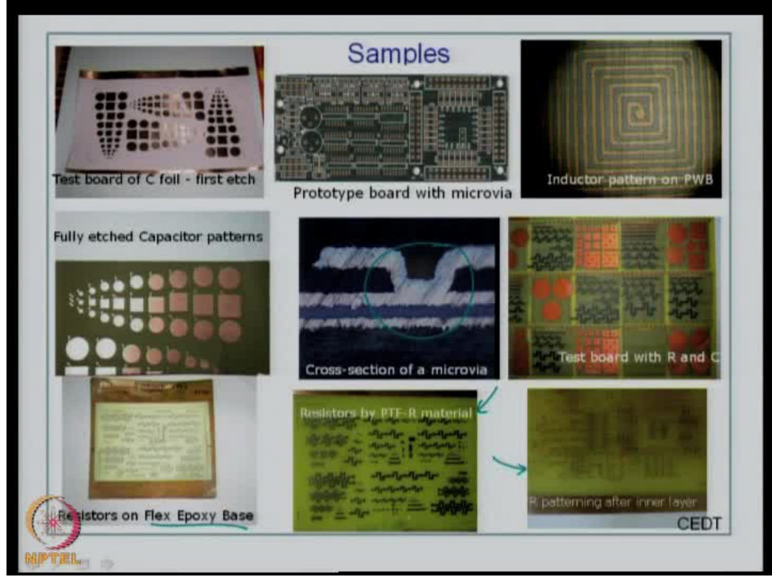
Now as in any process, you have to do characterization of resistors and capacitors. Some of the important points I would like to mention here is, look at the adhesion test I mentioned before copper and dielectric to be checked, look at dielectric shrinkage, it should be minimal, do thermal cycling typically 125 C for 100 less than 10 percent change in R and C values is expected to define tolerances and reliability, temperature humidity cycling normally is done in the industry for new designs, so less than 5 percent failures it could be more rigorous with the industry like less than 1 percent, peel strength in the case of resistors nichrome foil and deposits again very key because after building up you cannot repair these devices.

(Refer Slide Time: 43:38)

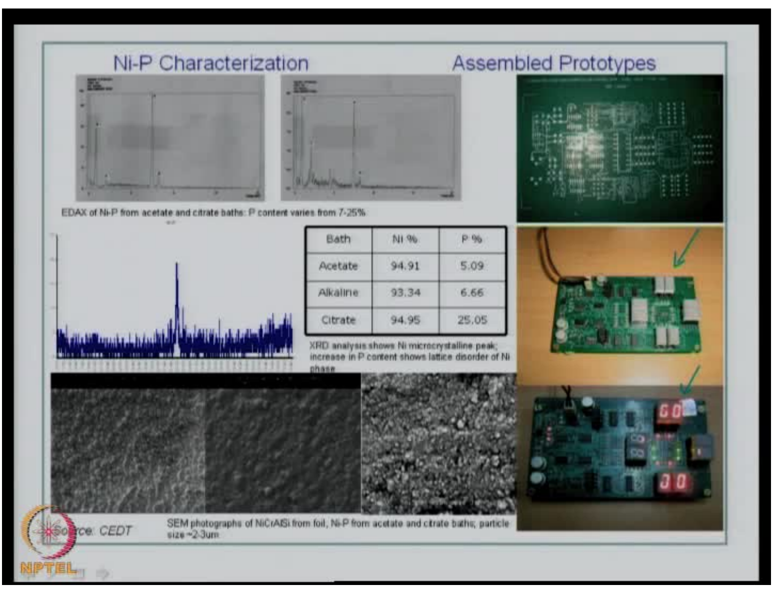


These typically talks about the structure, then the range of values that you get for various structures in terms of dimensions and so on. These are for the capacitors, product A and product B different thicknesses and then you can look at the geometry area and the values that are obtained. These results are in pico farads and this is in ohms. So, normally the reliability is very key issue especially the thermal reliability and electrical test. So whenever such a structure is built, we need to a thermal stability test by doing a thermal cycling in. Here you can see the results of temperature humidity cycling and these are the results of thermal cycling of resistors by foil and electroless methods and then. As for as capacitances are concerned, you have to extract the capacitance using an appropriate equipment. You can do high frequency measurement and look at the adaptability of these structures for such applications.

(Refer Slide Time: 44:24)



(Refer Slide Time: 45:02)

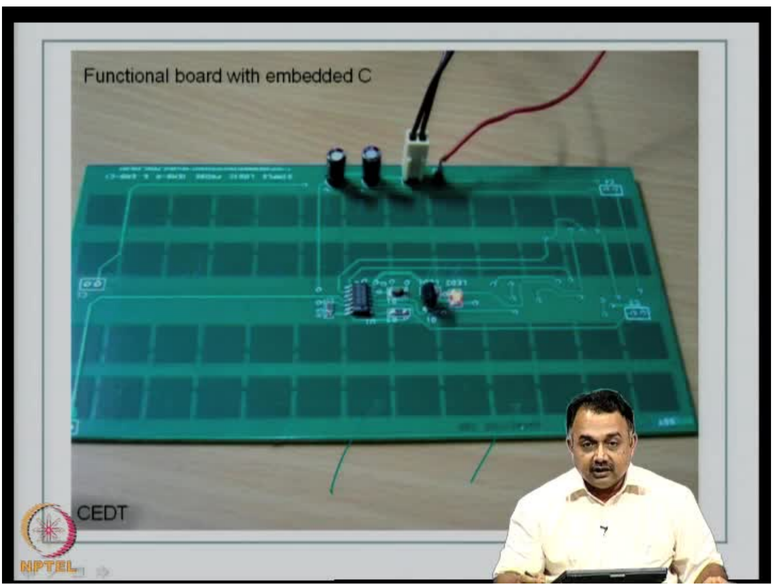


Now these are some illustrations of various samples: inductors, capacitors by foil capacitors, by printed etch method, resistors on flex epoxy base, these are resistors by polymer thick film and this is the cross section of microvia that is highly recommended for hide density inter connect structure using R F C embedded and these are combined R and C board. This is inner layer of a resistor that will subsequently be used for buildup. Here you can see on the right side these are assembled prototypes, what I am trying showing here is a working prototype of a product, a design using embedded R and C. So, it has been demonstrated in CEDT by taking a particular design and kind of

reengineering by modifying the designs especially replacing the normal resistors and capacitors with these structures and demonstrating the working of such kind of a product.

(Refer Slide Time: 45:45)

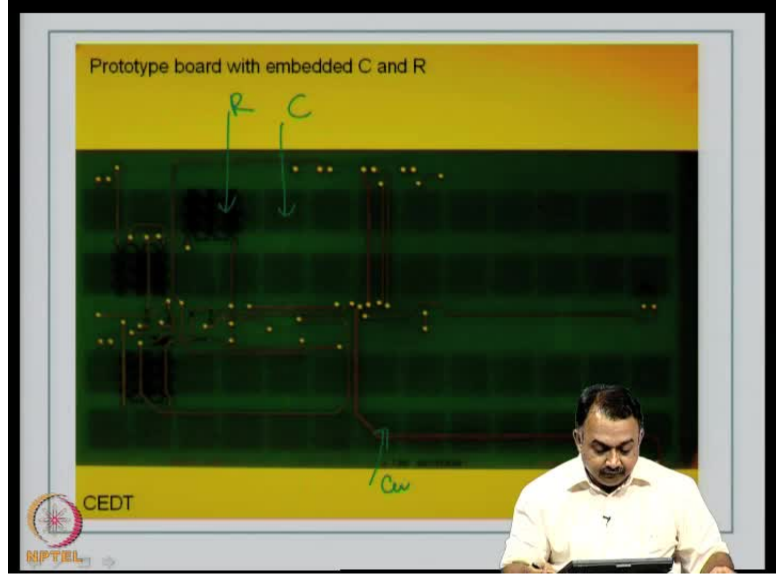
(Refer Slide Time: 46:07)



You can see here a close up of a functional board with embedded resistors. In this particular case, you can see capacitors are mounted, there are active devices, there are other large through-hole components also but all of the resistors have been embedded into the one of the inner layers. Now you can see here in this functional board these are

embedded capacitors. You can see here the inner layer that is capacitor and this is basically a small circuitry demonstrating the working of these embedded capacitors.

(Refer Slide Time: 46:40)



Now the idea is, from this picture if you are using ahigh-end design a manufactureable industry design, the geometries of these capacitors have to be reduced to such an extent that you can reduce the real estate of the entire board. You can see a prototype with embedded C here and then these are embedded resistors. This is you can see in the background. So the top copper layer has been built over the inner capacitor and resistor layers. This is a working prototype board. A case study has been done on a simple demonstration of the effect of using R and C on PWB miniaturization, what we have basically done is taken a standard double-sided board, number of layers is two through-hole technology, lines which are fairly large, through-hole via fairly large the board size you can see 75 square inches.

(Refer Slide Time: 47:45)

Case Study on PWB Miniaturization Implementation

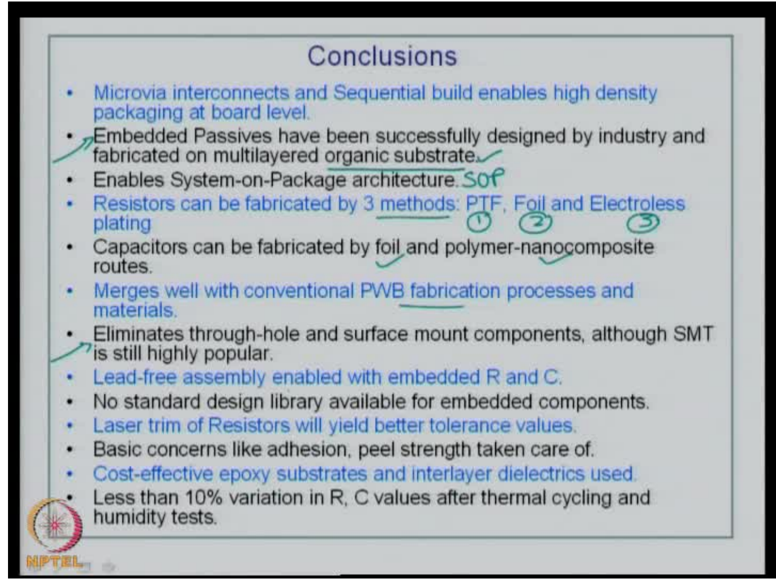
Board Type	No of layers	Component mounting Type	Line widths used	Via type used	Approximate area of board	Board area savings
Standard Double Sided	2	Through-hole	16, 20, 40 mils	TH via 55 mils	75.0 sq. inch	
Standard Double Sided	2	Mixed type-THT and SMD	12, 16, 20 mils	TH via 55 mils	26.8 sq. inch	~60%
Multilayer	4	Mixed type-THT and SMD	06, 12, 16 mils	Microvia (100um) Buried and TH	16.8 sq. inch	~75%
Multilayer (build on both sides)	6 Signal-4 Emb R-2	Mixed type-THT and SMD Emb R ~100 on two sides	06, 12 mils	Microvia (100um) Stacked via	12.0 sq. inch	~82%
Multilayer (build on only one side)	4 Signal-3 Emb R-1	Mixed type-THT and SMD Emb R~100 on one side	06, 08 mils	Microvia (100um) Stacked via	12.0 sq. inch	~82%

CEMT work

Then we try to move into the next step using through-hole and surface moon devices, again two layer board and you can see that the area of the board has been reduced so the board area savings is 60 percent. Now, it has been fabricated as a multi-layer, the same circuit four layers, mixed component type, through-hole and SMD, and then you can see the reduction in the line widths. Microvias have been used, some through-holes have been used and then you can see the reduction in the total area of the board with the board area savings around 75 percent.

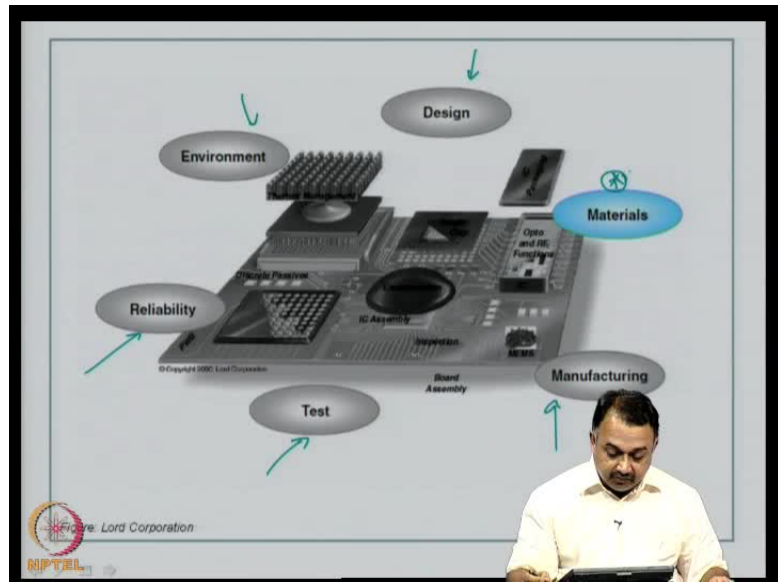
Then multi-layer built on both sides, embedded resistors, two layers and signal in four layers of the six layer board, about 100 embedded resistors were used on the two layers of the embedded resistor layers, you can see line widths used, microvia sizes 100 micron, stacked via technology and you can see the savings 82 percent. Then again a variation in that is that a four layer multilayer board build up on only one side, signal layers three, embedded layers one, slight reduction in the line widths of these conductors, same embedded resistors and then you can see that we are able to show and demonstrate miniaturization using R and C. So, it could be cost effective if we can reduce the area and the volumes of the material that are used and the key here is the line widths it can be generated and the microvia sizes that could be generated. So, line definition and photolithography is definitely a key issue.

(Refer Slide Time: 49:26)



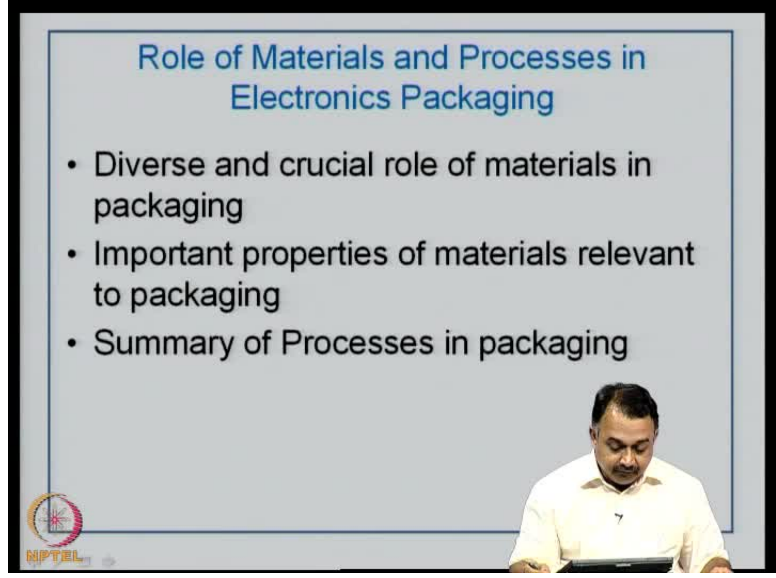
Conclusion on this particular chapter is that as far as embedded R and C is concerned, microvia interconnects and sequential build up technology are very key to build high density in packaging of the board level. You have to integrate them with embedded passive technology and you can be cost effective only if you work on organic substrates. It enables SOP as we have seen. It can be fabricated by three methods PTF, foil and electroless technology. Capacitors can be fabricated by foil and polymer nano composite, merges well with PWB fabrication process, eliminates through-holes technology and surface mount devices. Although SMT is still highly popular, the technology is going to exist definitely for the next five years based on the kind of equipments that we have seen and it is highly popular. We are not going to see a radical change although embedded passives are slowly getting into the thoughts of many industry people, lead-free is possible with embedded R and C, no standard design library is available, laser trim of resistors is possible. Basic concerns are adhesion, peel strength which you have to take care and cost effective epoxy substrates and inter layer dielectric that have to be used and you are look at tolerances after thermal cycling and humidity.

(Refer Slide Time: 51:19)

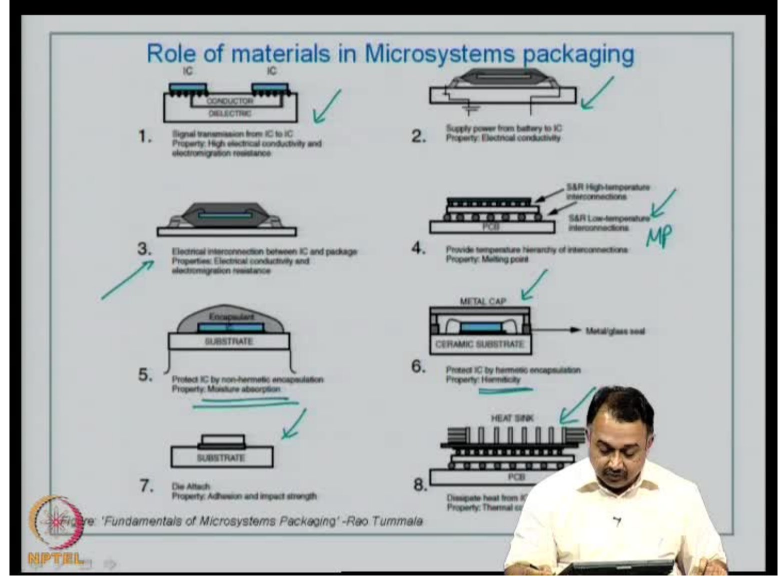


This concludes the chapter on embedded resistor and capacitors. For the next 10 minutes, I will take you through some very important issue that covers the entire course that is electronic systems packaging course. We have seen a system level Printed Wiring Board. We have seen what design is, what the green electronics are, what is reliability, electrical test, large area manufacturing and a key in component here is materials. So, we will briefly talk about materials here.

(Refer Slide Time: 51:36)



(Refer Slide Time: 51:54)



The role of materials and processes in electronic packaging, it is diverse and crucial. Several important properties of materials are relevant to packaging. We need to understand them and will also summarize some processes in packaging. If you look at the role of materials in micro systems packaging, there could be many areas. One could be the signal transmission from IC to IC; there we are worried about the electrical conductivity. Very important. Then we talked about electrical conductivity that is from the battery to the IC again through the interconnections, then we talked about electro migration resistance and electrical conductivity in the electrical connection between IC and package then again various materials are used. You are worried about the melting points of these materials.

Then we talked about moisture absorption we have talked enough about this particular property hermit city in packages kind of metal caps that you are using to protect the die. Then we talked about die attach materials especially in first level interconnect packaging and then we talked about thermal issues. Thermal conductivity is a key issue. Heat sink material is also very important.

(Refer Slide Time: 52:58)

PACKAGING TECHNOLOGIES	FUNCTIONS	MATERIALS	PROCESSES	PROPERTIES
Single Chip	• Protection • Interconnection • Heat Dissipation	•Plastics •Epoxy + filters •Ceramics	• Compress Molding • Tape casting • Dry Pressing	• Permittivity • TCE • Thermal conductivity • Moisture Absorption
IC Assembly	• Electrical connection	• Copper • Aluminium • Gold	• Thermocomp. Bonding • Ultrasonic bonding	• Electrical conductivity • Oxidation resistance • Fatigue • Creep
TAB	• High I/O density	• Cu on Polyimide	• Electroplated copper • Polymer deposition	• Heat resistance
Flip Chip	• Reliability	• Pb -Sn solder • Non-lead solders • Cr-Cu/Au • Cr/Cu/Ni/Au	• Reflow • Evaporation plating • Evaporation dep. • Electroplating, etching	• Wetting • Surface properties • Melting point • Electromigration resistance • Interdiffusion
	• Environmentally friendly	• Conductive adhesives: Ag-filled epoxy • Underfill: Silica filled epoxy	• Screen printing • Curing • Dispensing	• Electrical conductivity • Modulus • CTE • Nontoxicity

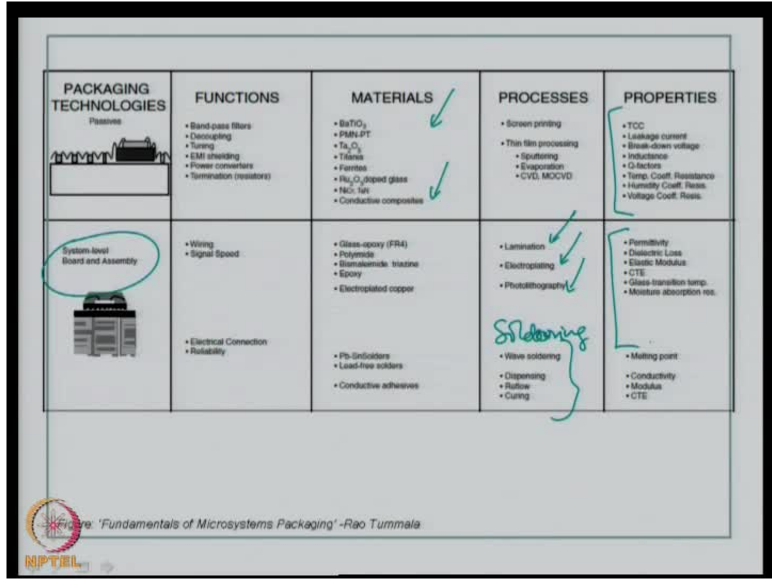
Figure: 'Fundamentals of Microsystems Packaging' -Rao Tummala

NPTEL

So there are various materials that are used. Various functions that can be defined, processes both that that are in the first level packaging and the second level packaging. So, in the single chip for example, we talked about protection, interconnection, heat dissipation, materials that are used plastics epoxy and filters ceramics and so on, processes like compress molding, tape casting, dry pressing, and so on properties like TCE, permittivity, thermal conductivity, and moisture absorption.

In the IC assembly like tab, flip chip and wiring bonding we have seen various materials used: copper, aluminum, gold, polymides, epoxy materials, Teflon and so on. There are different solder materials that we have seen lead based, lead-free and then the first level you have chromium, copper, gold, nickel being used then lot of conductive adhesives we have seen are used today that are environmentally friendly.

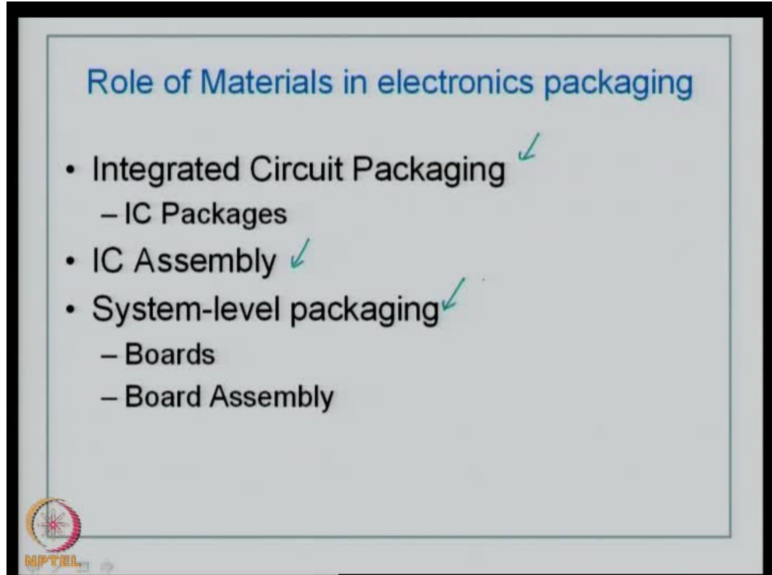
(Refer Slide Time: 54:07)



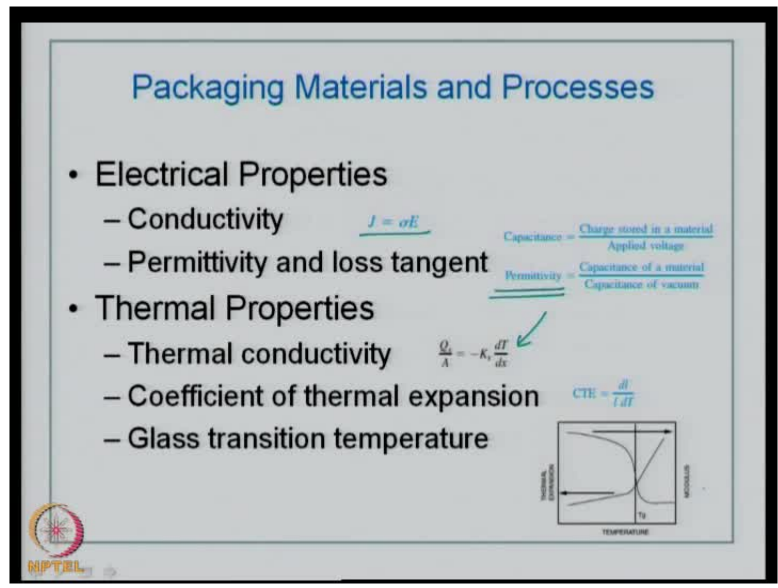
As far as the passives are concerned, there are various materials just now we have seen thick film hybrid circuits or thick film LTCC processes materials like barium, titanate, tantalum oxides, ferrides, ruthenium oxides, polymer thick films, carbon paste, conductive composites etcetera. All of these are new materials that are being used and we have just now seen various properties that are key to passives technology like TCC, leakage current, q factor, temperature coefficient of resistance and so on.

Now finally at the system level also, they are very important because when you talk about building system level Printed Wiring Board, here again the key issue what kind of organic substrate that you can use, what kind of reliability issues you will get with processes like lamination, electro plating, photolithography, soldering processes very key and we are spent lot of time on soldering processes and there are various properties of materials that we have seen like dielectric constant, loss, elastic modular less strain issues, CTE moisture absorption and so on.

(Refer Slide Time: 55:36)



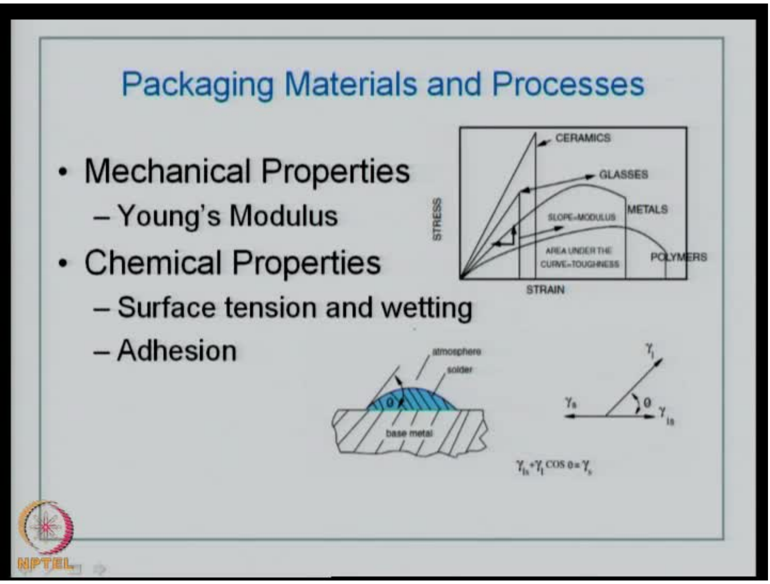
(Refer Slide Time: 55:45)



So materials play a very key role in deciding the functionalities of products. As we have seen in the previous slide, it could be in IC packaging, it could in IC assembly or in system level packaging. The electrical properties briefly that you must be aware of which I want to some summarize and give it you in a nut shell is conductivity, remember this equation, permittivity, and loss tangent, we were talking about dielectric constant, capacitances of materials, ratio of capacitances of material to capacitances of vacuum ,that is permittivity very key property, thermal conductivity again it is the amount of heat transferred through a material per unit of time denoted as heat flux that we have seen,

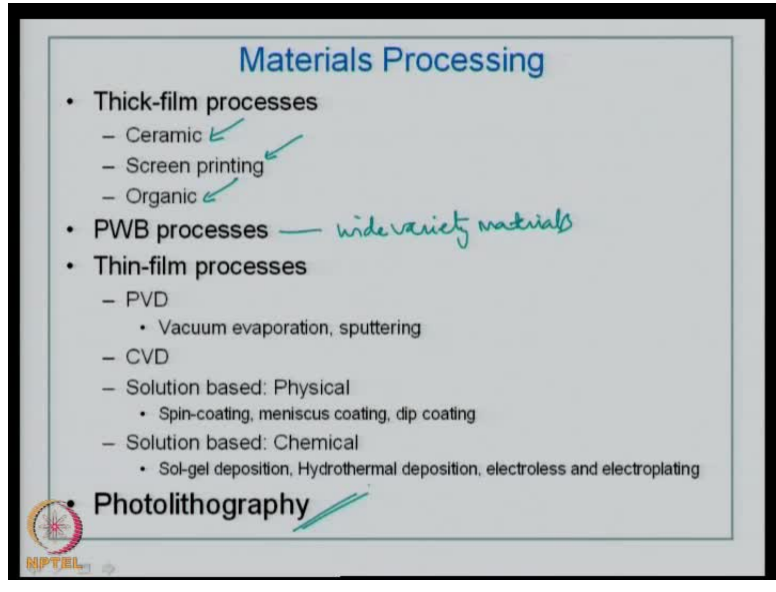
and area is here is very important d t by d x is a temperature gradients we have seen, CTE again talks about dimensional change, property of polymers, and related material.

(Refer Slide Time: 56:40)



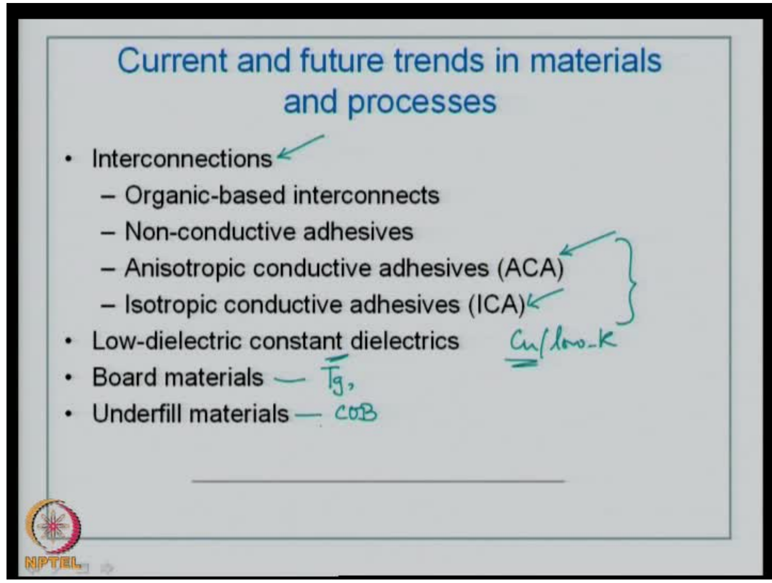
Then mechanical properties we have seen again Young's Modulus very key because it again talks about the stress strain relationship and how these affect the materials that are being used in system level manufacturing. Chemical properties, surface tension, and wetting especially in the case of solders adhesion in the case of adhesives, conductivity and so on, all of these have been reviewed.

(Refer Slide Time: 57:07)



You should also know about thick film processes. We have seen ceramic LTCC, screen printing key issue, organics you have to be aware of. All the PWB processes used a wide variety of materials there are innumerable materials that contribute to the reliability of the Printed Circuit Board or Printed Wiring Board. Then thin film processes again for specific applications like PVD, CVD, physical solution base like spin coating, meniscus coating, dip coating, chemical solution based like sol-gel and not to forget photolithography process.

(Refer Slide Time: 57:49)



Now finally, the materials part of it on the processes in first level packaging and second level packaging are defining today the road maps in industry. New materials are being proposed; new materials are being tried by industry to generate road maps that are challenging for the industry especially in the area of interconnects in the first level and second level. So, we are talking about today organic based interconnects, nonconductive adhesives play key role when you mount this devices like tab or a flip chip so they definitely aid or play key role in defining the interconnects on the system. .

Anisotropic conductive is growing. Lot of challenges in anisotropic conductive adhesives and isotropic conductive adhesives we have seen what they are when we talked about packages. Today the key is copper low K for highly reliable interconnects. So, the key is how do you use copper in conjunction with low K materials, then again board materials that are green in nature, high Tg and adaptable to PWB processing and underfill

materials, if you are using chip on board technology and so on. They are very key issues when you are using flip chip for example, and then encapsulation materials if you are using chip on board technologies are also very key. So, that concludes the brief overview I wanted to give on materials and processes in electronics system packaging. This concludes the module on embedded passives, embedded resistors capacitors mainly and then overview on materials and processes in electronics system packaging. .