An Introduction to Electronics Systems Packaging

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Module No. # 09
Lecture No. # 40
Introduction to embedded passives
Need for embedded passives
Design Library
Embedded resistor processes

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We will begin with the next module in this electronic systems packaging course and this is titled embedded passives technology. Embedded passive components, as you know play a very vital role in designing system level Printed Wiring Boards. Therefore, we are going to talk about the current state of the art technology, which is embedding passives on to a system level Printed Wiring Board.

All of you have heard and used regular components, passive components, and active devices. Now, we are going to see how to create or use embedded passives in your design.

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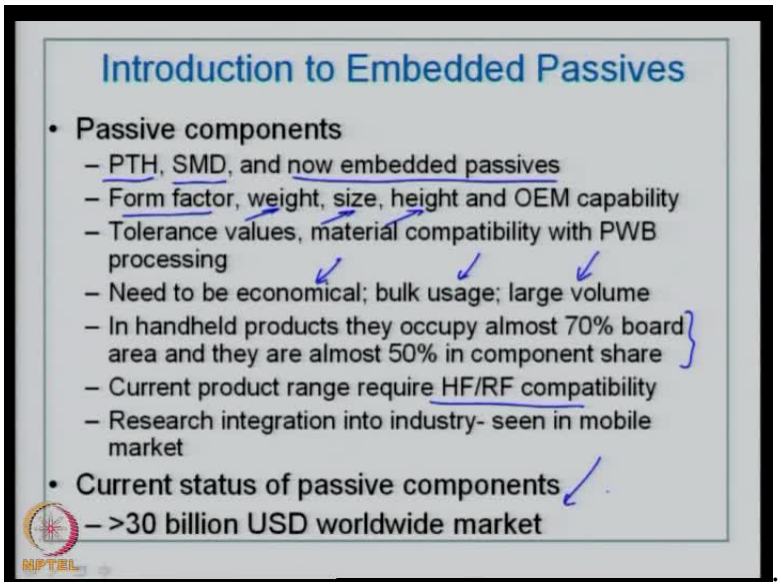

Let us get introduced to embedded passives technology. Firstly, passive components: we have heard about plated through-hole components, surface mount devices and now we are going to talk about embedded passives. That is the flow of this particular lecture.

We have seen different packages in one of the earlier chapters. We have seen through-hole components and the requirement for assembly of through-hole components and so on. Now, we are going to talk about the requirement of using passives in embedding them, while fabricating a substrate that is used in system level packaging.

Generally, for passive components we are worried about the form factor, weight, the size, the height of the component, and the OEM capability. OEM means Original Equipment Manufacturers capability. As a passive component usage, we are worried about its value. We are worried about the tolerance that is marked for the passive component during its manufacturing and the material compatibility with PWB processing. Because as we have seen in the case of surface mount devices, there has been a shrinkage of the devices in terms of size and form factor and we have seen alternatives in the assembly process.

In some cases, we are using wave soldering. In some cases, we are using a reflow soldering process. As far as the PWB fabrication is concerned, we have to be very clear about what kind of passive components footprint we are using in the design; because if

we use a through-hole device and SMD device, you have different design considerations to be thought about.

Now, as far as the passive components in general are concerned, we are going to use bulk volumes in large scale manufacturing. Therefore, it needs to be very economical, because we are going to talk about new products, new systems that will use a large number of passive components. Therefore, it has to be economical, cheaper, and cost-effective so that the manufacturer of systems or products can consider using that particular passive device in large volumes.

Now, if you look at any product, the percentage of passive components is very large. For example, in the next bullet I have mentioned here that in handheld products they occupy almost 70 percent board area in terms of size, footprint, and the interconnects. They are almost 50 percent in the component share as far as active and passive components are concerned.

Therefore, this is a very important statement. As far as a designer is concerned, your aim would always be to reduce the footprint area; so that you can get a high density board; also in the case of passive components. As you have seen, the footprint area of the active devices is shrinking and it is but natural that you will move into using passive components with smaller footprint area.

A large change has occurred due to SMD footprint being very small. Now, we are going to see how embedded passives can help in such a design issue. The current product range requires high frequency and RF compatibility. Research integration into industry is currently seen in the mobile market.

As far as embedded passives are concerned, we have seen some kind of an integration of the research results into the industry as far as mobile market is concerned. Whereas for other products, it is still in the prototyping stage and the materials that are used for the fabrication of these devices has to be seen from the point of view of high frequency compatibility and so on.

So, when such a synthesis is done with new materials for passive devices this is one very important aspect, testing these devices for high frequency compatibility. Generally, the

market share of passive components worldwide is more than 30 billion US dollars. So, it is a large market.

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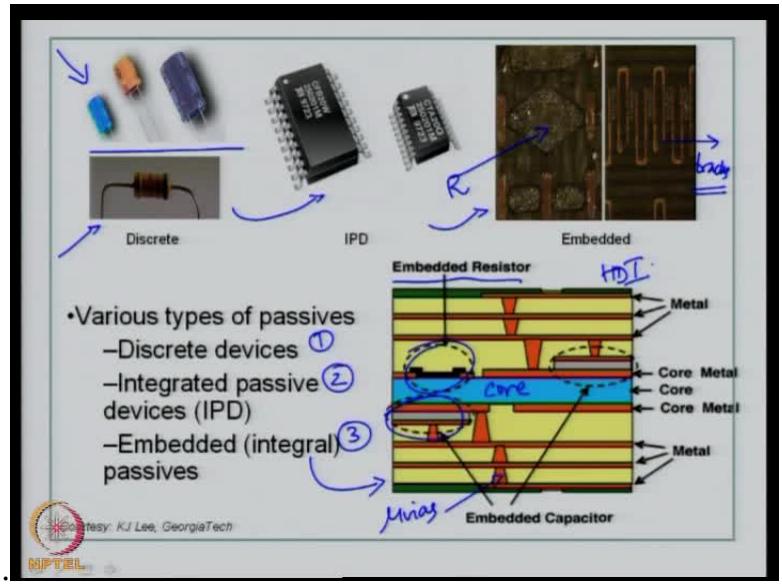

In this illustration, you will see on the left here, these are the through-hole devices, capacitors could be electrolytic capacitors or it could be axial form of capacitors, then you can see resistors here, normal and electrolytic capacitors and similarly, you can see discrete resistors with color coding and so on. These are generally marked with the values of capacitances or resistances from the color coding and then they have long leads. We have seen and discussed during this course, the difficulty in electrical design issues with leaded devices but nevertheless, they have played a great role in the electrical design for more than three decades and they have been part of many systems.

Now, because of a large footprint area occupied by these capacitors and resistors in through-hole format, the migration took place to integrated passive devices, where the footprints of these packages will be in the form of a Dip packages or surface mount device, and small outline IC kind of a format and there will be integration done of the capacitors and resistors in this package, plastic package typically.

Then came the migration into embedded devices as you can see in this picture here, this is a Printed Wiring Board on which there are footprints generated for resistors which have been fabricated in to of that particular layer fabrication and then these are

connected to the tracks of the Printed Wiring Board to the required interconnect scheme according to your schematic.

So, summarizing or take away from this slide will be various types of passive devices are known. First thing is the discrete devices, second is the IPD or integrated passive devices and the third is the embedded or integral passives. As you going to see, it is going to be integral of a system level Printed Wiring Board, the concept of which is shown here. This is similar to your system on package configuration and you can see there is a core Printed Wiring Board and then you can see the multi layers and connected by microvias and then you can see there is embedded resistor here, then there is an embedded capacitor that is generated as part of the system.

Then you can also have inductors generated, and then you can have metallization done on top of these resistors and capacitors to connect to inner layer coppers by microvia technology. So, this is typically a high density interconnect scheme that you are already aware of from the previous modules and we are not trying to see how you can device a scheme for embedding resistors and capacitors in this format.

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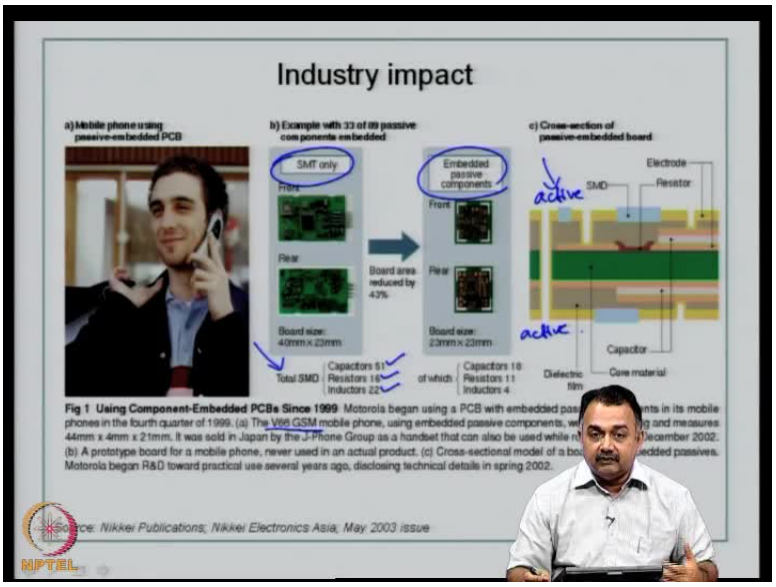

Just to let you know that the industry impact as far as embedded passives is concerned, I want to present a case study, a market scenario that has happened from Motorola, the handheld product in the handheld industry segment. You can see that the particular model of Motorola typically the V66 GSM mobile phone, the design consideration was

made to convert the SMT components to including embedded passive components plus SMT devices as usual.

Now, as far as the literature information is available the total SMD resistors in that particular design was let us say capacitors 51, resistors, 16, inductors 22 of which 18 capacitors, 11 resistors and 4 inductors were converted into embedded devices. So, there is reengineering done. A different layout scheme was considered to translate those SMD devices, key devices into embedded passives format and it was considered during the fabrication of the system level Printed Wiring Board.

As we have seen the previous slide, this will be the typical cross section of the passive embedded board. Here again, footprint becomes very important. The greatest thing about embedded passives is that it allows you to place more active devices on the top and bottom areas of the system level Printed Wiring Board and you can do a vertical integration. You can increase the number of layers of the system level Printed Wiring Board. You also have the flexibility to choose different dielectric materials for your capacitor and in fact if you want to have 2 resistor layers, 2 capacitor layers independent of each other but then connected to the main core that can be designed as well. You can use different resistor materials and different capacitor materials with a set of properties that are suited for your application.

So, this is a very good example and you can see here, the board area in this particular case study has been reduced by 43 percent. So, you can imagine a scenario when more number of components could be converted to embedded passives.

After having this case study before you, we will discuss the pros and cons of using embedded passive component technology. Why embedded passives? That is the main question. It improves the packaging efficiency because now we are going to do away with packages right and you are going to integrate it into the board.

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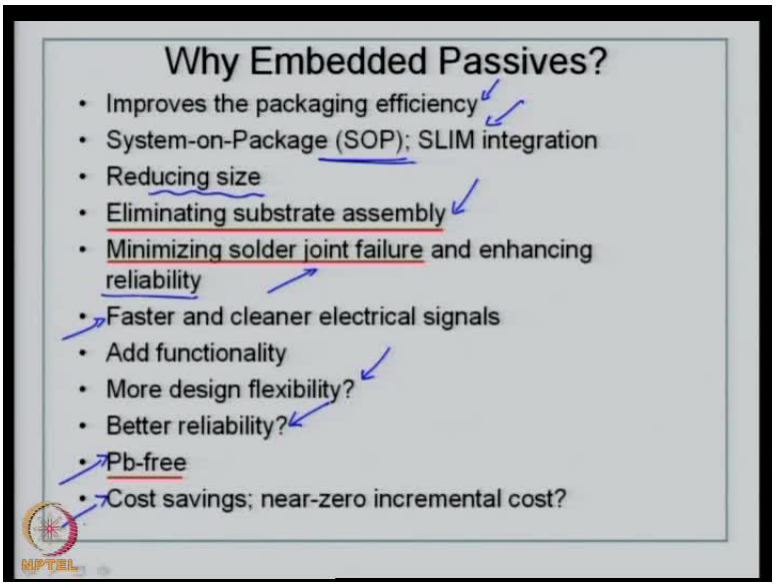

So, it is assumed that it will give a higher packaging efficiency. Now, the model that we have seen in the previous two slides really indicates that it is a system level integrated module and typically it signifies a system and system on package concept which we have seen and discussed in the module, a chapter on packages.

So, if you have questions on SOP, you can go back to the chapter and have a recap on what an SOP is. The other impact that embedded passives could give is reducing the size. This looks to be very important, attractive from the point of view of reducing your product size.

Because to some extent, your Printed Wiring Board plays a major role in defining the size of the product, eliminates substrate assembly, because if you are going to build the passives on the board, then all of those devices which you were doing by automated assembly process could now be shelved.

Minimizing solder joint failure, because you are avoiding solder joints totally from this process and enhancing the reliability therefore. The reliability is built on to the Printed Wiring Board and obviously once the Printed Wiring Board with these devices are built, you are going to check the reliability of that system. You are going to check for failures. You would be doing bare board testing with the passives on board. You would also be doing a thermal humidity cycling with the passives on the board and therefore, you could get a good measure of the reliability issues connected with such a system.

But the big advantage is that you could do away with soldering process for these replacements and because you are doing away with solder joint it is expected that you could get from the electrical stand point, faster and cleaner electrical signals. It adds functionality to the board; you have more design flexibility as we will see as we go along in the individual cases of resistors and capacitors. We will see how you can play a major role by building your own design library for resistors and capacitors.

Better reliability. It could be a question, because industry today has really understood well the plated through-hole and surface mount device formats and thousands of products have been built using this format and people have understood the reliability issues from this format. Now, moving over to a new technique which is hardly about 5 to 8 years now since prototyping has begun, there is always a bigger question mark on how reliable this will be. We have to move into those systems because it provides more flexibility and if you can build a new methodology or reliable methodology in building and assembling these devices, then we can expect better reliability. So, materials issue becomes very important for in-built reliability in this system.

One of the most catchy points in this particular slide would be that going into embedded process will make your system lead free, because you are not doing solder joint and you are going to basically concentrate more on active device attachment which could be lead-free and you can put this as a case for green electronics being implemented in your system.

There could be cost savings, if your materials cost are going to be less if you can integrate well into your PWB production and near zero incremental cost.

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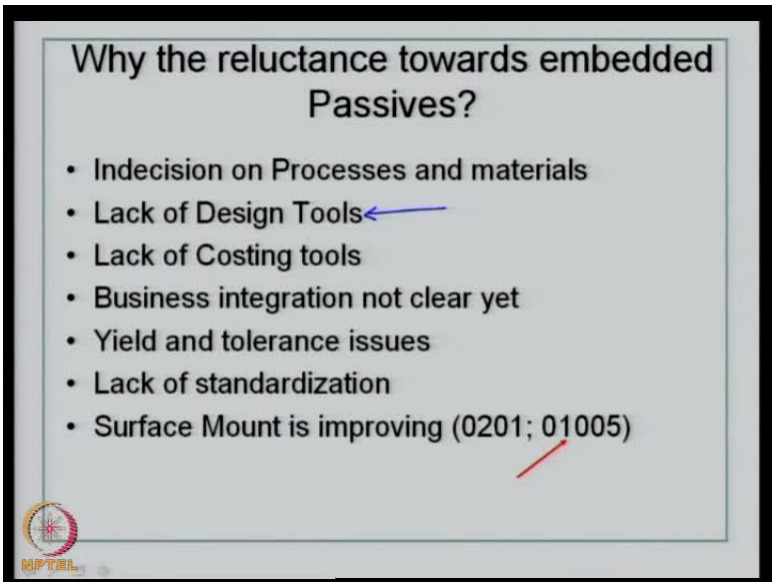

Now, the other question is why the reluctance towards embedded passives. Why are not many people getting into embedded passives design implementation? There is an indecision currently on the processes and materials that could be used. It is not yet large scale. There are not many industries that are using embedded passives in their systems or it is not highlighted in a particular system. Currently my impression is that passives are very ideal for handheld products rather than for large boards or systems.

An indecision on the processes and materials means that are there alternatives for creating or different rules for creating resistors. What are the different process steps for creating capacitors and inductors and so on? So, people are beginning to understand this and unless people in the industries are convinced about cost related issues with these processes, there will be this reluctance to move into these technologies?

Lack of design tools, so not just the manufacturing. As designers need to be educated, trained about the concept of embedded passives in electrical design, in your CAD system, how do you implement this? Are there any tools available in your CAD that could be easily utilized like your PPTH component or a SMD device? How can they be just pulled from your CAD library and placed in your schematic and then you could not worry about tolerances and values and so on? So, that is going to be a major issue.

Lack of costing tools. Now, currently there is actually lack of data about migration to this and then the cost that this particular technology possess and the capital investment that an industry has to in invest in such a migration . So, this could be a major question.

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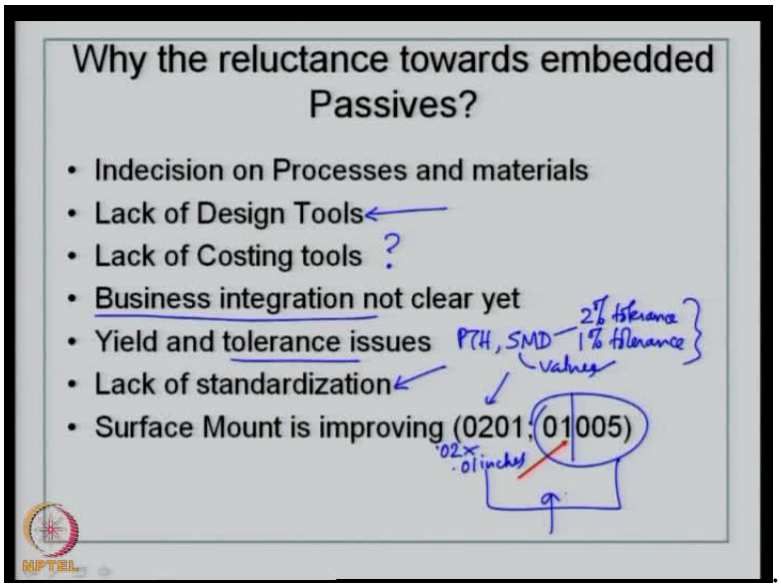

So, the business policies or the business integration in industry is still not clear. But this could be overcome by some training and understanding the concepts from people who have worked with these tools especially the CAD tools and the process methods. Now, you could buy a plated through-hole component or an SMD component with let us say, a 2 percent tolerance very clearly marked on the component or 1 percent tolerance. Then you could plan your design. The values are well marked on the component.

But with embedded resistors, how are you going to fix the tolerance. Because if it is going to be integrated with your PWB as we will see later, there are many issues that bother in realizing yield as well as tolerances. There are no standard tools for both fabrication and design, so that could be a major hindrance and on the other hand for people who have been using surface mount device for a very long time and who have been used to working with small footprints like 0.02 inches by 0.01 inches are beginning to use 0.01 inches by 0.005 inches form factor SMD chip components.

So, equipments are available to utilize these very small footprint passive devices. So, why the need to go to embedded if you can still manage with this kind of small devices. So, that is the major question that designers and assembly services are thinking about.

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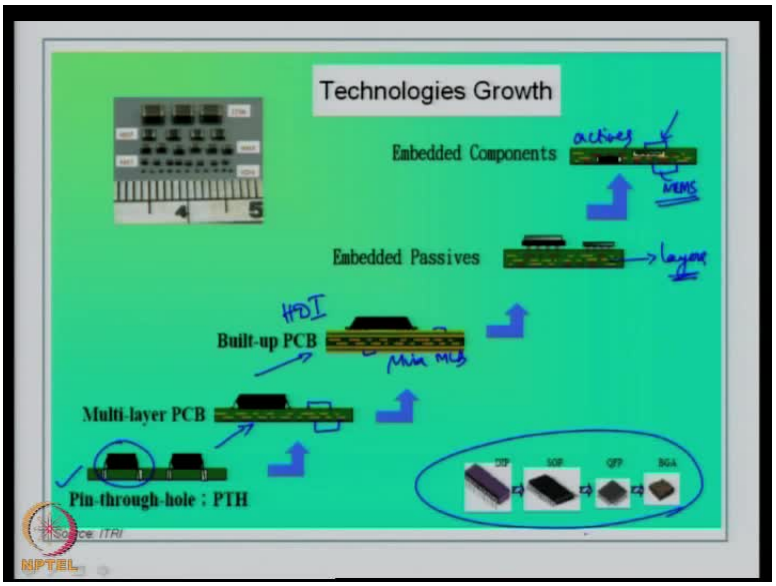

Just to recap the technology growth, before we actually get into embedded passives discussion, all of you know about the pin through-hole or plated through-hole. You can see the large size of the components, through-hole components, and active devices, a multi layer PCB much depends on the number of layers that you build. You can have your passives mounted on both sides of the board then you have the high density built up PCB or build up technologies that we have discussed. So, here again you will have multi layers with microvias and in this case, the surface mount devices will be placed on both sides of the system level Printed Wiring Board.

Now we are talking about embedded passives which means the inner layers will have the passive devices and there is also a high-end research going on at various universities on embedded components that is active devices being placed inside the system level Printed Wiring Board especially organic substrates. And the real estate on the top and bottom are being utilized for mounting your select active devices like your FPGAs or it could be your MEMS devices and special components that cannot be integrated and that requires frequent repair or replacement in case of fault measurements.

We have also seen the kind of active devices that have been seen over the last 4 decades, great improvement to the current CSP.

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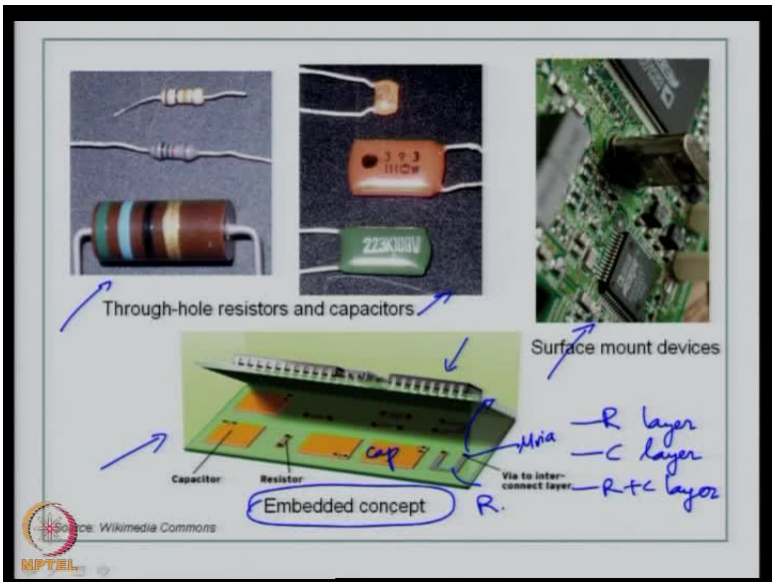

So, this is once again to recap. This is the through-hole resistor, the capacitors, through-hole then you can see in this particular illustration, surface mount devices in the form of actives and passives and this is the concept of embedded. As you can see, there are active devices here in the top and you can see these are the capacitors and these are the resistors and you can see the microvias being designed to interconnect to the connections copper at the top.

So, you have great flexibility. You can have R in one layer, you can have a capacitor layer or you can easily combine R plus C in one layer, if the density is low. You can have multiple layers, two capacitor layers, two resistor layers as per your design. If it is a high density board and interconnect by microvias to the active devices, you could create a heat sinking as usual. So, there are chances of great design flexibility using this concept.

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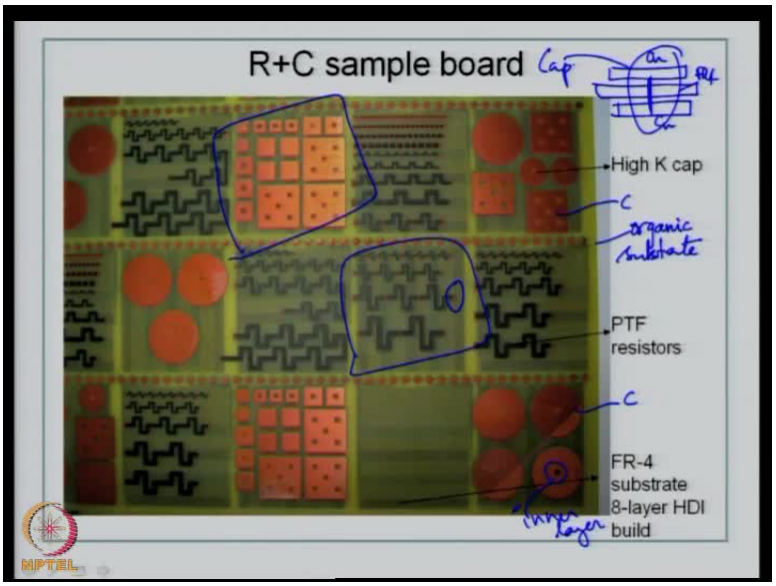

Upfront, I want to show you a sample of the features that you could expect from resistor and capacitor that have been embedded in an organic substrate. So, you can see here, this is an organic substrate. What I am showing here is the buildup player on which both the resistors, these are the capacitors you can see the black points here that you see are the resistors and these are the capacitors.

This is the flame retardant 4 FR4 8 layer high density interconnect. What strikingly you will see here first upfront is that the java trace of resistors and capacitors are varying. This is a typical test board and being a test board you could see various sizes of capacitors, square, circle and then the geometries serpentine kind of a structure meandering resistor geometries, from large to very small geometries and these are interconnected to inner layers of the 8 layer board. For test purposes, you can see there are copper terminals at the end of the resistor pattern. Typically in a capacitor, what you will see at the center is a microvia interconnect that goes to an inner layer and you can typically measure capacitances between layers.

If you look at the cross section, you could have copper, then you could have a dielectric and then another copper layer. So, this is a sandwich of copper, copper and theFR4 and then you could interconnect them by vies and this could be your capacitor. So, you could measure the capacitance of this kind of structures by varying the dielectric material by varying the thickness of copper, the dielectrics and so on.

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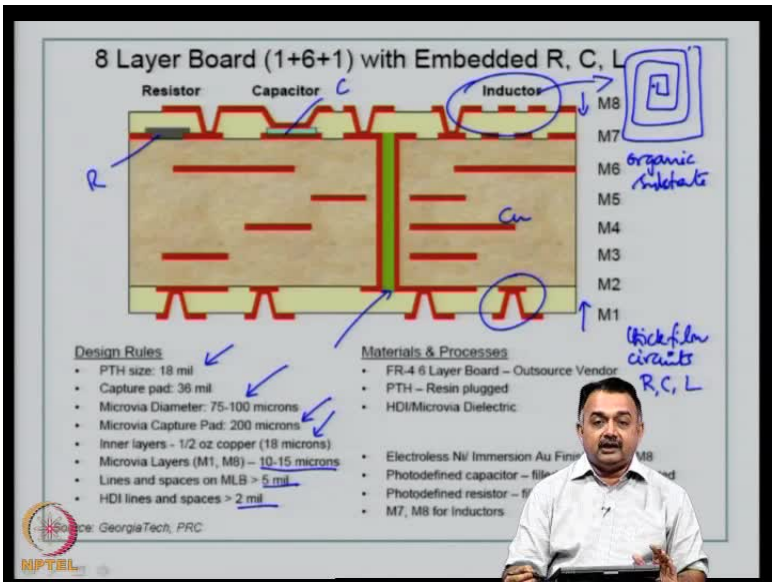

This is again a cross section of how currently embedded passives are being manufactured on organic substrate. Again I emphasize that organic substrate is cheaper compared to a ceramic substrate and this particular slide should give you some thought on a particular technology that we discussed earlier called thick film circuits.

Very briefly I mentioned about this where we use R C and L, the resistor, capacitor and the inductor in the form of inks printed on ceramic substrates and they will be co fired at fairly high temperatures varying from 500 hundred to 1000 in LTCEC which is just typically between 300 to 500 and HTCC from 600 to 800 or 900 degrees depending on the material substrate that you have chosen. And they form interconnects during the co-firing. So, embedded R C and L in some sense have been done with ceramic substrates before. Only thing it has been known as thick film hybrid circuitry but now this concept is with organic substrates.

Typically you have very common glass epoxy Printed Wiring Board. This cross section shows you various metallic layers right from M1 to M8 and then you can have through-hole structures for interconnecting very large separation of metallic layers, a microvias here, this is the copper, then you could have the resistor here, the capacitor and then the inductor that is formed with the copper on the board. So, you can have typically an inductor like a spiral here and then you could measure the inductance between the terminals. You could also realize inductors on board.

Now this is a slide from georgetic P R C, where we design this embedded R C and L and then this was fabricated and tested. Basically what I am trying to highlight here is that this is a high density interconnect circuit because you can see pad sizes are very small, microvia diameters are 75 to 100 microns, capture pad is 200, inner layer copper is 18 micron thick, there are microvia layers M1 to M8, 10 to 15microns, spacings are 5 mil, HDI lines are 2 mil 50 micron and so on. So, typically you expect a high density circuitry when you design embedded passives.

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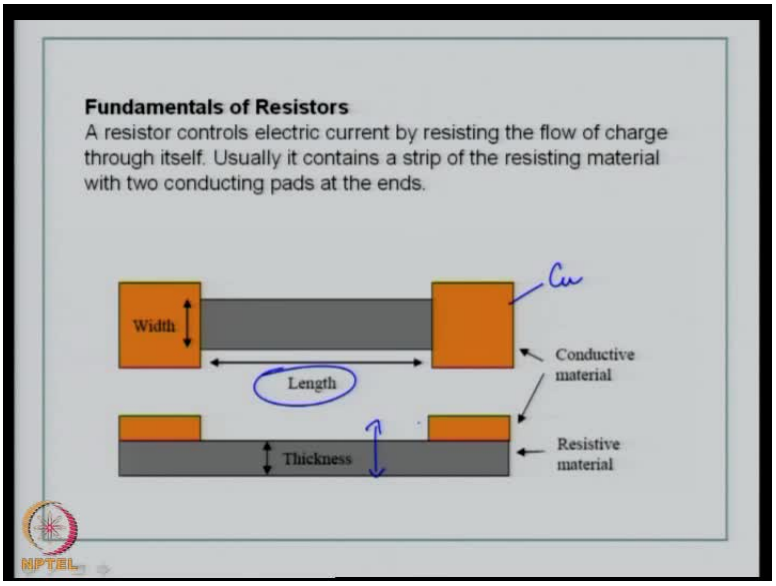

Let us get into some fundamentals before we actually go into the process details of embedded resistors and capacitors. A resistor controls electric current by resisting the flow of charge through itself. Usually it contains a strip of the resisting material with two conducting pads at the ends. Basically what you are seeing here is a conducting material like copper and then you have which is basically connected to the rest of the Printed Wiring Board or solder joint using solder paste material reflow, wave soldering process and so on.

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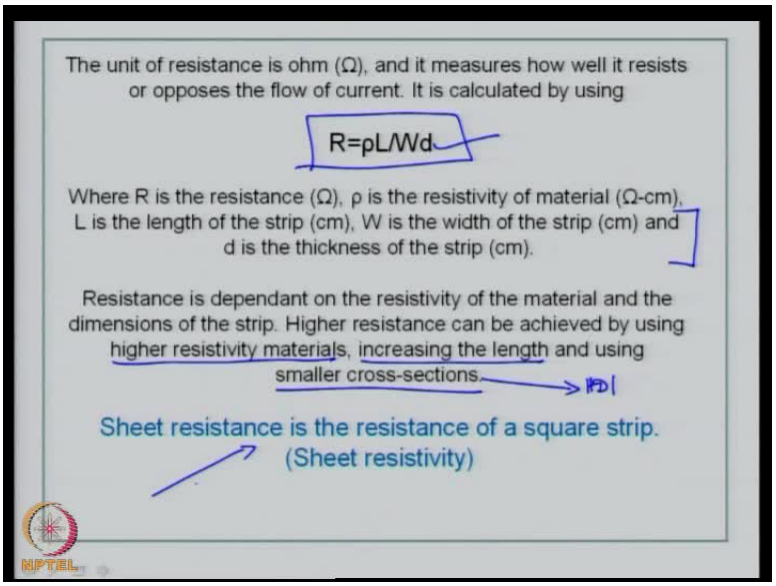

And then the key issue here is the length of the resistor strip and the thickness. This is going to be a key issue in designing embedded passives. So, again a few of the basics which all of you are aware of, the unit of resistance is ohms and it measures how well it resists or opposes the flow of current. It is calculated by using the well known equation R is equal to rho into L by A area which is a width times the thickness of the strip that we saw in the previous figure.

So R is the resistance in ohms, rho is the resistivity of the material. We are going to talk about sheet resistivity here being an important factor in deciding or choosing resistor materials. So, rho is the resistivity of the material, ohms centimeter, L is the length of the strip that you have to design W is the width of the strip that you have to fabricate and d is the thickness of the strip.

So when you fabricate, the key issues that you have to talk about is how do you define the length, width and thickness because that is going to be related to your resistance finally. How are you going to define tolerances of your geometry during the fabrication? Normally when you buy an SMD component or a through-hole component, we do not worry about this because it is well defined by the manufacturer. So, resistance is dependent on the resistivity of the material and the dimensions of the strip. If you want a higher resistance, you can achieve it by using high resistivity materials, increasing the

length of the strip and then using smaller cross sections because this is the key. In high density, you do not want large areas to occupy in the layers.

So, key to amalgamating this process with HDI will be to define using photolithography, smaller cross sections of your resistor material and then finally the take away from the slide would be know what sheet resistance is?

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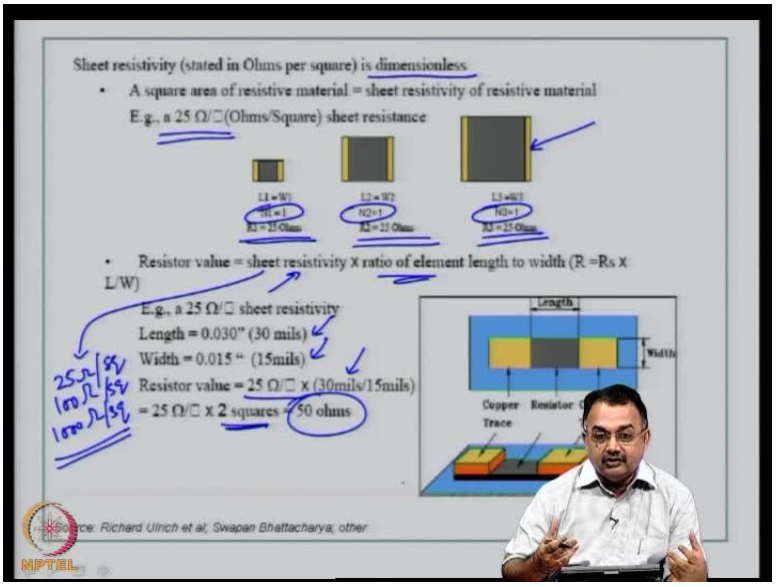

Sheet resistance is the resistance of a square strip. You can call it as sheet resistivity and will be using this term more often. Sheet resistivity stated in ohms per square is dimensionless but this gives you a very good idea about what material you are going to use.

A square area of resistive material is the sheet resistivity of the resistive material. For example, if you have a 25 ohms per square sheet resistance, then if L is equal to 1, if L1 is equal to W1 and the ratio is 1, then your R1 is 25 ohms. If the ratio increases or if the size increases L2 W2, then the ratio is still 1 and the value is still 25 ohms. If it is three times then L3 is equal W3, the ratio is 1 and your value of this geometry of the resistor is still 25 ohms.

So the key will be to reduce the geometry and then use larger sheet resistivity material to get larger values. Resistor value equals sheet resistivity and then you need to know whether it is what material you are using whether it is 25 ohms per square or 100 ohms

per square or 1000 ohms per square accordingly, if you know the quality property of the material then you can design.

Suitable geometry is for certain range of values in your design. For example, at 25 ohms per square sheet resistivity material is being used, length is 30 mils, width is 15 mils then the resistor value is 25 ohms per square and then the ratio is 30 by 15, which is 25 into 2 squares, the value is 25 ohms. So with the 25 ohms per square sheet resistivity material and if the ratio is 2, you can get 50 ohms. As a designer your CAD does not have this data right now, so CAD programs have never considered so far, these kind of data that the geometries that you can pick.

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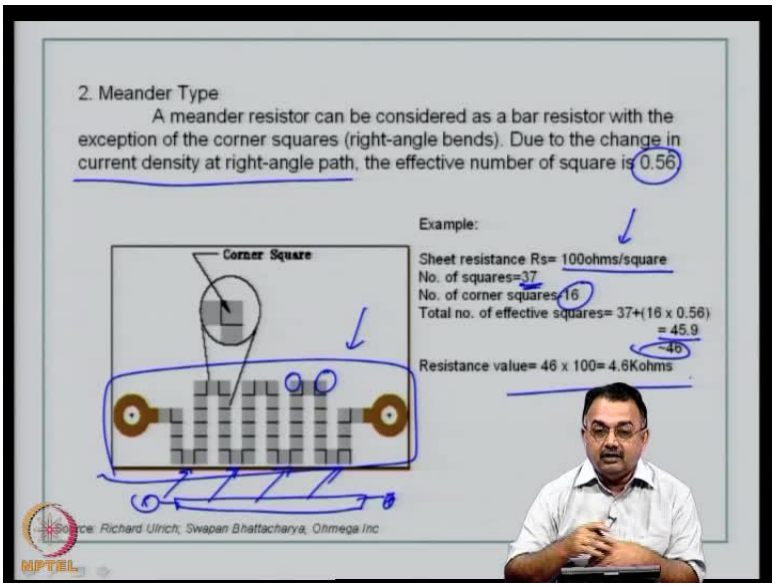

Of course you can create these geometries very easily in your CAD and then store it as your own library. So, this is very important for a designer. If you look at the basic resistor pattern, there are two types. The first thing is the bar type, where the geometries, the pattern is simply a sequence of bars, multiple squares so this is a square, multiple squares so N is greater than or equal to 1 then you have partial squares N is less than 1.

Then you have meander type resistors which can be considered as a bar resistor with the exception of corner squares. You can see that the pattern is meandering over a given area. The idea is to increase the length of the entire strip by using this pattern instead of a simple bar between the stubs. This helps in increasing the number of squares and increasing the value of the resistor and when use right angle bends, there are problems

with manufacturing as you know at the right angles. There are also electrical issues because there is a change in current density at the right angle path, we have seen this when we talked about the flux circuits.

So, the effective number of square for each square is typically 0.56 only. So, taking into consideration losses and so on, if you have such a design that you have to consider, then please look at the following calculation for resistance value of such geometry. The sheet resistance here R s is 100 ohms per square that is the material you are going to use; number of squares here is 37. Total number of corner squares in this is 16, so effectively you want to convert this 16 into 0.56, add it to the number of squares you get 45.9 which is rounded off to 46.

Therefore, the resistance value for this particular geometry with this number of squares is essentially 4.6 kilo ohms. So, if you are in your prototyping or in your large scale manufacturing if you are authorized or if you are considering this particular pattern for this particular value, you can use the same material constantly which has the same sheet resistivity.

Now the key is, when you use the same material, if you want this value with the particular tolerance, you have to worry about the thickness of the print that you are going to generate. Because as we will see the methods of manufacturing resistors, getting the required thickness time and again is going to affect the resistor values.

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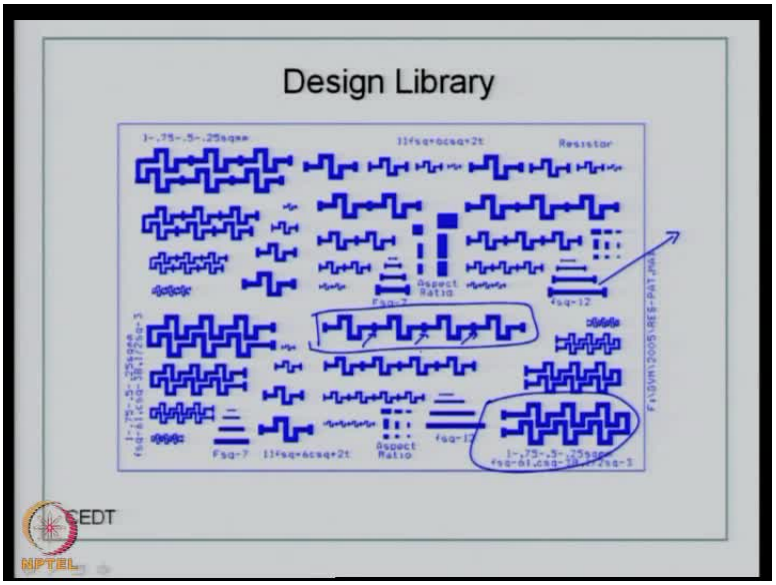

So, this is what I meant, when you can think about having your own design library. For example, this is library of the resistors that in CDT we have generated and because we know what kind of sheet resistivity, resistor material that we are using. For example, we are using carbon paste as one of the resistor materials with known sheet resistivity values and we know the number of squares. Each of these patterns, if you see in this particular illustration, you can pick these patterns quickly and put into your schematic of that particular layer and then define your electrical circuit.

So, again the key is using this pattern is fine, using the sheet resistivity and the same material is fine. But the process, whether it is screen printing or other forms that you will see shortly is a key. You can see from very simple strips to meandering resistors patterns like this and then here you can calculate the number of squares and in between you have the copper so even if there is an error in processing in your bare board testing, these will be shown up.

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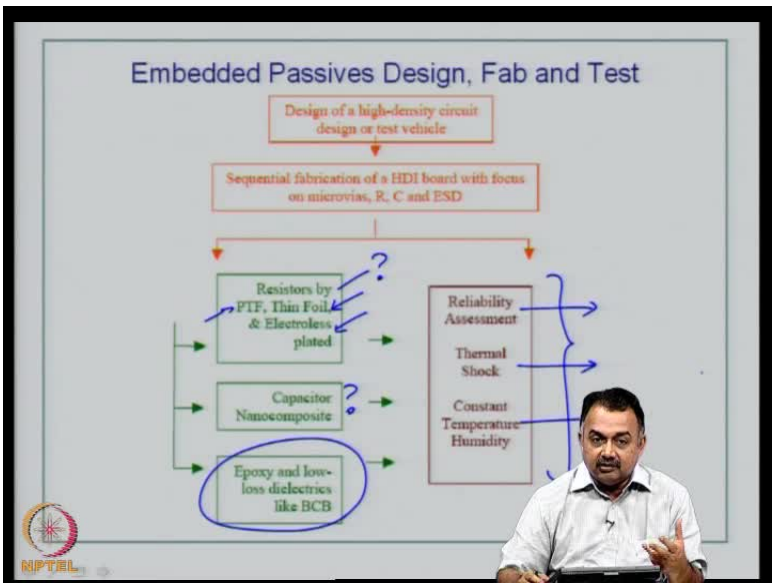

Now, resistors could go as individual inner layers as I told you and here at this point, the N terminals you can consider microvia interconnections that go to the other layers of the board. Generally when you work with the embedded passives, it is very clear that you will be working with high density circuits. So, you have to spend a lot of time on the design of such a high density circuit. Then you have to think about the fabrication methodology, whether it is going to be a conventional methodology or it is going to be a

sequential buildup and you have to look at what are the issues, their microvias, number of microvias, number of capacitor layers, resistor layers, and other electrical issues.

Then, we come to a point when how do you manufacture the resistors. Is it going to be by the three different methods that I am going to talk about today; polymer thick film methodology, a thin foil methodology, or an electroless plating methodology?

Capacitors, how are you going to fabricate and integrate and then can you use different dielectric materials for different layers apart from the core PWB material, which has a different dielectric constant. So, how are you going to integrate all of this to give a reliable board? Obviously as in system level Printed Wiring Board; you have to do reliability assessment, thermal shock test and then constant temperature or varying temperature cycling, humidity cycling to access the performance of your embedded passives that have been integrated.

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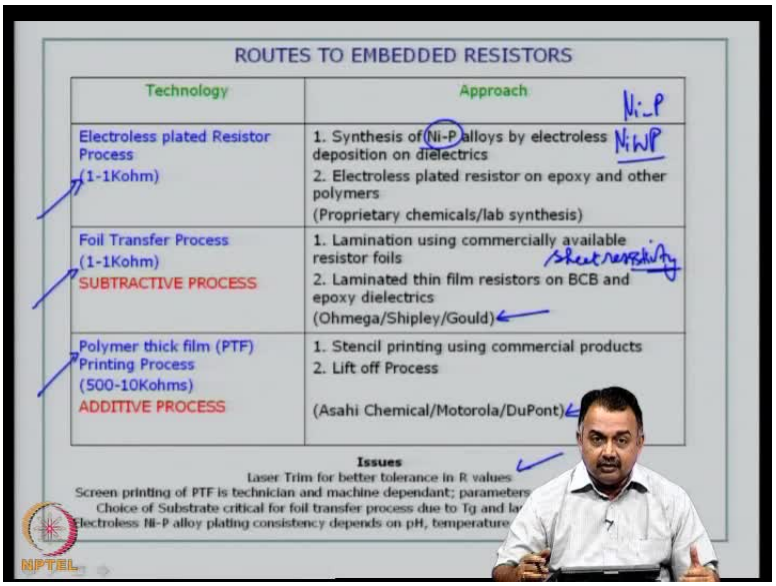

The routes to embedded resistors therefore could be three. I would pick the first one as polymer thick film because it is a very common process to do screen printing. All of you are now aware of this screen printing process or the stencil printing process. You can use that technology to print polymer thick film PTF materials. There are a wide variety of materials available today starting with carbon paste, ruthenium oxides and so on. And depending upon the sheet resistivity that is available for the same set of materials, you

can do screen printing in specified areas of your inner layer Printed Wiring Board, cure it and then test it.

The second one is foil transfer process. Typically it is a subtractive process, because you can get resistor foils readymade synthesized and available as sheets with defined thicknesses of the entire structure and also the individual resistor layer thicknesses from commercial manufacturers and then you can look for specific sheet resistivity that you require in your design so when you do your design, look for this material and then design it.

Then it can be laminated on to your Printed Circuit Board, to any kind of a dielectric it could get laminated. It will be part of the structure and then start removing the unwanted resistor material from the surface so that you can get the required geometry. I have listed here some manufacturers. There could be others too that could make polymer thick film material and the foils.

The last one that I want to highlight here is the electroless plating. I have talked about electroless plating in the PCB manufacturing section where we talked about electroless copper. Here I am going to talk about electroless resistor material plating and typically for electroless resistors, you would be using nickel phosphorous alloys. Nickel phosphorous is the first choice then it could be nickel tungsten phosphorous that could be used and typically this is a kind of an additive process. You are going to add these materials on to the surface of the layer which is part of the Printed Wiring Board and obviously you should have masking because you need to define exactly where this material has to be plated and that will then define the geometry of the electroless plated resistor. So, you can do it in-house if you know the process literature. It gives you methodologies to prepare solutions for electroless nickel phosphorous and nickel tungsten phosphorous and the only thing that you need to worry about the compatibility of the base substrate that you are working with.

There are three processes, three very important processes that could be adapted to your process. Now if you are a designer, interact with manufacturer and really find out which one is suitable for your application from the point of view of resistor value ranges and then what kind of tolerances that you can get from each of these processes. In all of these again, the highlight is getting the right thickness range for a particular resistor value.

There will be issues. First thing is again over plating, over design in terms of tolerances, values and so on, Then you can use laser trimming in some cases just like in your thick film process where you do laser trimming of your material after the firing process is over. Here you can do laser trimming to get better R values. Screen printing if you are choosing, it is dependent on the technician and the process control that you have including the ink, the squeezy, the dispense volume and so on.

So parameters could be a difficult to reproduce but then with the experience it could be possible. Choice of substrate material is crucial because you need to worry about Tg here again and the lamination temperatures especially in the second process you are going to do laminations. So you need to worry about temperature ranges and then electroless plating thickness definition, very important and the quality of deposit consistency depends on various factors just like in alkalis copper. Here you have to worry about pH maintenance of temperature, agitation, catalysis of the surface and so on.

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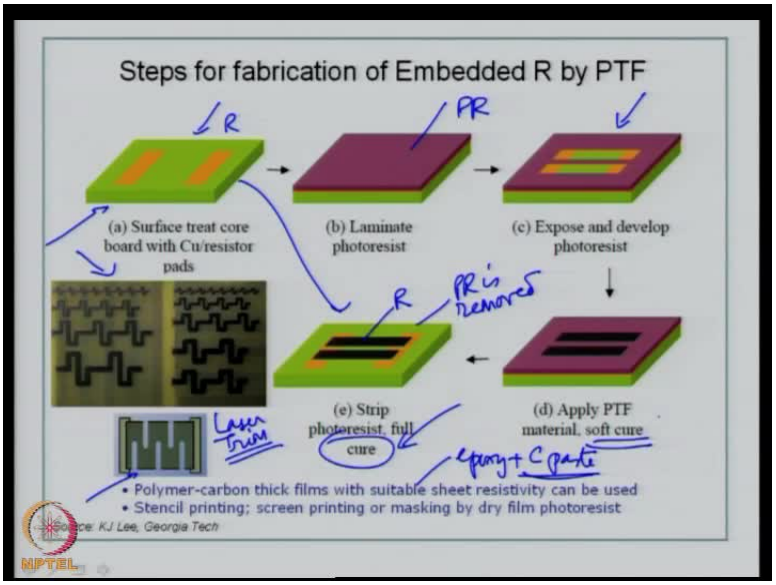

What I am trying to show you here is the illustrative sequence of embedding resistors by polymer thick film. As you can see, this is a simple process compared to the other two because basically you need to surface treat your substrate core or inner layer flux core with the copper pads. Then you can basically what you are seeing here is the copper terminals that have been designed and you need to realize your resistors here, then you can laminate your photo resist material. This is your PR photo resist. Then you expose

and the normal photolithographic process you use a mask and then define the areas so the photo resist material is removed off from the focus area then in this area you are going to do screen printing of the polymer thick film and then you soft cure it.

You can remove the photo resist now because the job of masking is over and then you can strip the photo resist material and then fully cure it. Now you can see that the photo resist is removed, PR is removed here and you can see here on the copper pads, you have the resistor material printed and it is fully cured.

The key here is how well the material will adhere to the copper surface. So, the curing temperatures become very important. This is an example here what I have shown is such a system where a polymer thick film is printed and it is cured. I talked about laser trim. Sometimes it is possible to work on your structures by doing laser trim as shown here; only thing is compatibility of the materials with laser etching.

So polymer dispersed carbon thick films with suitable sheet resistivity is the key requirement. You can do it in your lab; you can synthesize it if you know the base material considerations or these are available in the market today. So the best thing would be for example, to use epoxy as a media and then use for example, your carbon paste. The only consideration is how much material to dispense and how well you mix them so that you get well dispersed media.

So this is a process step that could be attempted for medium dense boards and then here the key would be how well you can control screen printing process.

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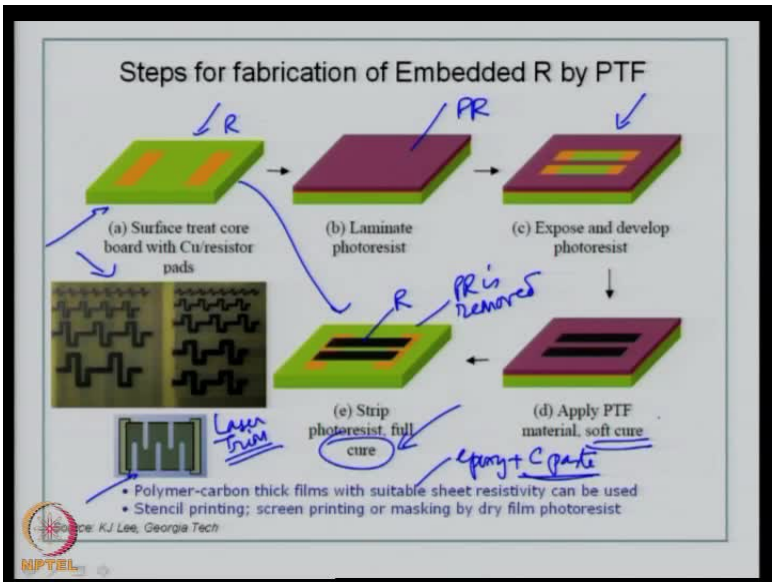

The next step is how to fabricate resistor by the foil method and then the electroless process. If you look at this slide, it gives you the process sequence for fabricating resistor. Now, resistor foils are available from a few manufacturers. For example, in this particular work, the material used is from Gold electronics as I mentioned in a couple of slides before there are other manufacturers also.

Look at these specifications that suit your integration process; so you could get foils in 25 ohms per square 50 and 1 k thousand ohms per square and so on. You could have multiple fabrication steps if you require more than one different R material, resistor material for a particular design. It is going to be complex but then you could either do it in separate layers or in the same layer. The only thing is you will have to do different masking and photolithography steps. One of the materials that is used for foil is nickel chromium, very common. The other one is nickel chromium aluminum silica for which this particular slide is based upon. You can see here on an FR4 nickel chromium aluminum silica resistor foil is laminated and you can see the black layer that is sandwiched between the top copper and the bottom green FR4 material. From the manufacturer, you will get this foil where the resistor is actually bound to the copper foil. Now you do a lamination using photo resist, then expose and develop so you are defining certain areas now.

Now you are removing a part of the copper plus resistor away from the FR4. So, the first etch process removes both copper and the resist material. Use a suitable etchant for that. The etchant that will remove both copper and the resistor material is nichrome or nickel chromium aluminum silica.

Then the next thing would be to remove the photo resist which protected this area, where you are going to define the resist. Now we have created the pattern here as you can see then after that you remove the copper from this base only copper not the resistor.

So the second etch process will remove copper only, so the key here is the second etchant should not react with the resistor material, this is the R material. Now, you have defined the length and the width of the resistor by double step etching process. So, the key here in this is, it is very similar to your PWB, Print end etch methodology.

The key is how well you utilize the two etchants to define your length and width of the resistor and finally you can strip the photo resist and you will get an R defined. The same thing goes with electroless process. Here if you want to do electroless process, again you can open up those areas using photolithography and then add by additive process. As you recall in the additive electroless process, you have to do palladium plating. You can do the same process here and then add electroless nickel phosphorous or electroless nickel tungsten phosphorous. Tungsten is usually added to increase the mechanical strength of a deposit.

Copper thickness in usually about 18 microns, resistor foil thickness is usually 1 to 2 microns, so when you do electroless plating also, you need to worry about this range of thickness.

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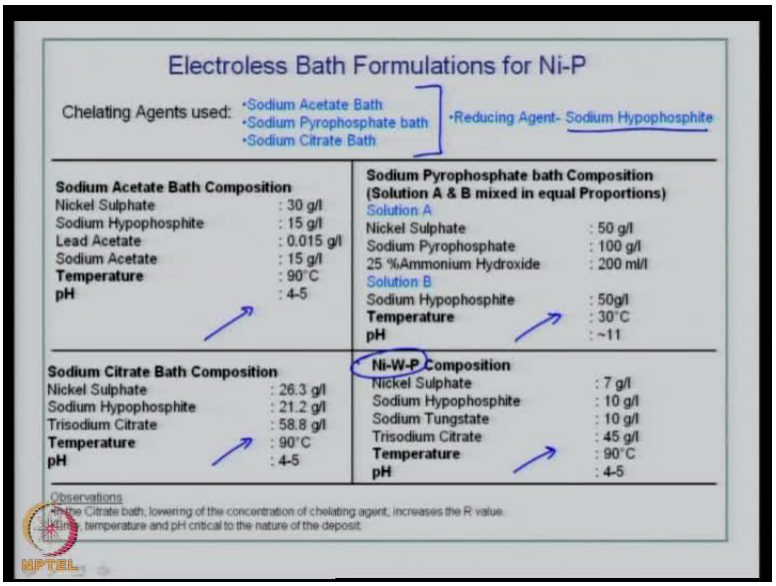

So the electroless bath formulations for nickel phosphorous are available from the literature. You can go through that, but the gist of the entire summary here is that the reducing agent is sodium hypophosphite. There are three different baths available for nickel phosphorous and all of those who are interested in the details of creating or synthesizing your own bath, you can find these compositions here, this is for nickel tungsten phosphorous and you have to do a careful control of these electroless bath solutions to get the required thickness.

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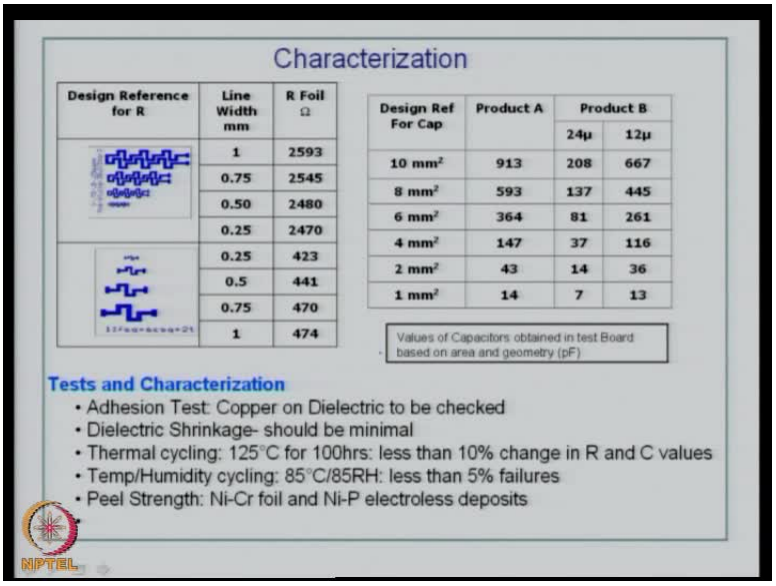

Now as usual you have to characterize in a thing that is synthesized. So, once it is fabricated you have to do the characterization. In the next lecture, we will talk about characterization issues, challenges and will also get into fabricating capacitors and how do you evaluate resistors and capacitors and qualify them as reliable materials.