An Introduction to Electronics Systems Packaging

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Module No. # 06

Lecture No. # 30

Microvia Technology and Sequential Build-Up Technology Process Flow for High-Density Interconnects

We will continue with this module on printed wiring board technologies, which also encompasses high density interconnect process issues.

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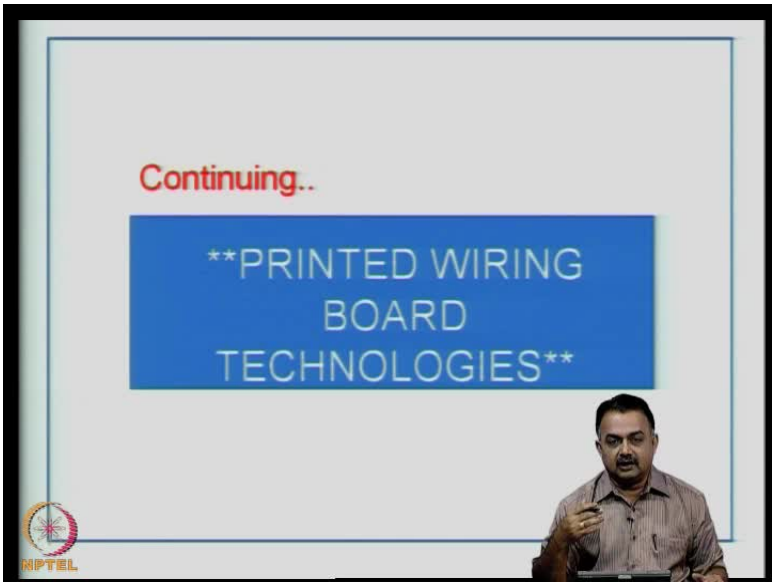

We will continue with this module on printed wiring board technologies, which also encompasses high density interconnect process issues. As I mentioned time and again for advanced packages to be mounted on let us say – an organic substrate or a ceramic substrate, you need to understand the I/Os. If there are going to be large number of I/O's and if they are going to be mounted on an organic substrate, then the substrate has to be compatible with the package and the package design that you have. Therefore, you are now trying to understand the technologies that enable us to build a substrate, that is compatible, that can sustain, that can provide electrical performance, and also sustain the

reliability issues that we are talking about. Therefore, you should have good thermo mechanical reliability. Thermo mechanical reliability is not just applicable to the chip level packaging, it is also very much applicable to board level packaging issues.

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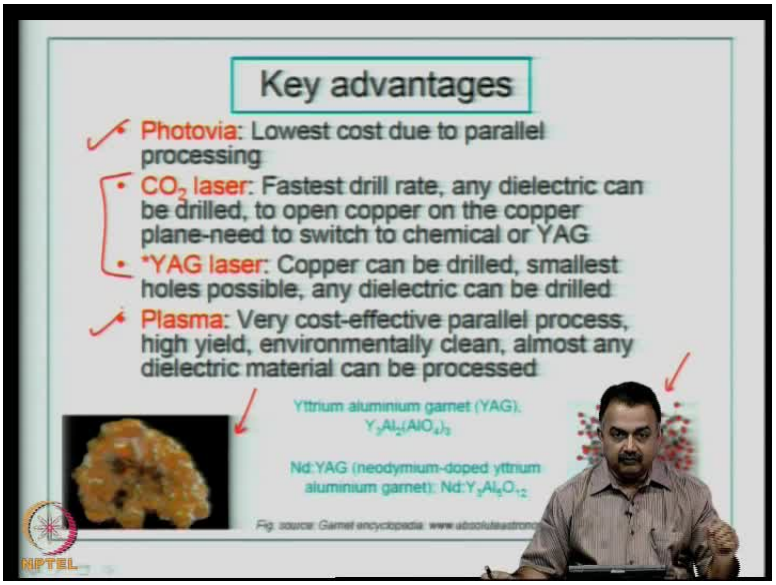

In the last class, we have been discussing the interconnect hole formation methods. We will continue with that. If you recollect, we have seen the various methods to drill a via or a Microvia. It can be a mechanical drill. We have seen the mechanical drill limitations. If you recollect, the limitations today in terms of the equipment is something like 150 microns, but there are a few equipments in the market today, which can drill 0.125 mm, which is 125 microns. They can be expensive and it is not only that – if you use those kind of mechanical drills, the next issue to consider is that how well you can wet the barrel – hole barrel and the inside of the dielectric hole to make it conductive. So, your chemistries and the technologies needed to plate the through hole, or it can be a blind via, or it can be a buried via. Nevertheless, as the size decreases and if you are going to depend on a larger aspect ratio, then you will have difficulties in electroless plating.

Therefore, the alternate methods like the photovia technology, which uses a very thin dielectric and you are trying to use only that thin layer typically about 15 to 35 microns of the dielectric material, which needs to be opened up by photolithographic methods, which we have seen earlier. The via has to be electroless plated and further electroplated

to create a Microvia structure. Here, the aspect ratio is comfortable to work with. Therefore, you have much better yield in a photovia, but further to that, we have seen over the last seven to eight years that – the laser drilling has picked up very fast; the equipments have been affordable; companies have invested in the capital of the company to have laser machines to improve the yield and the throughput.

In the laser drilling method, we have two types: one is the carbon dioxide laser and the other is the chemical laser, which is basically YAG (Yttrium Aluminum Garnet). You have modifications of YAG like the neodymium doped yttrium aluminum garnate (Refer Slide Time: 04:18). As you can see here at the bottom, you see the structure of the garnet material and this is also the atomic arrangement in the crystal of a garnet. Therefore, on one hand you have the photovia, which is a very good option.

There are two options in laser, which are being practiced for large volume production – one is the carbon dioxide laser and the other one is the YAG laser. The only thing is, photovia is lowest in terms of cost due to parallel processing, which means you have a mask, you have a substrate that is well prepared, you have a photo resist material that is applied on to the surface, and then using simple UV lithography, you can transfer the image on the entire panel. So, compared to a mechanical drill, or in some ways, the comparison to the laser drilling, the photovia is economical because of its parallel processing, but we are looking at in terms of holed reliability and the dimensions of the hole that you can generate using a photo via as compared to a laser drill.

Carbon dioxide laser will drill fairly fast; it has a good drill rate; any dielectric can be drilled. So, you have flexibility here to choose various types of substrates and thinner dielectrics in the sequential build up layers to create microvias. However, using carbon dioxide laser, you cannot open copper because if you look at buried vias where include copper, the carbon dioxide laser will not be able to drill on the copper layers. Therefore, you need to switch during that time to chemical or YAG.

With YAG laser – yttrium aluminum garnet, you can drill copper, you can drill small holes, fairly small holes, and any dielectric can be drilled. Typically, today, in the industry and even in the research papers and prototyping activities in this S B U methodology, we have seen that laser drilling has gone even up to 50 microns. Therefore, during the last seven to eight years, we have seen extensive development in the use of

new dielectric materials and the compatible nature of laser drilling with those dielectric materials. Then, we have plasma drilling. It is a very cost effective parallel process similar to the photovia process. It has got high yield and environmentally it is very clean because you have a special chamber for it where you create the plasma and almost any dielectric material can be processed. Therefore, cost wise if you compare plasma with photovia, photovia will be less expensive, but plasma still is not a preferred industrial choice for microvia drilling.

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Now, what I would like to show here is a sample of a laser drilling process. You can see here that there is a substrate, typically an organic substrate mounted on a laser drilling machine. Now, the data for this drilling process is taken from your cadwork. So, it can be an inner layer drilling typically to create microvias, or it can be a top or bottom layer after the sequential process has been completed to create the microvia structures.

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You can see here that typically, the copper is drilled, and then you can see the cross section here the dielectric is opened up, and finally, you end up at the base copper. Essentially, you can do what is known as a depth drilling. (Refer Slide Time: 08:59) You can see once again that if we use YAG laser, you can combine both copper as well as dielectric drilling to a definite depth. Now, these kind of depth drilling is required if you want to create blind vias in a structure that you have built up from a core substrate. For example, if you have created a 4 layer core, and then you want to build a 2 layer at the top and a 2 layer at the bottom to create a 8 layer sequential built-up technology, then these kind of controlled depth drilling to create microvias for your signal lines interconnects are very useful.

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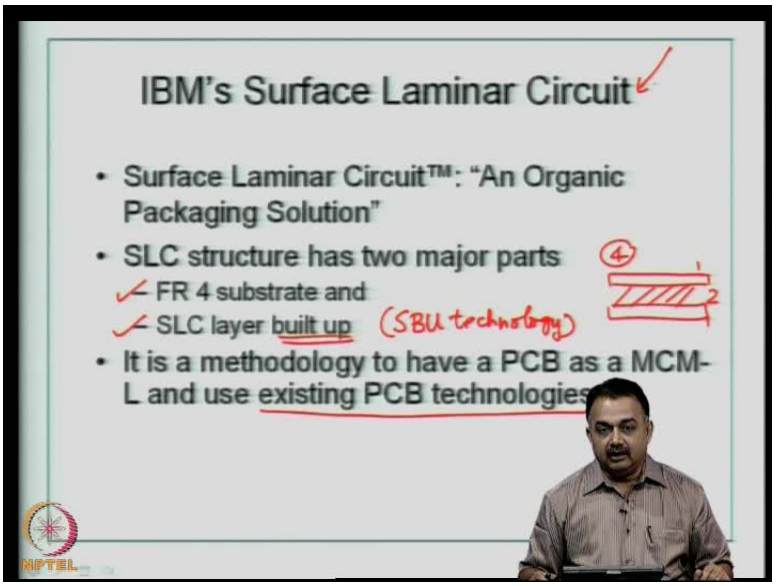

Now, we will come to some of the classic examples that we have witnessed in the last ten years for creating high density interconnects. All of you are aware that we have a single sided board, a double sided board, and a multilayer board built by conventional techniques. Now, that really does not give a high density board, a high density organic substrate. In those cases, you are typically using for example, an FR 4 core and a similar material is used as the prepreg material for building the inner layers. Finally, your both thickness comes to around 1.6 mm or maximum 3.2 mm.

You may have multi layers, but your interconnections are still dependent on the through holes, which are fairly large. In order to improve the density on the printed wiring board and in order to qualify the substrates for advanced packages, IBM introduced this technology called Surface Laminar Circuit at that time around the year 1997/1998. This technology was introduced and termed as SLC, Surface Laminar Circuit. It is a trade mark belonging to the IBM organization. So, it is basically a pure organic packaging solution.

Now, SLC – what does it contain? It has two major parts: one is an FR 4 substrate and the other is the built-up layer. That is why it came to be known as Sequential Built Up technology or SBU technology. So, you will start with a core. For example, this is a core (Refer Slide Time: 11:45); let us say a 2 layer core and then you build an additional layer at the top and additional layer at the bottom to create a 4 layer structure, but built by

nonconventional method using thin dielectrics at the top and the bottom, and opening microvias and interconnecting these pads and tracks to the inner structure by very small microvias of the order of 4 mills and so on.

Essentially, in this technology, you are describing a new method to create an SLC layer. It is also a method to have a printed wiring board or printed circuit board as MCML structure using existing PCB technologies. The advantage of using an SLC method in those days when it was introduced was the attractive concept that you do not have to change major of your printed wiring board process line. A couple of changes in terms of imaging and a couple of new materials like the dielectric that you would like to use specifically to get very thin coatings is all that was required to convert or improve the density part of it or high performance qualification of a PCB to what is known as a Multi-Chip Module L-type substrate. If you recollect, we have discussed what an MCML is. Typically, it is an organic substrate and you can create an MCML using thin dielectrics.

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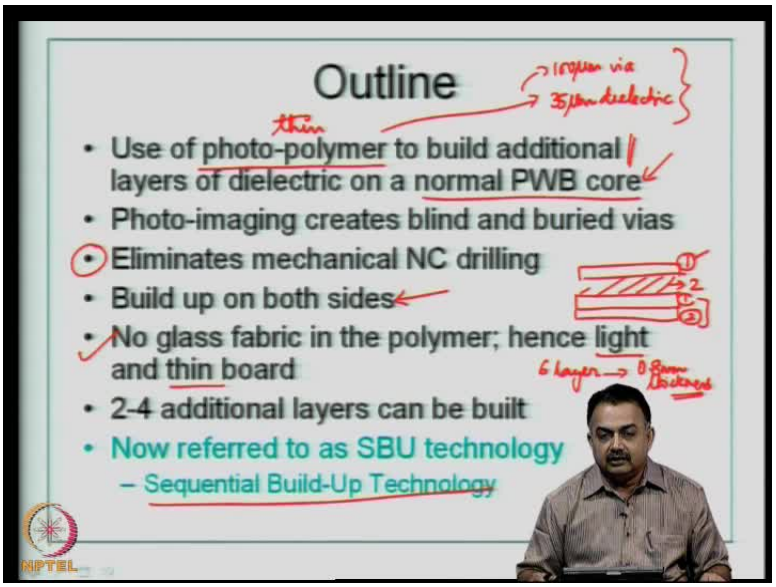

The outline of this SLC process is that it uses a photo polymer to build additional layers. That is the first key point here to build additional layers. That means you have a normal PWB core that is already available in your design. Essentially, you will now try to design the additional layers by not using a prepreg, but using very thin photo polymer layers. This has to be a very thin layer so that your aspect ratio is high at the same time you can

handle them. For example, in this particular case, we are talking about a 35 micron thick dielectric material on which you can very comfortably open up a 100 micron via structure.

You can easily plate the hundred micron via to establish connection from the top layer to the immediate adjacent layer. The uniqueness of this is that you are not creating larger depths of microvias, the opening is only on the thin dielectric and it connects to the immediate bottom copper plane. Therefore, the reliability is very high. Photo imaging creates blind and buried vias; it eliminates mechanical drilling. So, this is a very important key point that made this process successful; otherwise, you have to depend on the limitations of the lowest drill bit that your NC drilling machine can work with and still depend on cleaning the via that has been mechanically drilled to clear the debris and so on, and make it conducive for electroless plating.

The buildup can be done on both sides. This is another attractive feature. (Refer Slide Time: 15:30) As I said earlier, if we have a core substrate, you can do the buildup on one side or even on the other side. The buildup can be uneven, which means you can have one buildup here and then you can have 2 layers built up on the second side, which means if you start with the 2 layer core, you can end up with a 2, 3, 4, 6 layer structure, but at the same time, you can see a 5 layer structure – one at the top, two at the bottom, and two at the core. So, it is a 5 layer printed wiring board built by SBU technology or built-up technology. Unlike in the conventional case, design wise to avoid warpage and so on; you try to make it an even structure. If you build 2 layers at the top, you also build 2 layers at the bottom, but in this case this is not necessary because we are talking about thin structures and you would not see the effect of warpage in these cases.

No glass fabric in the polymer. If you compare with the prepreg material, there is a filler material along with the resin. For example, in FR 4, you have a glass fabric along with the epoxy resin in the prepreg material. Therefore, it is more rigid, you cannot reduce the thickness, and typically you can work with 200 microns to start with. Hence, because of this, the entire structure is light and thin.

(Refer Slide Time: 17:08) Typically, even if you build a 6 layer board, you are saying SBU technology; you can still end up with 0.8 mm, total thickness of the board, which is an indicator of the high density that you can achieve. You can build two to four

additional layers from your core. (Refer Slide Time: 17:29) This is known as Sequential Build-Up Technology.

There are various methods, various roots that many companies have tried from this original SLC technology. So, I would say that the Surface Laminar Circuit technology was a key driver for this industry to enter into high density interconnect structures, which enabled usage of these printed wiring boards for various handheld products like your digital camera, your camcorder, and then PDAs; all handheld products including the current iPad, mini computers, and so on have tried to utilize SBU technology in their systems.

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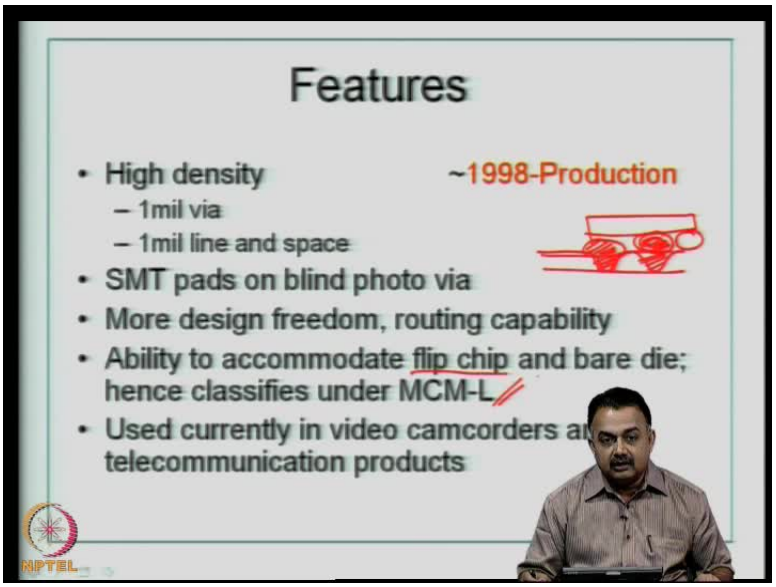

The features of this SLC technology is that it is high dense. At that point of time during 1998, when it went to production and it was targeted for the year 2000, when the product can be gone full fledged into the industry; especially in Japan, 1 mil vias were used that was the target and 1 mil line and space. So, this is a very great deviation from the conventional multilayer boards that we have been used to.

SMT pads can be placed on blind photo vias on the top surface and the bottom surface. That means you are avoiding additional pad area that needs to be provided for surface mount devices. So, you can use the photo via land itself as a pad. For example, if you have a thin dielectric and if you are opening about via here, (Refer Slide Time: 19:21) and you are plating this via, then your surface mount device; one of the pads can sit on

this microvia. Similarly, if you have another via here, the other pin can sit here and so on. So, this is the package. So, you are gaining a double advantage in the sense that your via becomes secure, which means you can fill this via with a metal paste, or you can plate it additionally to provide rigidity to your microvia, and then also, you can mount your component on the via so that it becomes a via on pad type of structure. It reduces the board area, increases the density. More design freedom because of usage of microvias, routing capability is very high and you provide additional layers for fanning out your microvias to inner layers. Ability to accommodate flip chip or a C4 technology and bare die; hence, classifies under MCML. Used currently in video camcorders and handheld products, telecommunication products, and so on.

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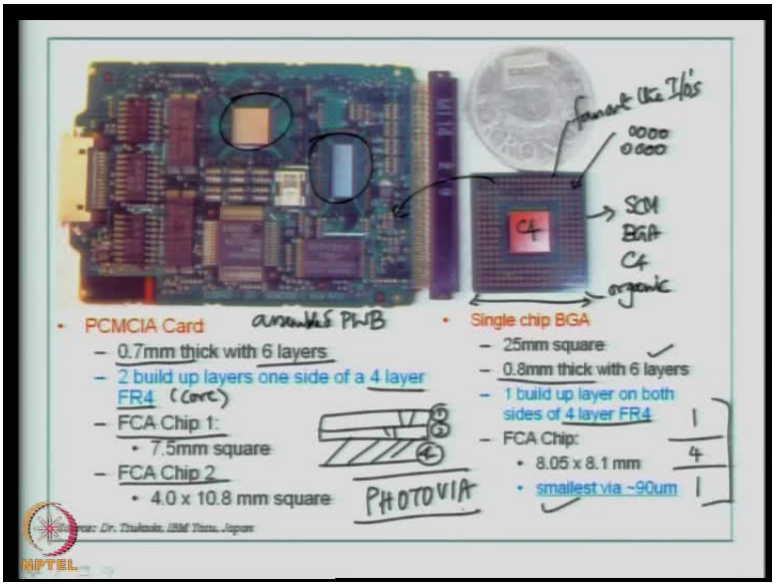

This is a picture of the original, the first product that came out using IBMs Surface Laminar Circuit. These two were introduced by IBMs Dr. Tsukada, working from IBM Yasu in Japan. You can see that in the left, there is a PCMCIA card. It is a LAN adapter card, where you can see typical numbers. For example, the thickness of the board is only 0.7 mm. It has got 6 layers. So, 0.7 mm, and then having 6 layers is not possible via the conventional multilayered board methodology because the limitations are two: one is the prepreg thickness, the copper foil thickness that you normally get in the market, and third is the mechanical drill via size structures.

In this particular example, 6 layer board, there is a 4 layer FR4 core that has been taken and 2 build up layers have been created on one side of a 4 layer board. So, it is typically a design issue. It has been decided to have a 4 layer structure here (Refer Slide Time: 22:04), and then 2 layers have been built on one side so the other side did not have the Sequential Build-Up methodology at all. So, these were provided with a lot of microvia structures to interconnect to the core substrate.

You can see here (Refer Slide Time: 22:25), it has accommodated flip chip: one, which is 7.5 mm square and the other is flip chip 2, which is 4.0 by 10.8 mm square. So, these are the flip chip substrates that have been mounted. You can see that this is a classic example; an introduction from IBM about the usage of the bare die directly on to the substrates. There is no packaging, it is a bare die flip chip methodology and it is a reliable interconnect. In addition, you can see that all the components are surface mount including the resistors and capacitors. Absolutely, it has eliminated mechanical drilling except in the core structure, and then no through-hole components have been used. So, this is how the progression has taken place from conventional multilayer boards, where the limitations have been there for high performance because of the size.

Now, we have the microvia showing us how we can generate by proper design methodologies…; understanding manufacturing, you can create a high dense microvia board. Now, this is actually (Refer Slide Time: 23:45) an assembled printed circuit board containing the microvias. What you see here is a single chip module BGA component containing a C4 device. You can see here, this is the C4 flip chip, then you can see this is an organic substrate, and then it has got a BGA interconnect; the solder balls are visible. This is the top side.

On the other side, pertaining to these pads (Refer Slide Time: 24:17), you will see the matrix of the solder balls. The features of this single chip BGA is that it is a 25 mm square package. This can be mounted on to any printed wiring board if you provide the right registration LANs. It is only 0.8 mm thick with 6 layers. In this case, it is a 4 layer FR4 that has been started to work with, and then 1 build up layer on both sides. So, it is 1 4 1 (Refer Slide Time: 24:53). This is the type of arrangement that we see in this particular single chip module for creating a 6 layer substrate.

In this particular case of single chip module, BGA, as I mentioned in the packages chapter, the job of the substrate or the function of the substrate here is basically to just fanout (Refer Slide Time: 25:04). Fanout the I/O's through the organic substrate into the BGA balls at the other side of the package. The flip chip size here is almost 8 by 8 square and the smallest via used here at that time is around 90 microns, which is a very remarkable achievement considering that this was the introduction or the beginning of these kind of concepts.

Today, using laser drilling and… By the way (Refer Slide Time: 25:45) this process used photovia method, but today people are using laser drilling to achieve 60 micron or even 50 micron drills.

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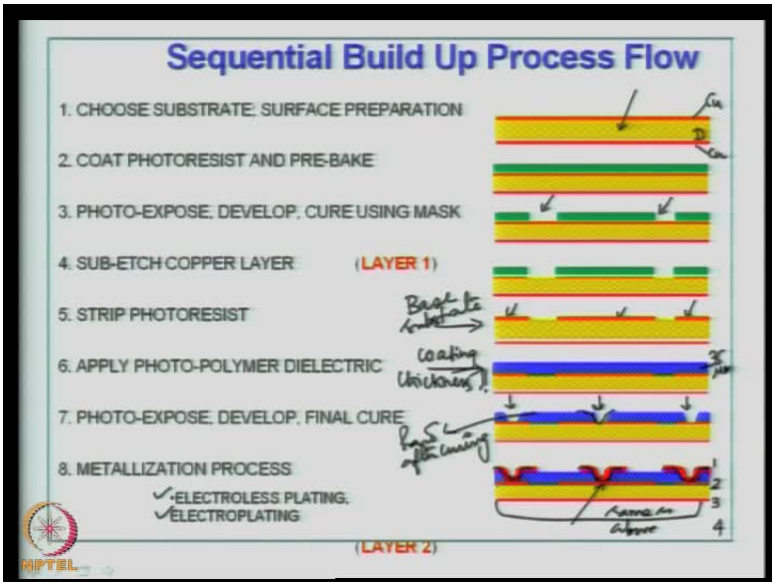

What is this SBU process flow? How does it go about? Now, if you look at this figure on the right and you can look at the explanation on the left, you will be able to understand how a microvia is generated and how you make it conductive.

Now, let us look at the top. Here is a substrate, which there is copper on a top side and there is copper on the bottom also. Then, this is a dielectric material; this is the starting. Now, you do the surface preparation as you know. Coat the photoresist; the green one here what you see is the photoresist, and then prebake it. Then, you photo expose, develop using the mask; the mask here should contain the photovia elements.

You can see here (Refer Slide Time: 26:54); this pertains to the openings, where the photovias need to be formed. What is next? You now create the pattern. In this particular case, you are now doing the etch process and then you can see here at this point of time that base substrate imaging has been formed. This (Refer Slide Time: 27:26) is the circuitry; these areas are the circuitry. So, a particular layer imaging process has been completed. All of you are aware of this entire process; we have seen this using video highlights.

Now, begins the SBU process technology. If you can carefully look at the bottom three figures, apply the photo polymer dielectric here (Refer Slide Time: 27:53). Now, how do you apply this photo polymer dielectric? You can use typically curtain coating, or you can use spin coating. So, the performance of this process whether it is spin coating or curtain coating, to achieve a desired thickness; here, thickness is very crucial; thickness is very important.

Assume you have got about 35 microns. Now, you take the mask that is required for the microvia (Refer Slide Time: 28:28) and place it on top of the cured dielectric material. This dielectric material can in fact be a better dielectric in terms of dielectric constant compared to your host core substrate. Once this is cured – after the microvias have been opened, it is cured. Now, it becomes very hard. So, this particular layer (Refer Slide Time: 28:55) becomes very hard after curing. Now, you have to metalize this microvia. You can see that the hole walls are not conductive. So, you do an electroless process followed by electroplating process, and then you can see all of these layers have been coated with copper. You can see electroless first, followed by a flash electroplating to metalize the hole wall. In addition, you can see that the hole wall copper at the bottom touches the copper plane in the adjacent layer. So, this is how a connection has been established between this layer and this layer (Refer Slide Time: 29:41). Then you have the third layer here. You can build another additional layer as we have seen here same as above, and then you get the forth layer.

Now, you can repeat this process once again to get 2 additional layers: one at the top and one at the bottom. That will give you a 6 layer board. After the plating has been done, you can image it according to your circuit design. So, this is a very convenient process, where you can inspect the process at every stage, whereas in multilayer board, once the inner layers are done and if you have combined them in a press, it is very difficult if you

have a registration problem or if you have a plating problem in the large mechanically drilled through hole, then you cannot repair the board at all; you have to discard the board. Here, at every stage, you can inspect, you can rework on the layer, and build the additional layers. So, it is an excellent process, which was used in the SLC method. People in the industry have modified these processes by using various dielectrics and currently, made it compatible with the laser drilling process. So, this is the SBU process. As a result of this SBU process, what kind of structures can you get?

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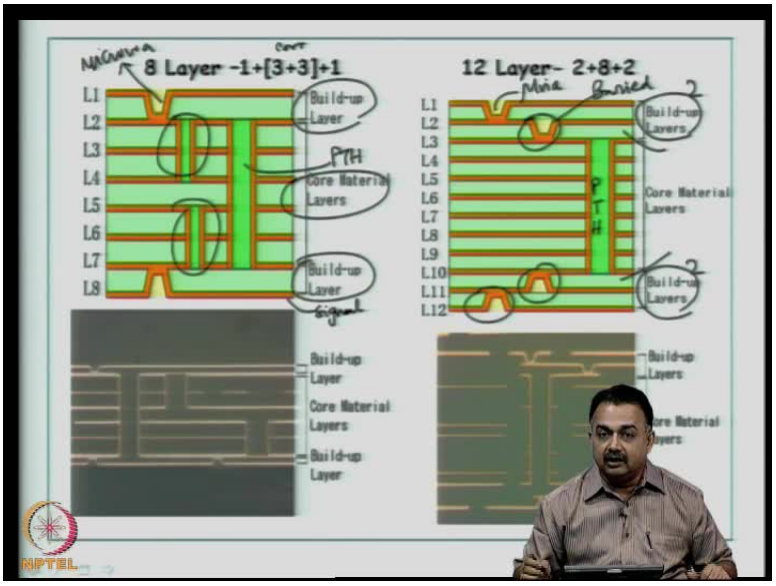

Suppose if you want an 8 layer board, and then you have a core layer, for example, you can see here in this particular figure, this is an 8 layer board; has been described. The build up layer is here and another build up layer is here. This build up layer contains the microvias, whereas here, these are through hole structures done by mechanical drilling. This is a PTH – Plated Through Hole. Therefore, this is the core. Typically, this is the core – 6 layer core and then 2 build up layers have been done on this core structure to give you a 8 layer board. Ideally, you place your ground planes in the core layer and typically in the build up layer, you have all the signal lines thin structures. So, ideally you do not want to have too much copper on the build up layers. So, you will have thin structures typically 4 to 8 mills in width and spacings are also typically 4 to 8 mills. Those layers – top and bottom will be used for accommodating or mounting your surface mount devices or advance packages like your BGA flip chip, CSP and so on.

The next one is a 12 layer board. You can see here (Refer Slide Time: 32:39), the top one is a build up layer, which means 2 layers have been built at the bottom and 2 layers have been built at the top. So, 4 layers for the structure have been done by build-up technology. You can see this is the microvia (Refer Slide Time: 32:56) and this is a buried microvia. Similarly, here we have the microvias. You can have various microvias in this particular layer interconnecting or connecting to your inner layers. This is a plated through hole (Refer Slide Time: 33:17) structure done by mechanical drill. So, this is how you build or increase the density of your board from a simple 8 layer core. Lot of packaging has been done in these 4 layers. So, that is the key to it.

You can inspect once this layer (Refer Slide Time: 33:37) is completed and this layer is completed. Again, if you want to rework, you can remove the dielectric and redo the imaging process. So, that is the advantage of using a build-up technology. This is the cross section of the same process – you can see inner layers containing through hole, buried through hole structures, and the top layer containing the microvia structures. This is the cross section.

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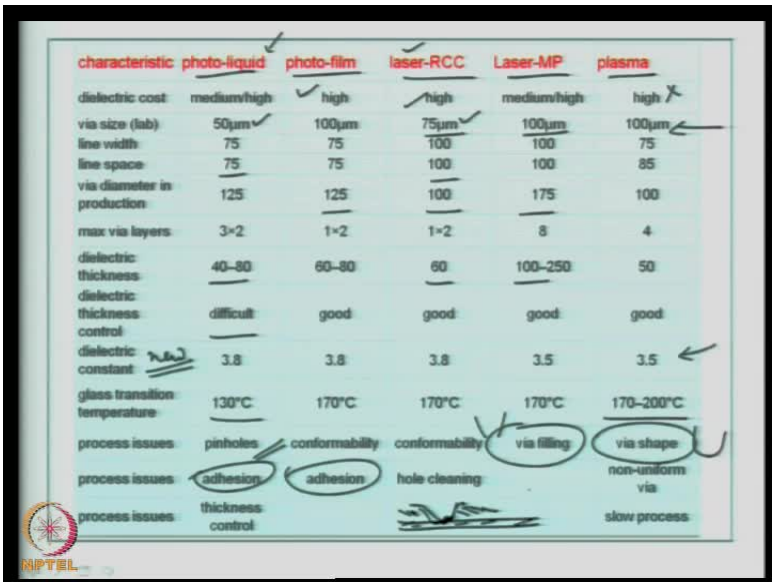

Now, we will look at a review or a summary of the highlights of the key properties of these materials. The materials in consideration here are the photo-liquid imaging system, photo-dry film imaging system, laser drilling in conjunction with resin coated copper foil, and then you have the laser and the plasma drilling.

Now, if you look at the various parameters, you have these materials in consideration today. If you look at the dielectric cost, the photo-film; dry film is very difficult to be made available. Today, the availability is low, cost is also very high, whereas a liquid is easy to work with. You can work with various coating methods like your meniscus coating, or your curtain coating, or the spin coating method.

The resin coated copper foil, that is readily available and compatible with the laser drilling, the cost is fairly high. Then, plasma because it is also fairly a parallel process, but again depending on the thickness of the material that needs to be edged, it can be time consuming. Therefore, manufacturing wise it is a costly process.

For medium numbers, industry also prefers to use a liquid for the polymer. If certain industries are still believing or making sure that their feature sizes are easy to work with using liquid photo polymers, but where there is a more stringent regulations in terms of tolerances and lower feature sizes that are required by certain customers, then people have to prefer laser drilling.

Now, have a look at the via sizes that are possible. Typically, liquid photo polymer – you can work from 50 microns. Current-day technologies for laser also targets 50 microns, but very safe is 75 to 100. So, typically, the range from 50 to 100 should be possible for various methodologies listed here to create a microvia. As I said by definition, a microvia is one which falls in the range of less than 125 microns; around that number because otherwise, it can be done by a mechanical drill and does not classify as a microvia. The line width and space is typically (Refer Slide Time: 37:14) 75 to 100 microns for all these processes. Then, you have the via diameter in production, which is currently about 100 to 125; in some cases, even more - 150 microns or so; so that the high reliability is maintained, whereas for prototyping, one can go for these kind of numbers.

The via layers maximum is 4 additional layers, but in some cases, people have gone in for 6 layers. Typically, if you start with a 4 layer board, you can build 2 to 3 additional layers. Dielectric thickness varies from (Refer Slide Time: 37:57) 40 microns to 60 microns and in some cases, it has even gone up to 100 microns to 250 microns.

Dielectric thickness control, which is a very key parameter for the technicians to maintain and then understand the working of the equipment; with the liquids it is going

to be very difficult, but if you get a readily available substrates like your resin coated copper foil along with the dielectric material because there are some companies which have provided standard thicknesses of dielectric coated with the copper. In those cases, thickness control is not an issue; it is only the drilling depth that is an issue.

Dielectric constant from around 3.5 to 3.8. Now, the key to your electrical performance when you use an SBU methodology is to experiment with new dielectric materials that are low dielectric constants and that has probably available as a liquid, that can be coated using curtain coating. So, the key here is try out new dielectric materials with lower dielectric constants.

Glass transition temperature of your core substrate that can vary from 125 C or 130 C to about 190 today, can be used. We are also worried about the glass transition temperature of your dielectric material. In some cases, you may use a dielectric material with some filler content in that, but in most cases, it will be a filler free dielectric material that you will use for the inner layers.

Process issues are - working in a clean room. Therefore, things like the pinhole, debris sitting on the liquid, photo polymer with no protection, and so on, can be very destructive in terms of the yield part of it because of lot of rejects; because the size of the via itself we are talking about 75 to 100 micron - therefore, your pinholes represent a significant defect.

You have to look at the conformability of your drilling process especially, the laser with the dielectric material. Also, we are talking about the process issues in terms of the PWB processing because it goes through the various chemicals and then the substrate compatibility. In some cases you may want to use a via filling (Refer Slide Time: 40:39) as I said because you want to mount an SMD component on top of the via. Therefore, what type of filling you will do for a microvia filling. The shape of the via in the case of a plasma seems to be well in tune with the desired results, whereas in the case of laser, we could end up with a plateau like this (Refer Slide Time: 41:02), whereas in a plasma you might get an almost cylindrical shape. How do these vias behave during thermal cycling and during the life of the product?

As some of the key issues that designers as well as the manufacturers will be interested in. The other key process issue that all of us have to be aware of is the adhesion. What is

the adhesion we are talking about? We are talking about a dielectric material that is coated (Refer Slide Time: 41:32) and on which a via is formed. So, we are talking about the plating of the via and there is a dielectric material here. We are talking about the adhesion at the surface of the dielectric to the copper. Now, if there is delamination of copper from the dielectric material, then your microvia has failed. So, the key to getting high yield and sustaining during the thermal cycling and the natural life of the product is that these microvias should be defect free during its operation. The plating that happens and the electroless copper to dielectric adhesion is also a very key issue. If you are doing laser drilling again because it is an ablative process, you have to make sure that you clean the hole walls fairly well just like in your conventional MLB process before your electroless plating. So, thickness control, adhesion, and being defect free are some of the key issues that one has to be aware of.

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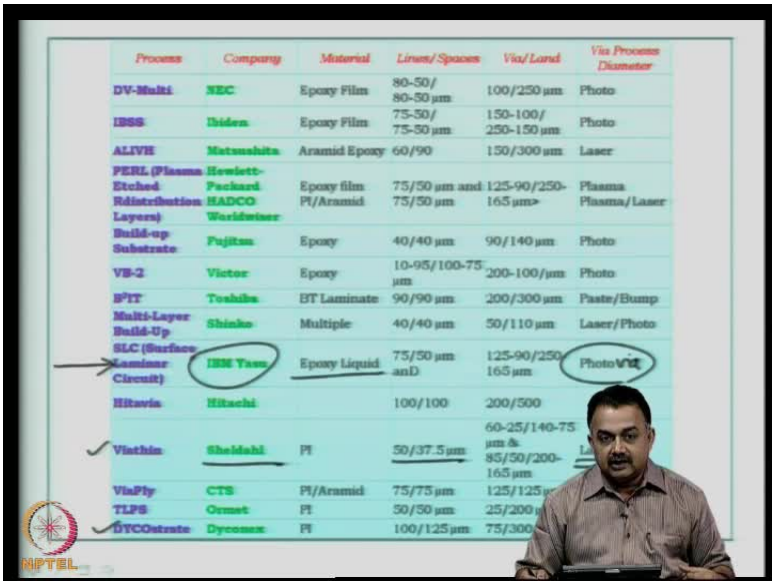

Now, here is a list of companies, which has been picked from various sources. This information, which have… If you look at this, this is probably the starting point - the SLC (Surface Laminar Circuit), which uses epoxy liquid from IBM Yasu. This is a photovia process. Then, came up various processes from different companies like Fujitsu, Toshiba, Hitachi, Sheldahl; Sheldahl came up with a readily available substrate that can be used for laser drilling. So, you do not have to worry about thickness control of the materials. You can see that lines and spaces like 50 to 37.5 microns have been well defined.

DYCOstrate (Refer Slide Time: 43:35) is another major company that came up with photo imagible dielectric material, which information is more confined with the company because it is a patented process called diaconic substrate, where you can see the feature sizes like lines and spacing 100 to 120, via/land 75 to 300 micron, and you see a plasma compatible dielectric material. So, depending on whether you want to use a photovia or a laser drilling or a plasma process, you can adapt the kind of materials that are available.

We are going to talk about one or two of these in this particular chapter just as a case study because if you want to describe all of these, it is going to take too much of time. Therefore, as a typical case study or an example, we will describe a couple of these processes and you can see that from the original SLC methodology, how people have modified this technology yet maintained in the SBU concept, and then built high density interconnect structures.

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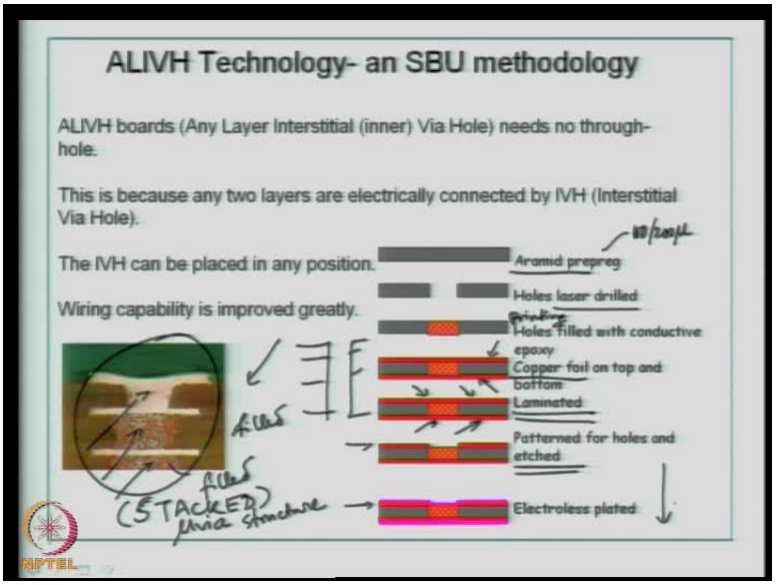

The first one that we will describe or look at is the ALIVH technology. It is an SBU methodology. ALIVH stands for Any Layer Inner or interstitial Via Hole, which requires no through-hole technology at all. So, again just as the SLC, this is an encouraging concept, which says you do not have to have a mechanically drilled hole at all in your 4 layer or 6 layer or 8 layer structure. These technologies are not for building a 60 layer board like you normally do in a ceramic board, or let us say a 24 layer board in an

organic substrate. These are for substrates that are typically used for handheld products, not generally used for your desktop, computing motherboard. There you still depend on the existing technologies because it is reliable and well documented. As I said, these are for simple computing boards that uses a DSP processing, which is requiring; let us say – sip package or a CSP package or a BGA package or an FPGA module; let us say – which is being used and so on; fairly small sized boards, which can be built entirely using an SBU method.

Now, why does this technology require no through-hole? This is because, any 2 layers are electrically connected by Interstitial Via Hole; that means you can place the vias wherever you want in your design. So, it requires your ingenuity in the CAD system to fanout your I/O's from the packages very comfortably using small microvia structures. To remove the heat, you can use them as thermal pads or thermal vias to dissipate the heat from your packages and still maintain the reliability of your system.

The IVH in this particular case can be placed in any position. That is the beauty of this process. The wiring capability is improved greatly because you have more space for wiring, your wiring diameter, or interconnect track widths are very small matching with the thickness of the via structures. Typically you want to use; let us say if you use a 4 mill via, you want to use a 4 mill spacing as a general guideline. You still can increase the spacing if you are worried about the crosstalk and other parasitics involved with your electrical interconnections.

On the left, what you see here is a (Refer Slide Time: 47:46) cross section micrograph of any layer, Inner Via Hole or Interstitial Via Hole technology. What you can see here is the microvia that has been built up first; it is filled. Then, you have the second microvia structure, which is again filled and then you can see another microvia. So, these are basically stacked. This is a stacked microvia structure.

Now, there can be questions about the reliability of this stacked microvia structure compared to your through-hole structure. That is why we say – in the case of stacking of a microvia, we do not want to exceed 2 or 3 or 4 layers because it depends on the conductive paste that you are using to fill the microvia hole structure. The rigidity of the structure is dependent on the properties of the material that you are using to fill the microvia structure because it should not cave in during a thermal cycling process. There

should not be too many solvence in the makeup of the conductive paste, there should be no air bubbles or voids and it should provide very good curing so that you have very good contact with the adjacent copper structure. How do you prepare this kind of board using ALIVH?

Use a material called aramid fiber (Refer Slide Time: 49:33) and the prepreg is made out of the aramid prepreg; let us say – this is typically about 100 micron or 200 micron. Now, you can use this as a substrate and do a laser drilling. Based on your CAD data, first you create the holes. You feed it into you laser drilling machine and you get a substrate that has been generated with the microvia structures. Now, using a stencil printing process because, you need to use a right conductive epoxy material; instead of epoxy, you can use some other material, but the general commercial material, economic friendly material is epoxy resin. You mix it with a suitable conductor material – it can be silver, gold, silver copper, or copper alone. It can be finally dispersed - very fine small particles dispersed in this media, and then they can be screen printed or stencil printed into the via structures.

You can see here that after the printing process is over; this is by printing (Refer Slide Time: 50:49). After this process is over, copper foil is taken on top and bottom. Now, you decide what kind of thickness you want. It can be a 100 micron foil that you can put, wrinkle free and treated copper is now placed on top and the bottom, and now, the structure is laminated. Here, what do you do? You want to cure the material and you are also using the prepreg material's physical properties because it contains some kind of a solvent – it is a B-stage resin as you know. Then, you have the uncured conductive paste that has been dispensed in the hole wall. All of these entities together are laminated. Now, you get a very good bonding between the conductive paste, between the prepreg and the copper at the top and at the bottom, and you get a very rigid laminate structure.

Now, this is very suitable for patterning your holes and etching out. So, you can remove the copper here (Refer Slide Time: 51:55), you can create a pattern as you have seen here, and then you can create a microvia again by using your print (( )). By using your photovia methodology, you can open up a microvia, or you can also use a laser drilling additionally to open up the copper, and then create a microvia structure. So, you can build up layer by layer, but the essential process is that you get the readymade available prepreg materials from using aramid. They are of standard thickness, but you utilize and

you eliminate mechanical drilling here totally. You can align these microvias like here and stack them to get a comparatively through-hole structure kind of a formation, construction. If your process is well established, you can expect a very good reliability even in these through holes in these stacked microvias.

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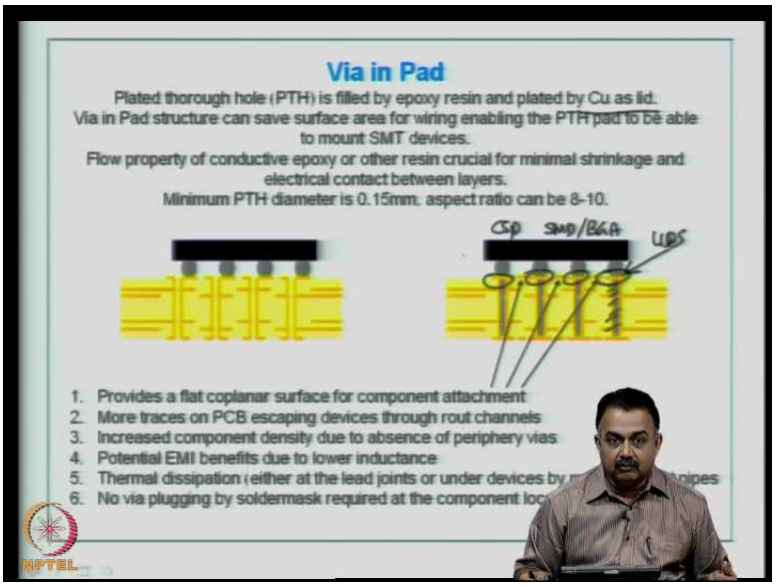

The other one that we have seen briefly is called a Via in Pad structure. A plated through hole; in this case, microvia by mechanical drilling is filled by epoxy resin and plated by copper to form a lid. You can see here (Refer Slide Time: 53:15), these are the lids, where a through hole has been plated and then they have been filled by the conductive material. If you talk about a very large depth, then the conductive paste material has to flow much better, rather than being a thick paste because you want to cover the entire area of the through hole. Now, Via in Pad structure is called because you can utilize the lid of your through hole for mounting your SMD or a BGA; let us say for a CSP. So, it becomes more dense and it is not required to provide additional pad area on the surface of the board. So, Via in Pad structure can save surface area for wiring enabling the PTH pad to be able to mount surface mount devices.

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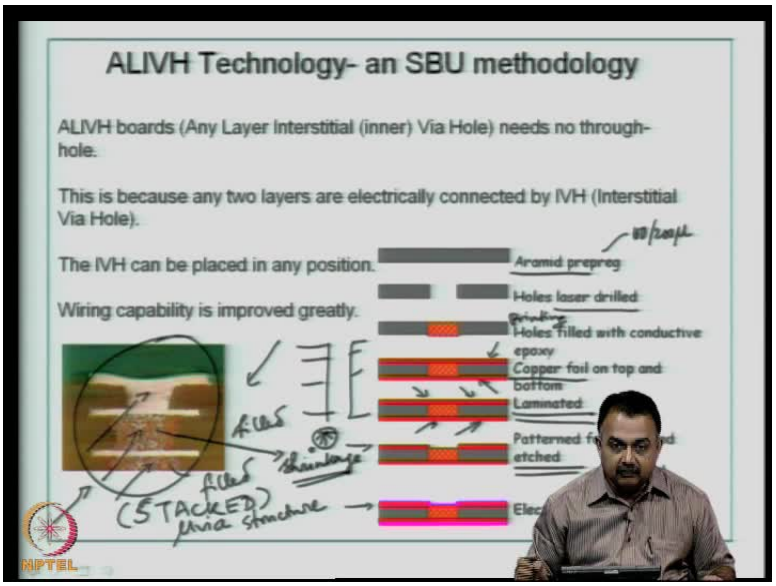

Flow property of conductive epoxy or other resin - crucial for minimum shrinkage - even in the earlier figure, what I wanted to emphasize here is that, the material should not undergo shrinkage (Refer Slide Time: 54:31). So, look at the property of the conductive paste very carefully when you are using for filling the microvia structures.

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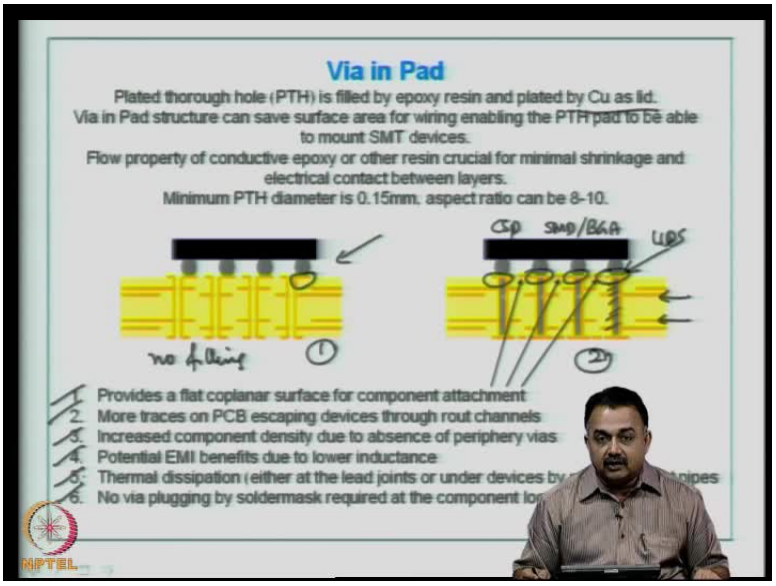

So, resin property is very crucial for minimal shrinkage and electrical contact between layers because here again you can see that this electrically conductive paste is interacting or connecting to your inner layers. So, you cannot lose the reliability in those areas.

Minimum PTH diameter is about 150 micron, aspect ratio can be 8 to 10. You can work with this aspect ratio in this process because you are not doing electroless plating, but you are simply filling it. The aspect ratio in these cases can be an issue if you are using wet process like an electroless process because you need to make sure that your liquid; that is, the electrolyte in the electroless copper plating bath, wets through the micro holes and then provides a very good even thickness of copper. That can be done by micro sectioning; but, rather than going through that route you can work with the filling of the via.

What is the advantages of the Via in Pad? It provides a flat coplanar surface for component attachments. So, you have to do some kind of a polishing at the top. You can see in this particular figure here (Refer Slide Time: 56:01), if you have provided an extended pad area for the microvia, you can utilize that pad for mounting your BGA devices. You do not have to fill the microvia with conductive paste. So, this is an additional option that you have. Here, you are not utilizing the entire area or the lid of the microvia. In this case, there is no filling, whereas in this option (Refer Slide Time: 56:34), you can place it directly on the lid of the via, which has been filled with the conductive paste, but in this case, you have to polish the surface of the top and the bottom if required in a different area. Then, provide a very good surface – planar/coplanar surface for mounting your devices.

More traces on PCB escaping devices through the routing channels because it acts as a… Again, in this case, it acts as a thermal via. Then, you can design accordingly that where your thermal via routs can go into the thermal relief planes that you have provided in the inner layers.

Increased component density due to absence of periphery vias. Potential EMI benefits due to lower inductance because if you look at the contact point between the BGA solder ball and the pad, it is almost a very low interconnection length. Therefore, there is low inductance.

Thermal dissipation either at the lead joints or under devices by means of heat pipes. So, these structures act as heat pipes and no via plugging by solder mask required at the component locations; otherwise, what you do is, you plug the area with a solder mask material. So, here we are using a conductive paste to perform that function.

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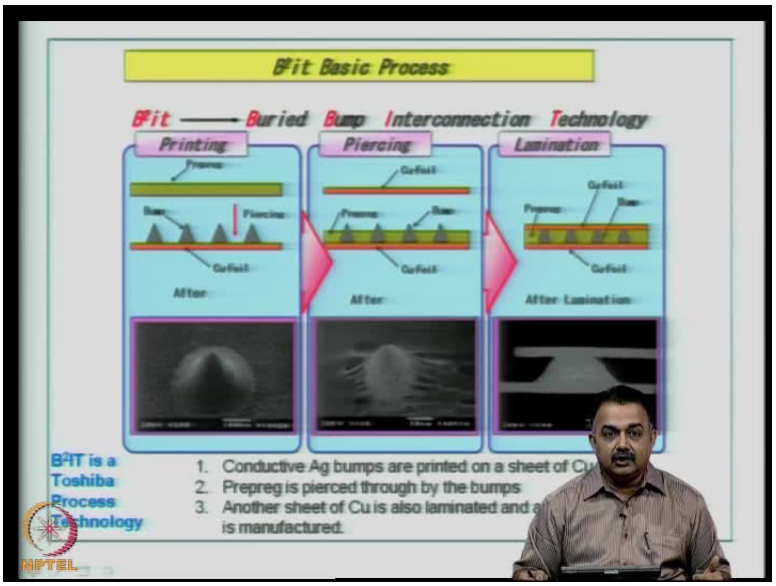

Now, we will look at another process as a case study which is called the B squared I T process. B squared I T is known as buried bump interconnection technology. It is a patented trade mark process technology owned by Toshiba. B squared I T is a Toshiba technology. The popularity of this is not well known, but Toshiba has experimented with this technology and probably used in a few of its commercial products. We will look at this process in the next class in detail.

What we have seen today is a summary of the high density interconnect processes, we have seen how an SBU process flow is, we have got into the basic mode of comparing between conventional multilayer boards and high density interconnect boards, and we have seen a couple of high density interconnect processes that have slightly extended compared to the SLC processes. We will continue with another example called the B squared I T, in the next class.