An Introduction to Electronics Systems Packaging

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Module No. 01

Lecture No. 02

Definition of a system and history of semiconductors

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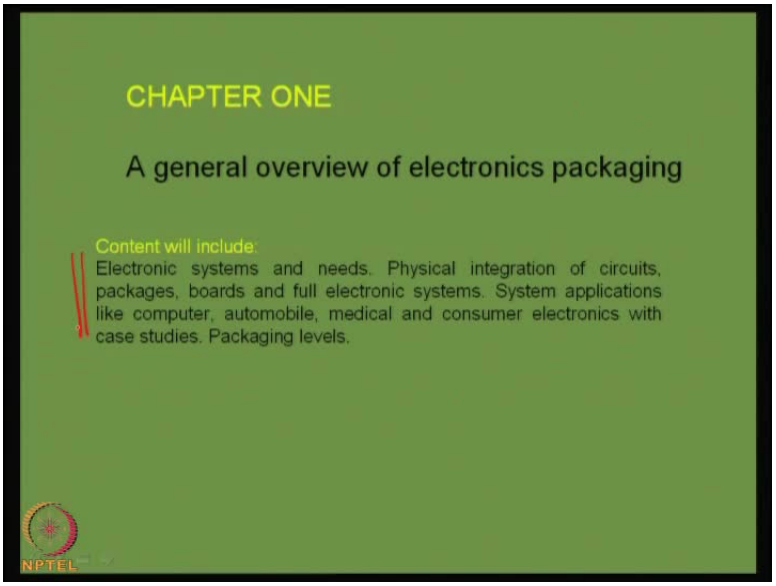

Chapter 1 will consider an overview of electronics packaging and as I mentioned before, the content will include electronic systems and needs, physical integration of circuits, packages, and boards; by boards I mean printed wiring boards, and complete electronic systems. I mentioned before that for example, this is a complete electronic system; a miniature system. System applications like computer, automobiles, medical and consumer electronics, with case studies, will be presented. We will look at each of these sectors, like computers. What kind of packaging practices are followed in automobiles, in medical area and consumer electronics, and we will also define the various packaging levels.

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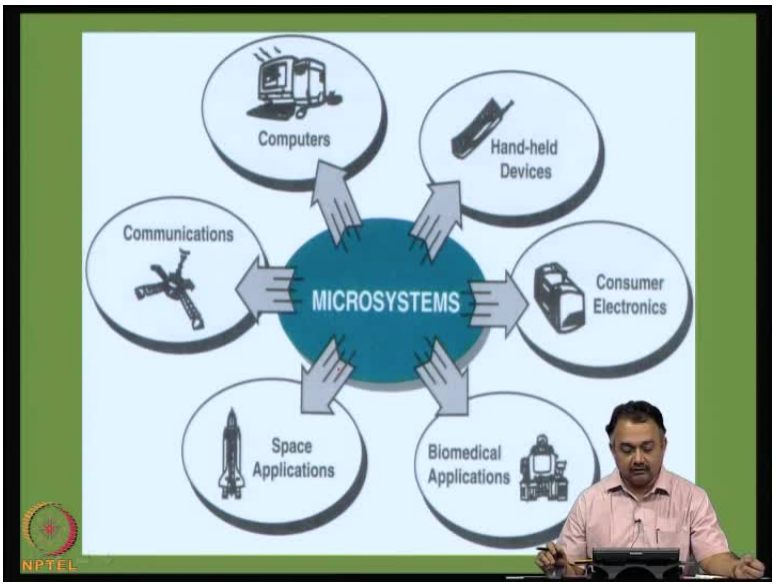

So, if you look at this figure, at the center we have what is known as the Microsystems. So, most of the miniaturized products will fall under this category of Microsystems. Then we have a majority of the market applications that is in hand-held devices area. Consumer electronics also occupy a major portion in the global market, whereas biomedical applications are very few, but today gaining great importance, because of the precision that is required in the packaging and the reliability that is required in the Biomedical Applications. In the field of communications, we have a wide variety of products and there also a great precision is required and as you know communication today is very important, globally. There are some strategic areas like space and military, these require very different kinds of packaging criteria that needs to be considered. In the case of computers this is a very large market. You have desktop computers, workstations, laptops and so on.(Refer Slide Time: 02:43)So, what are the essentials of every electronic product or system? As you know, if you open up a device, a system, you will see semiconductor devices such as integrated circuits, there will be packaging to integrate these ICs on other devices into components. So, when a bare die or an IC is manufactured, a group of these ICs are put together and interconnected to form components. So basically, from transistors we move into well-defined packaged components and that is used in every system.

Then we have system-level boards, which integrate these components, to form the system-level assemblies that provide all functions required of the system. There is a large degree of integration that takes place, because components are mounted on boards and there are interconnections between boards, and they form system-level assemblies, it can

be a sub assembly, various sub-assemblies are interconnected again by connectors wires and so on to form a main system.

So, in all of these, the functions that are required of a typical electronic system is, there will be electrical interconnections and they can be functions, can be classified as analog or digital. Components must provide the needed mechanical and chemical functions, because they require rigidity, sturdiness for a particular product, and in some cases, there are certain chemical functions that will be expected from a product, especially, in the case of bio applications. Systems packaging involves electrical, mechanical and materials technologies. So, I think one must appreciate the statement because if you look at any packaged system, the design will involve electrical issues, mechanical issues and materials issues, which in this course as we go along we will look at it.

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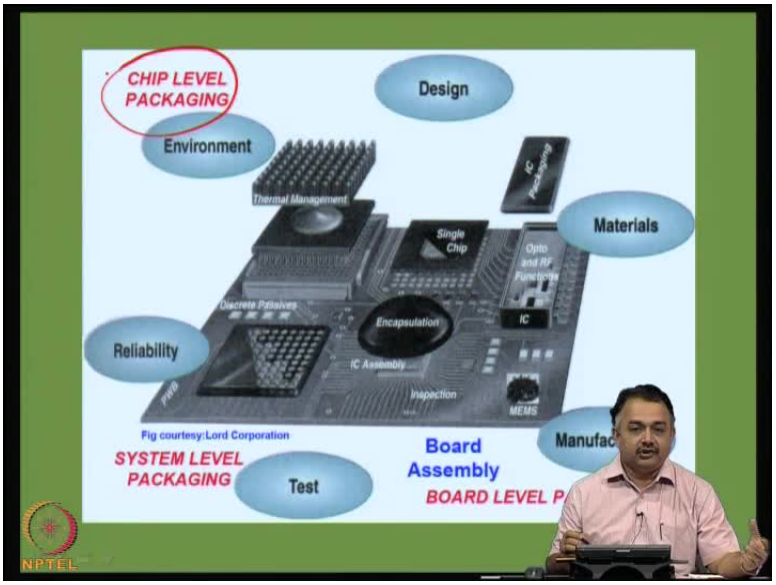

There are three levels of packaging; which I have indicated earlier. The lowest level or the first level is called chip level packaging; where we look at chips that are manufactured or dies that are manufactured, and how to make them or convert them into a package that can be handled by us. You cannot use bare die everywhere and at every point of time, but today bare dies are being used and we are able to understand how to handle bare die, but the majority of the die that is being used today is packaged. So, we will look at chip level packaging.

Then we have what is known as the board level packaging, where these bare die or packaged die are mounted on system level boards and they are assembled together to form or perform a system level function, and finally we have what is known as the

system level packaging, where these get integrated to form a complete system, like your mobile phone or it can be a laptop or it can be your i pod or i pad and so on.

So along these various packaging levels, we are going to touch up base with electrical design issues, new materials, volume manufacturing we are not talking about small volume manufacturing, we are talking about large volume in industry because, large volume can only reduce cost and any design that is being considered by the industry today is looked upon for high volume manufacturing. Then we have board level assembly issues that we will look at, and finally reliability issues, reliability comes from electrical reliability, mechanical reliability, thermo mechanical reliability. And then finally, we have very important aspect called electrical test, because any product should be tested for the electrical functions. Once the product is manufactured in large volumes, there can be instances where you require testing periodically. So, a well-defined test function should be established for a particular product.

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Now if you look at this slide, I have indicated why microelectronics systems packaging is important. Why should we, why should all of us have some kind of sensitization to electronic products and its packaging phenomena that have gone into the particular series of product? The reason is every IC and device has to be packaged. The packaging activity controls the performance of computers because, once it is packaged, you can really say how well it can perform, controls the size of consumer electronics, because today if you look at consumer electronics, people want very small products, we are already fed up with large size products. So, miniaturization has already taken place, for a common man we would like to look at how best to offer a small size. It need not be

always small size, but wherever possible it can be small size so that it becomes very handy, you can hold it in your hand comfortably, with low weight and high performance. So as I said it controls the reliability of electronics. Whenever we reduce size of a product, there can be lot of reliability concerns, because of heat dissipation and because of space constraints and so on. That is a very important aspect. So, again controls cost of electronic products, because if a product is manufactured in large volume, the cost will come down, required in nearly every industry such as automotive, communications, computers, consumer, medical electronics, aerospace and military.

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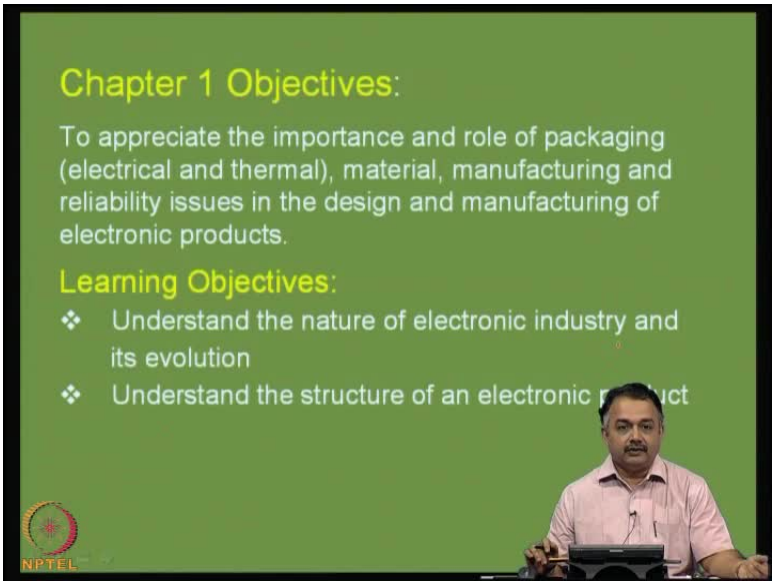

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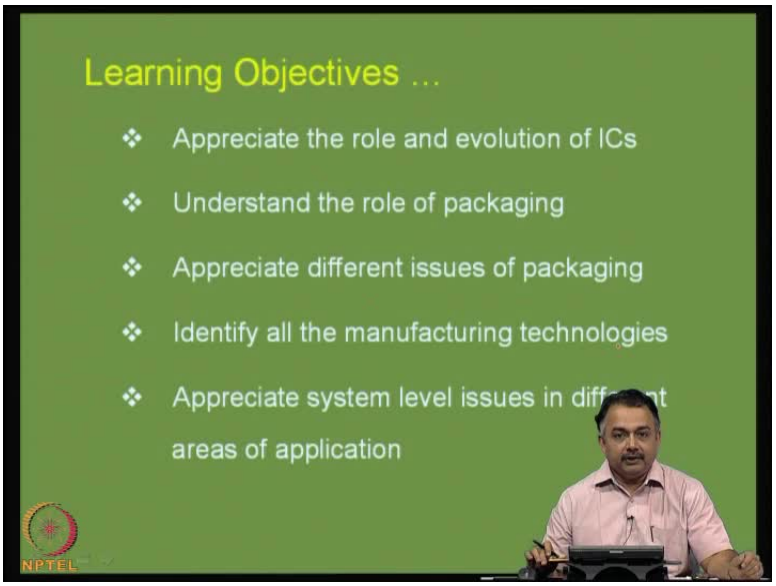

So the chapter 1 objectives will be to appreciate the importance and role of packaging, both electrical and thermal, material, manufacturing and reliability issues, in the design

and manufacturing of electronic products. We will understand the nature of electronic industry and its evolution very briefly. We will look at the structure of an electronic product. We will appreciate the role and evolution of ICs. I will briefly discuss how ICs have gone a long way from the early 40s to the current IC manufacturing situation. We will also look at some numbers, including line bits, sizes and so on. Understand the role of packaging in each of these areas; appreciate different issues of packaging which I mentioned in the previous figure. Identify all the manufacturing technologies both IC as well as the board level. Appreciate system level issues in different areas of application.

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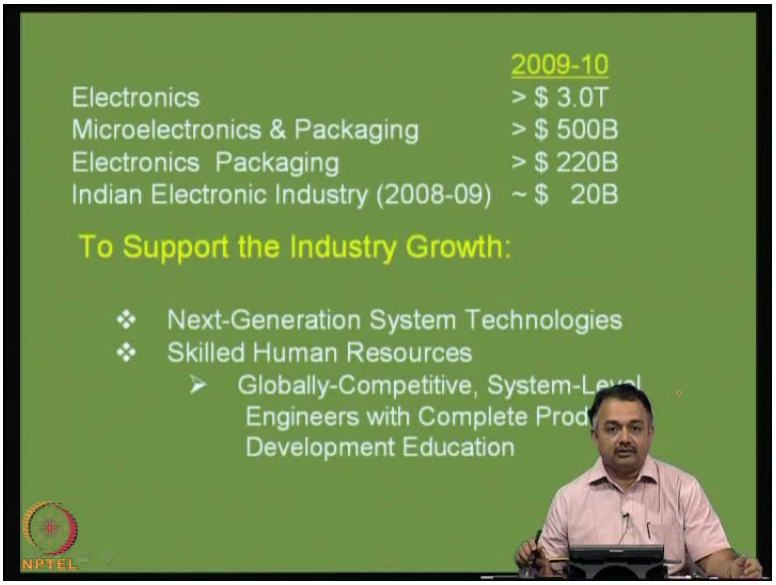

So, please remember we will be using the term system very often because, even if you manufacture a board it should perform system level functions, and so we will see what system level functions are from here on. If you look at the global market as of 2009-2010, this is very current; the total electronics industry is greater than three trillion dollars, which is very large. Microelectronics and packaging in that part of the electronics industry is about 500 billion dollars and electronics packaging is about 220 billion dollars and you can see in comparison, the Indian Electronics Industry is totally only around 20 to 25 billion dollars. So, you get a feeling that where we stand globally. So, obviously there are leading players in the global market including the US, Japan, China and Europe. We need to look at what are the issues? How this market grows? Is there potential for packaging in such a major industry today? So, out of the total global electronics we are talking about Electronics Packaging, which really excludes IC manufacturing. IC manufacturing would really come here under Microelectronics, so we

will look at what are the areas in electronics packaging which contribute to the global market.

So to support this industry and for this industry to grow, we need to work on next-generation system technologies. Constantly we need to look at new technologies that can support the system evolution, for this we require skilled human resources; globally. We need people who are globally-competitive, system-level engineers who can understand system as a whole and with knowledge of complete product development.

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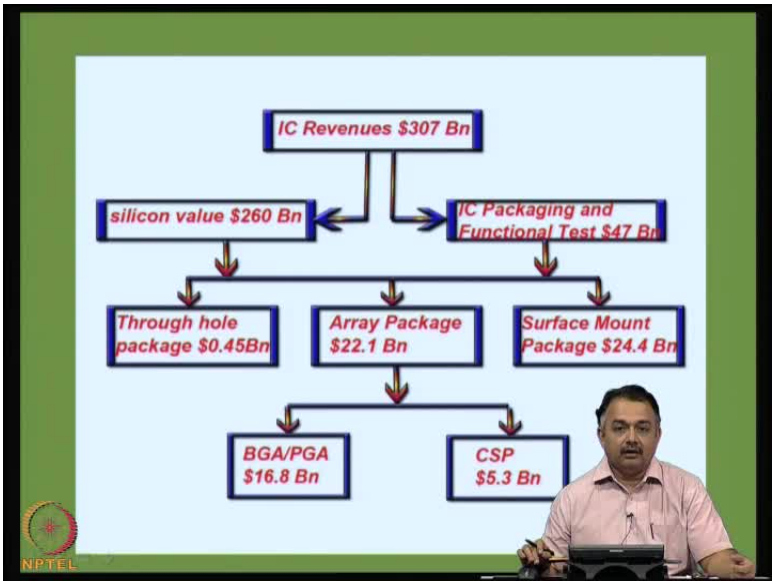

If you look at total global money involved in this industry the IC revenues totals around 307 billion dollars, that means this is all of IC manufacturing. Then we talk about silicon value in that because, IC does not really mean only silicon, there are other materials and processes involved. So, the silicon value out of that is about 260 billion dollars. Then there is definitely a cost that involves IC Packaging and functional test, which is about 47 billion dollars and if you look at the packages that come out of this silicon and, other materials are also used apart from silicon in this industry, so if you look at the packages that come out of this industry, you can classify it into different packages, the first one is called through hole package which is very commonly used today in the industry, the second one will be known as area array Package, which is about 22 billion dollars and surface mount technology or surface mount package which also has the largest market share or usage or consumption globally, which is about 24.4 billion dollars. This really shows that a through hole package, so I must tell you what is a through hole package, if you can see this video, this clip here (Refer Slide Time: 14:35) I am showing a package which is plastic in nature and it has got leads from both sides. So, there is a definite

separation distance between each of this row of pins and you can see how well it is packaged. This is known as a through hole package.

And when we talk about area array package, we are talking something like, packages like this which is surface mount. You can see the periphery of the pins are on the four sides of the package whereas, here it is only on two sides. So, this is typically known as the surface mount device. This requires a hole in the printed circuit board for assembly. These are the various types of components that are being manufactured today.

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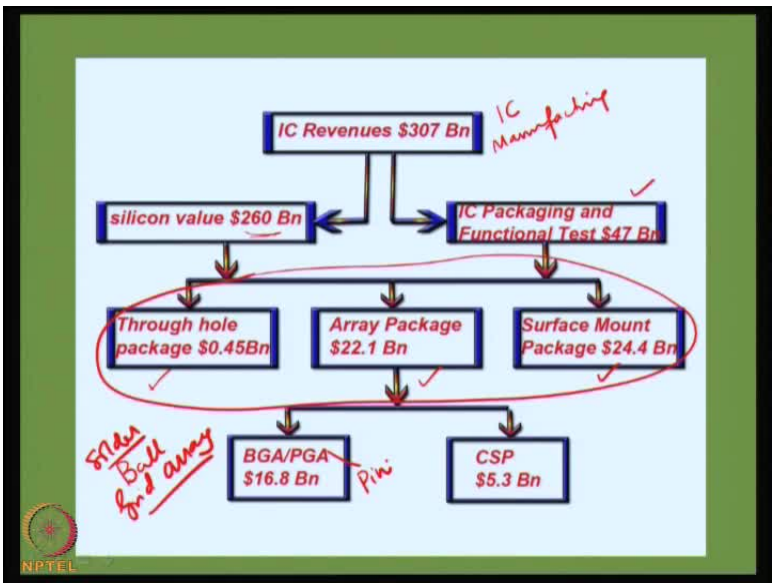

Then comes, the area array package which means the entire area under the die is being utilized for creating the IOs. So, under the area array packages we have ball grid array BGA stands for ball grid array, which means the interconnection of the package is in the form of solder balls. PGA indicates pin grid array. I will show you an example of a pin grid array, here you can see, this is a Pentium processor and you can see the IOs here at the bottom is in the form of pins. So, the connections are established through the pins. This is an Intel Pentium processor, fairly heavy, this is completely packaged. If you take a cross section of this die, you will see the bare die inter connected and finally, the IOs are in form of pins.

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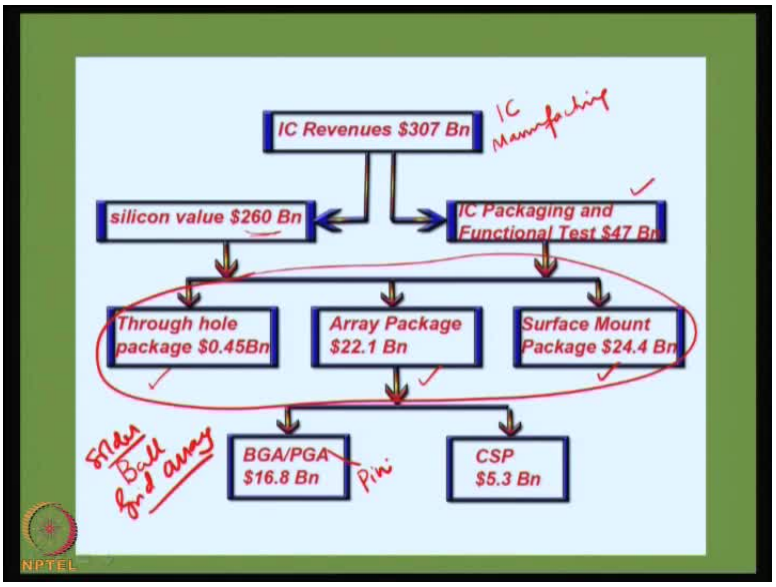

And finally, we will look at what is a chip size package CSP stands for chip scale or chip size package. This chart what I am showing you now, is fairly very current. 20 years ago most of us were using through hole packages, today we are into the area array and surface mount device arena and that is how it displays a significant growth and miniaturization across products.

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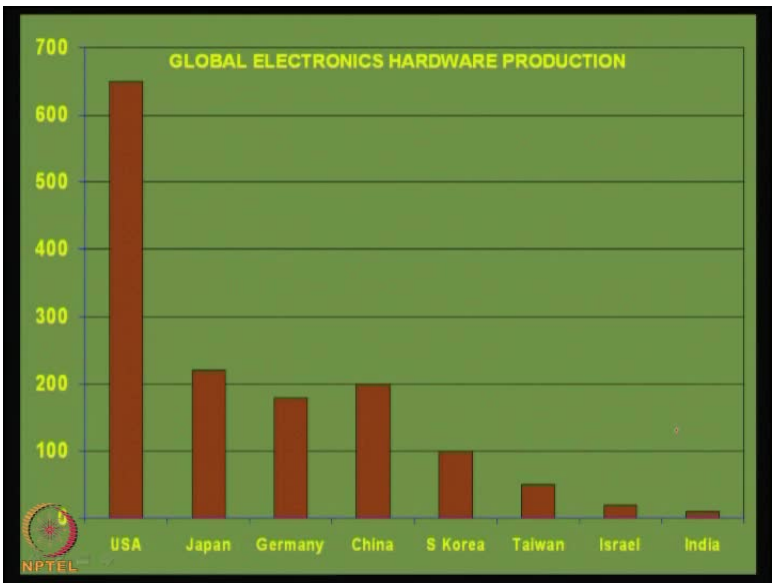

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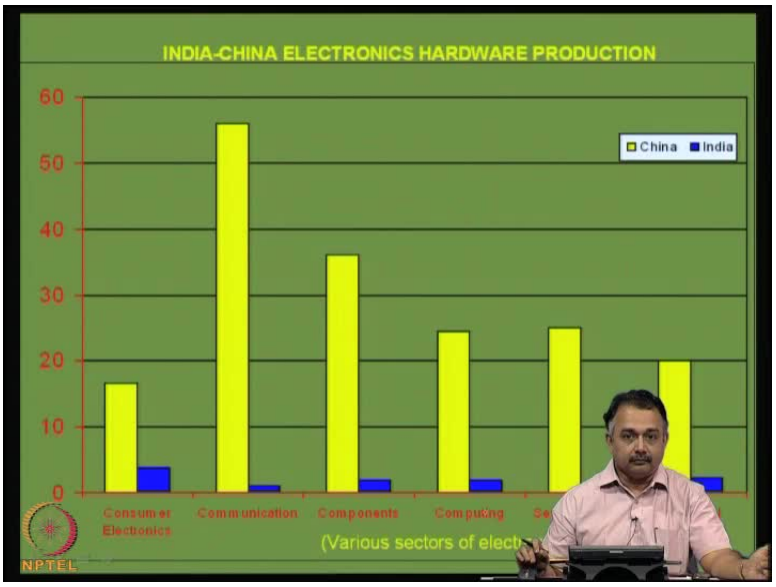

If you look at this slide where I have indicated Global Electronics Hardware Production, if you look at USA, it is almost 650 plus billion dollars. This is total electronics hardware production and we are close to about 25 billion dollars and there are players in between including European countries who have a major share in the market and if you just compare India-China Electronics Hardware Production, again we are lagging behind. We are very good in software but, we are slowly picking up the hardware production area and there needs to be a lot of growth in this sector also.

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Electronics industry is characterized by technology that is driving the business; you must know what the technology is that is being used in the packages today. And you must see how and when you can use that technology. Is it commercially viable? Rapid

technological advances take place because, every 2 years there are new technologies and every 5 years you can see one technology totally replacing other technologies. So, we need to keep pace with the advances and the designers should really take note of these technological advances and incorporate them into the product design.

You must be competitive, so you must be prepared for continuous price erosion. So, your design should also take care of new materials that are not very expensive. There is high growth rate, large volumes are required for any product and you must look at global market not just the local market and any product has got very short life cycle which means your company must be prepared for a new design or a new model or a new system even once a new product is evolving.

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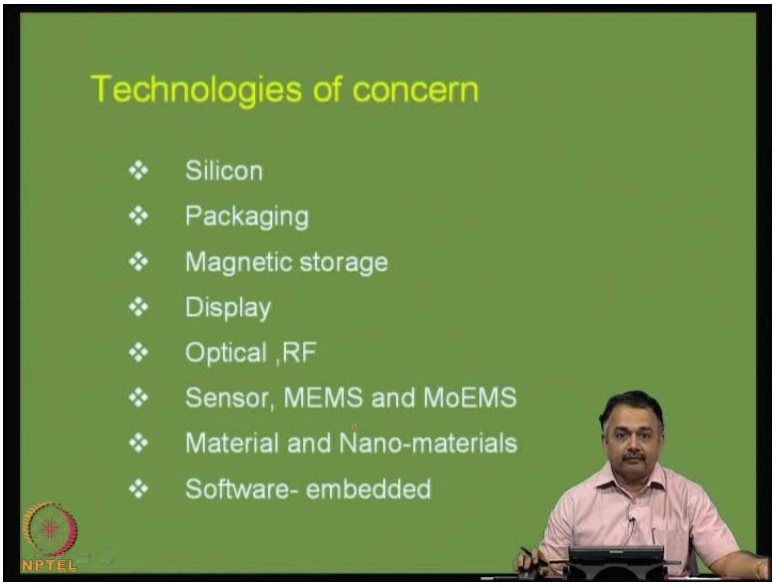

So technologies of concern in packaging will be, we must know the growth of silicon and other semiconductors, look at packaging options available, if you look at magnetic storage, most of the hard disks and other storage materials, we have seen a phenomenal growth over the past five years. So, that really indicates the growth in the industry, display technologies LCD, LED and so on. All of these display technologies have come up and these are now getting very nicely integrated with systems. A new area that we have to look at is optical and RF interconnections, RF components, optical components, RF components are now going to be used in very many hand held products and MEMS stands for micro electro mechanical systems, MoEMS stands for micro opto electrical and mechanical systems and sensor technologies are rapidly increasing today because, any system whether it is automobile or it is a consumer electronics or a precision bio medical application they require some kind of sensor technologies optical and RF.

So, we will have to look at when you do the packaging for a product, we need to look at these aspects also and these industries are growing, MEMS industry is growing, sensor technologies are improving, materials and nano-materials nevertheless, we are always on the constant lookout of new materials, because new materials will display or exhibit better electrical properties, better thermal management issues, better thermal properties like heat dissipation and removal of heat from surfaces and software of course, is embedded in systems, it is very important nevertheless.

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What I am now showing you is some kind of a history that has taken place and we need to know where we are in terms of IC and products. If you look at the growth of the semiconductor industry 1906 Lee De Forest discovered the Triode -The Audion- in 1906. We can see how bulky it is, then as we progressed there were other discoveries, but the important thing came from germanium, use of germanium, that is the first point contact transistor. You can see a transistor very bulky and you can imagine a current transistor today that shows the growth of materials. This germanium transistor was invented by or discovered by John Bardeen and Walter Brattain from Bell labs.

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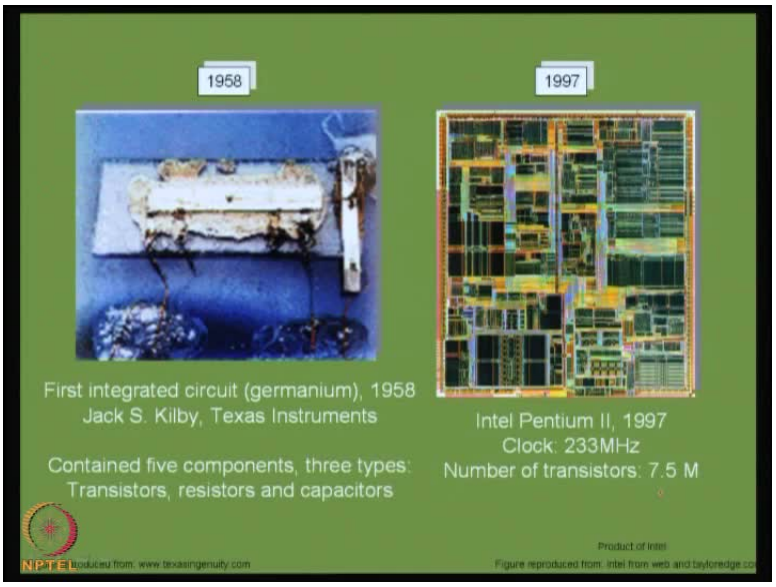

As we move along, we can see the first integrated circuit coming up in 1958 using germanium. This was put together by Jack S Kilby of Texas Instruments and it contained five components; three types, transistors, resistors and capacitors. Here again you can see, the bulky nature of this particular device and in 1997 you can compare, Intel has come up with this Pentium II and with a clock speed of 233 megahertz. Number of transistors there are 7.5 million. So, you can see in this very small die area, the entire die area how much of transistors have been packed.

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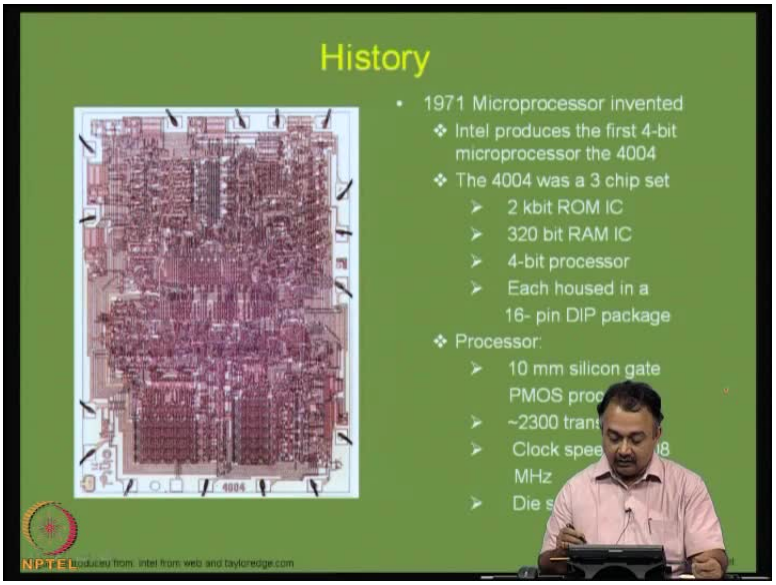

I will again briefly take you to some of the semiconductor manufacturing phenomenon that has taken place and that indicates the growth and how much of packing has gone into silicon die. If you look at 1971 the microprocessor was invented, Intel produced the

4-bit microprocessor called the 4004. It was a three chip set and you can see it housed a sixteen pin DIP package. A package something like this (Refer Slide Time: 24:11) and it contained a 10 mm silicon gate, it contained only 2300 transistors, but that was great at that time and the die size was 13.5 mm square. So it is fairly large but, compared to the previous slide that I showed this is a major improvement.

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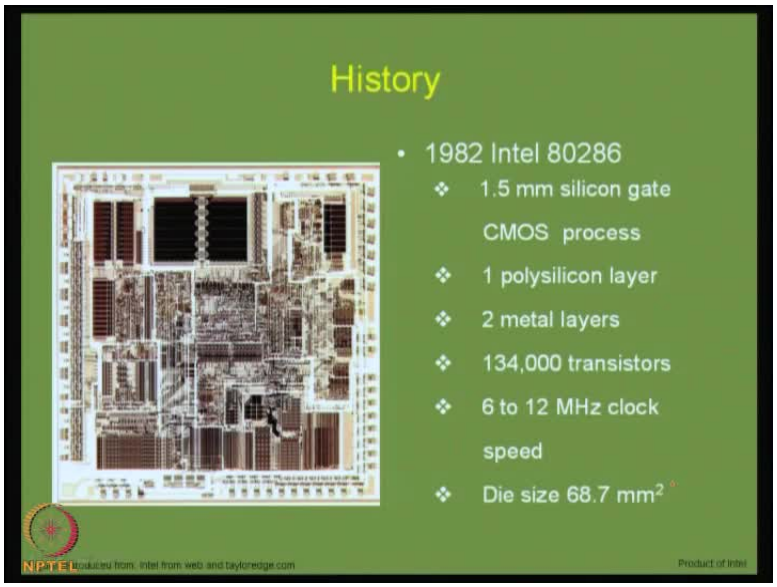

In 1982 Intel came up with 80286 1.5 mm silicon gate technology. It contained 134000 transistors and with a clock speed of up to 12 megahertz and the die size is about 68.7 mm square. So, you pack more material, obviously the die size will increase but, you can have two metal layers for example, that has been created.

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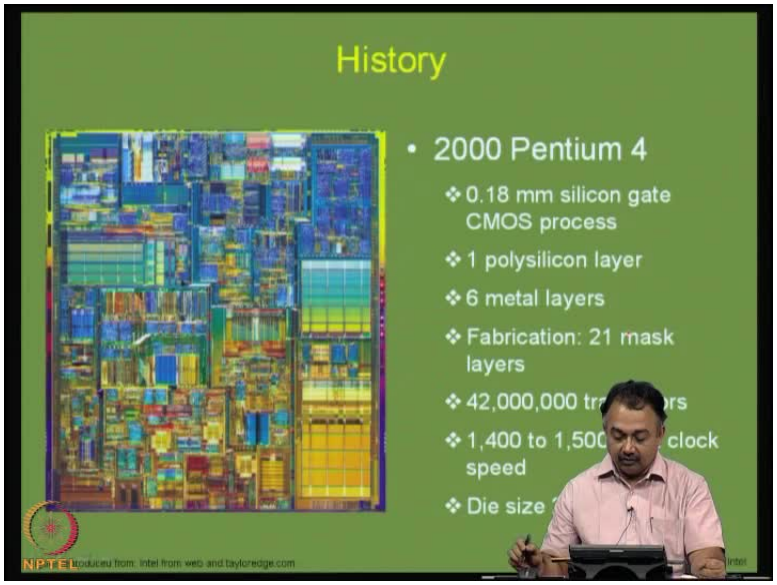

Then came Intel Pentium 4 in 2000 if you look at the technology used here 0.18 mm technology, what do you mean by 0.18 technology, that is the line width or pitch D RAM pitch that has been realized using photo lithography methods on silicon gate using CMOS process and it contains 6 metal layers. The fabrication involved 21 masked layers that means for photo lithography you need to require to prepare 21 masks that need to be sequentially aligned one layer to the other without errors and aligning them and it contained almost you can see here 42 million transistors. So that is a big jump in 2000 and the die size you can see is fairly large 224 mm square, so you can imagine a device something like this that I show here (Refer Slide Time: 26:14) if you feel this it is fairly heavy, it has got a metal package and it has got a large number of pins on the other side, obviously why should the die size be large because we have to accommodate so many transistors and when you pack so many transistors the one thing that comes to our mind is how much heat this will dissipate when the device is powered up. So, issues like electrical performance and thermal performance come into picture when we look at large die size and different package materials.

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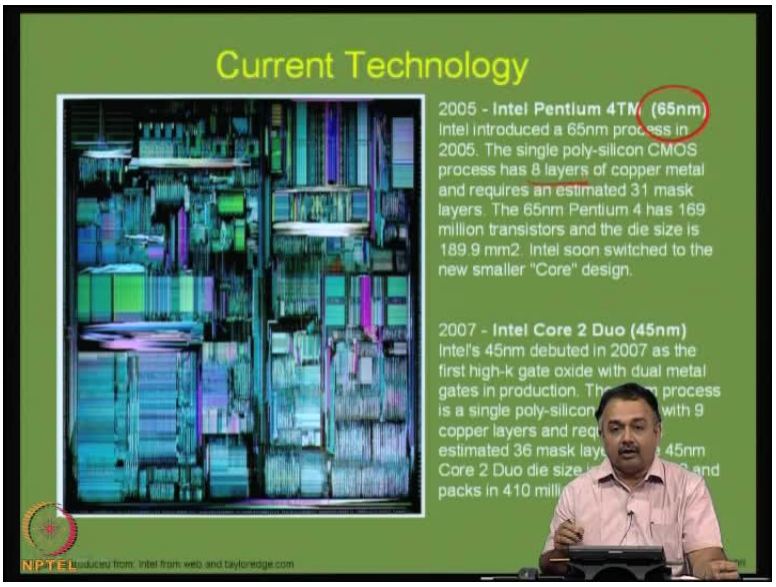

In 2005 the 65 nanometer technology was used. Intel used this microprocessor line width of 65 nanometers and it contained 8 layers of copper and it had 169 million transistors and the die size is 189 mm squared. So, Intel soon switched to the new smaller core design, in 2007 came the core design core 2 duo which used 45 nanometer technology and you can see that it contained 410 million transistors and the die size is around 105.78 mm square so the die size keeps varying but, you can see the number of transistors have increased so it is possible to increase the number of transistors as we have seen is

basically because the line width has reduced. If the line width had not reduced, if the technology had not improved we would not been able to increase the number of transistors.

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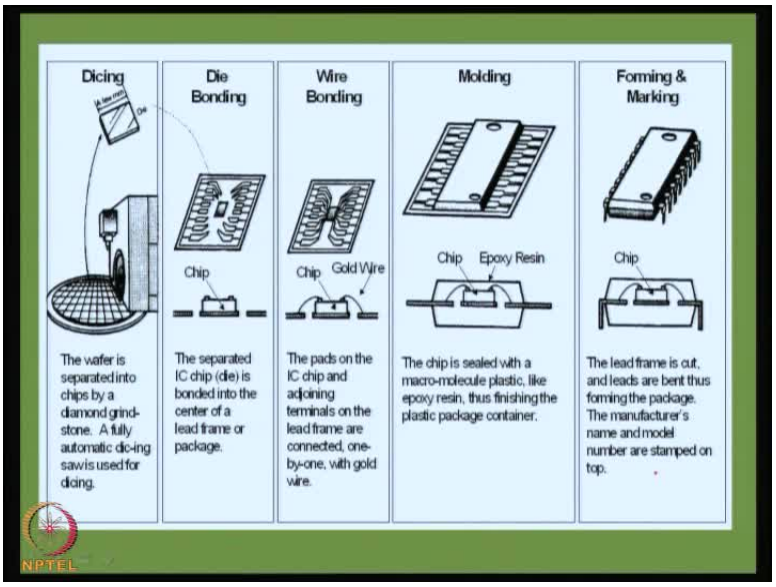

So a brief process of IC manufacturing will look like this. This is not very complete, but I will during the next hour or so talk to you about the complete IC manufacturing process, but if you look at a quick glimpse, if you look at the first slide after the IC is manufactured the wafer as you see it, (Refer Slide Time: 28:32) this is a wafer, this will be diced into chips by a diamond grindstone and the ICs will be individually separated and if you can see the slide, in the next portion of the slide the IOs of the die will be bonded to a lead frame or a package. So there will be some kind of a bonding that takes place from the IC to the lead frame. That is the first level of activity that takes place once an IC is manufactured.

So, once the die is actually bonded onto the substrate, then comes, the wire bonding phenomenon where gold wires are used to connect the IC to the lead frames. So, we can see here in this picture there is a substrate, there is a die, which is attached using some adhesive and then there is a gold wire, which connects the bond pads on the die to the substrate or the lead frame so once this is done it is tested, so next comes the testing process.

Then once it qualifies, it comes to be known as a known good die KGD means known good die. That means it has passed the quality process. Then, there is an encapsulation that takes place using a plastic material, which we call it as Epoxy Resin and then gold wire bonds and the IOs or the bond pairs of the die are protected by a molding process so

this molding process protects the entire interconnections on the chip and that is how it becomes a packaged die. So, now this is a packaged die.

And the final step is forming or marking, the lead frames as I have shown you earlier in this package, they are trimmed, they are bent so that they can be inserted into a printed wiring board and then it can be interconnected to different components.

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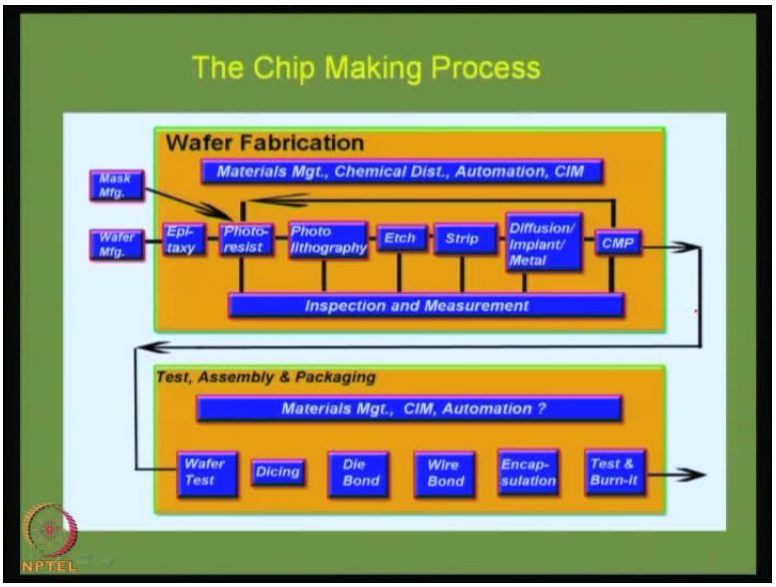

So this is a quick process flow and if you look at the complete and exhaustive chip making process as shown in this slide, there is a front end process. This is known as the front end process (Refer Slide Time: 31:28) and this is the back end process. In the Wafer fabrication, first you have to look at materials, you have to look at chemicals, automation and computer integrated manufacturing. The first thing is a mask that pertains to the design of the IC should be ready and then the wafer manufacturing starts. We start with the bare wafer like this and then there is a process known as Epitoxy which is basically an oxidation, then comes Photoresist, Photo lithography, Etching, Stripping, Diffusion or Implant or Metal, then CMP is known as chemical mechanical planarization or polishing and then finally, Inspection and Measurement. So it is very easy to list the steps but, the time taken and the precision that this wafer undergoes to get a complete definition of the design translated onto the surface of the silicon takes a lot of time takes a lot of quality control and inspection.

So we will try to look at all of these processes one by one during the course of this chapter and then the Back end process involves test, assembly and packaging. The first one is wafer fabrication basically, so once the wafer is completely well utilized there can be no wastage on this particular wafer. Once it is completely utilized and all the dies are

formed, we first test the wafer; dice the individual ICs that have been formed, do a die bonding that is the bonding is done to a base substrate that is there in this package inside. Then we do a gold or aluminum wire bonding, there are different types of attachment, here we are talking about wire bonding. We will also look at other interconnection choices other than wire bond gradually.

Then we encapsulate the system with a plastic package and then finally, test and burn-it. So there are certain conditions, test and burn-in is a very important aspect of the wafer fabrication process and the packaging process. So every die or package will undergo a burn-in test, so there are some temperature conditions and humidity conditions that need to be specified according to international standards including military standards and then we define or qualify this die. So here, out of this comes the complete package.

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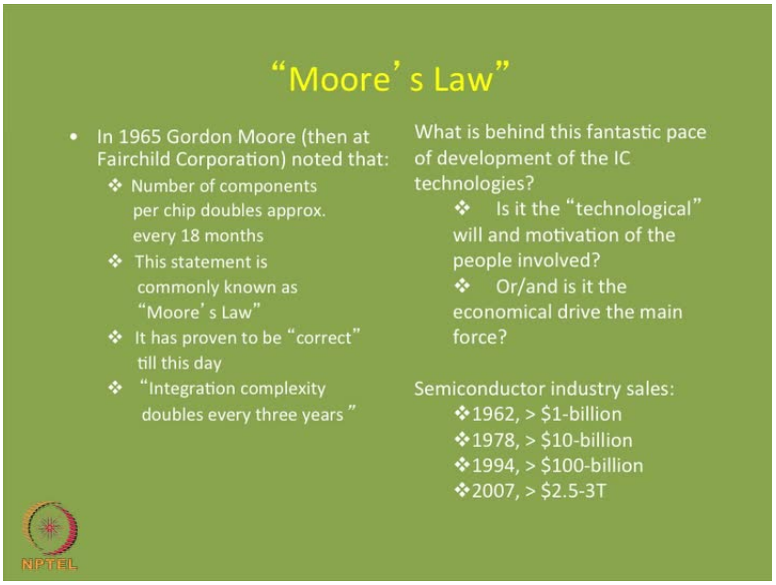

Now we will look at a very important statement or today it has become a law because of its persistent usage in the industry or interpretation in the industry. It was a basic, a mere statement by Gordon Moore in 1965 then at Fairchild Corporation; he noted that the number of components per chip doubles approximately every 18 months. So this was simple statement given by him in one of his papers, but this statement now commonly came to know as Moore's Law. It has been proven to be correct till this day, although there are claims today to show that it is not exactly eighteen months as was predicted at that point of time. So, from 1965 until 2010 we can say that the statement is more or less valid except for the point that, because there have been various economic impediments, we can say that the number of components per chip doubles approximately every 24

months. So that is the kind of a delay, probably one can look at as sort of a deviation from Moore's law.

So Moore's Law basically has been a driving force or you can say one of the important drivers for the industry. Everybody, every industry wants to keep up pace with the Moore's law. All roadmaps refer to Moore's law because they want to be in pace or in tune with the technology. So what it basically says is, integration complexity doubles every 3 years or continuously Integration complexity is increasing and that is the major challenge. Today in 2010-11 we are at the point of asking whether Moore's law is valid or not, because of a lot of restrictions or insufficiencies in equipment technologies. So what is behind this fantastic pace of development of the IC technologies? Is it the technological will and motivation of the people involved or is the economical drive the main force? This, you can ask this question, is a basic question because technology and economic growth are fairly related and as you know there need to be drivers for every technology and the semiconductor industry is also part of it because it defines the growth of many systems.

If for example, the Intel as we have seen from 1970s to 2007, we have seen the growth and this is because of the growth in the semiconductor industry, the processes, the materials and so on, which actually kept pace with the Moore's Law. So, that is how the industry has grown to these kinds of market levels.

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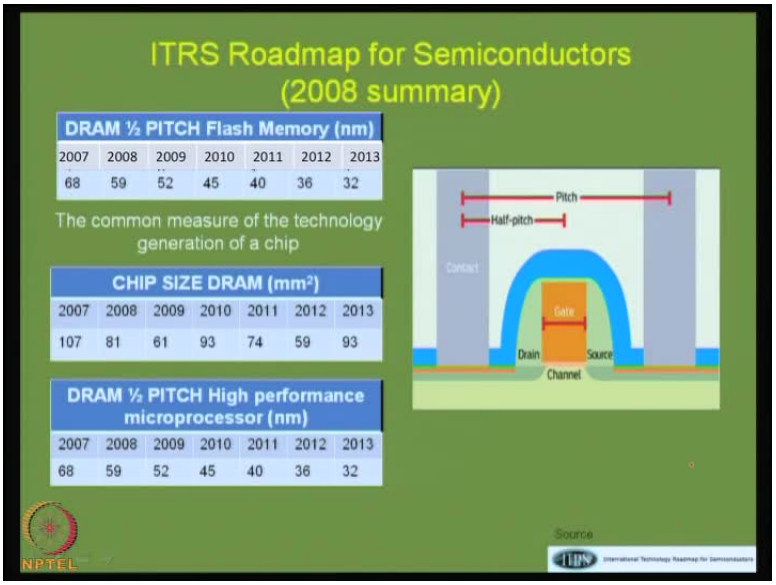

I think you must look at ITRS roadmap very regularly. ITRS stands for international technology roadmap for semiconductors. This is a website available; there are journals available from ITRS. I think as a packaging engineer we need to look at ITRS roadmap

very regularly because it defines the growth in the industry. Now, we talked about the line bits, in the semiconductor packaging industry we talked about 45 nanometers being used in the Intel processors and today in 2013 we are looking at 32 or today we are looking at 22 nanometer technology that is probably going to be used in most of the microprocessors. So, this is a rapid growth and this is a roadmap and we have seen all these growth happening and translated into products. The common measure of technology generation of a chip is basically the D RAM half Pitch.

So what is the D RAM half pitch, if you look at the figure here, this is the basic gate that is described or fabricated or realized in the semiconductor process and these are the electrical contacts and so if this is the Pitch, the midpoint between the conductors, if it is defining the pitch then the half pitch will be this one, (Refer Slide Time: 39:52) that is from the gate to the contact. So this really gives a big challenge to the line width. This is basically realizing using photo lithography process, the line width or the half pitch between the gate midpoint and the contact midpoint, so between these two, there needs to be an absolute dielectric material performance that will not tamper or hinder the electron flow or electrical performance between the two conductors.

So designers at the IC level are now looking at how to reduce this half pitch, as I said we are moving from 45 nanometers to 32 and now 22 nanometers. Can we really do this, do we have equipments that can translate our design in CAD; basically it is a VLSI design using CAD. Now we have to translate into a substrate, so we can see other parameters from the ITRS roadmap for example, CHIP SIZE of a D RAM from 2010 it is 93 and it is predicted to vary from 74 mm square to 59 and again it is predicted to increase with a lot of integration. So D RAM half Pitch high performance microprocessors, the nanometers the technology that are used from 2009 it is 52 to 2013 it is 32 and beyond and less. So this is a big challenge in terms of materials, equipment and also we are looking at dust levels, so if you look at these numbers 22 nanometers and 45 nanometers and so on, these processes take place in an environment where there is no dust. So clean rooms are very essential for IC manufacturing. We will talk about it later.

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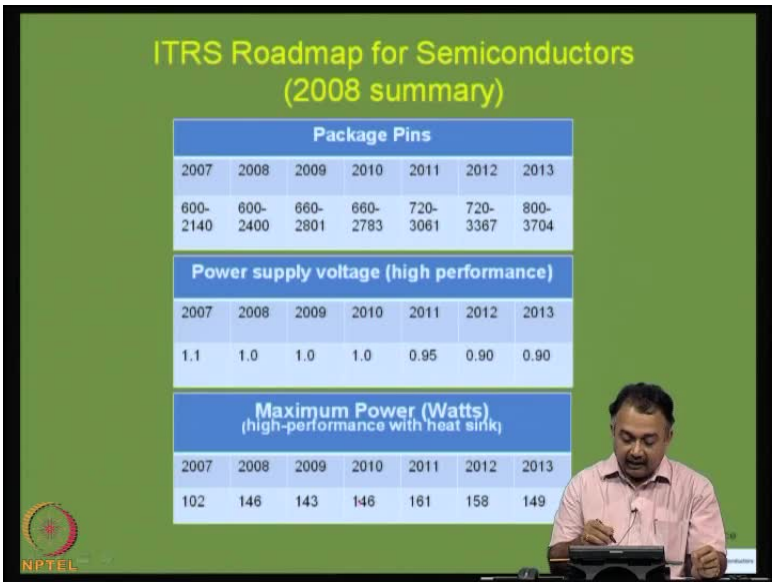

At the same time if you look at the package side, once the IC is manufactured, if you look at the number of IO pins in 2009 it is around 2800 maximum for various types of packages and we can expect it to increase to close to 4000 for the year 2012-13. This is the projection that is given for the coming year. Power supply voltage for high performance products, obviously, for the system, high performance system, the power supply voltage should be as less as possible and we can see from 1.1 volts in 2007, we are now looking at 1 volt and 0.9 volts, so energy efficient systems.

Maximum Power dissipated from the device, 2007 for high performance systems it is 102 watts, today we should be able to look at how to tackle heat at around 150 watts and remove it as quickly as possible from the device to the ambient environment so that your device is not damaged.

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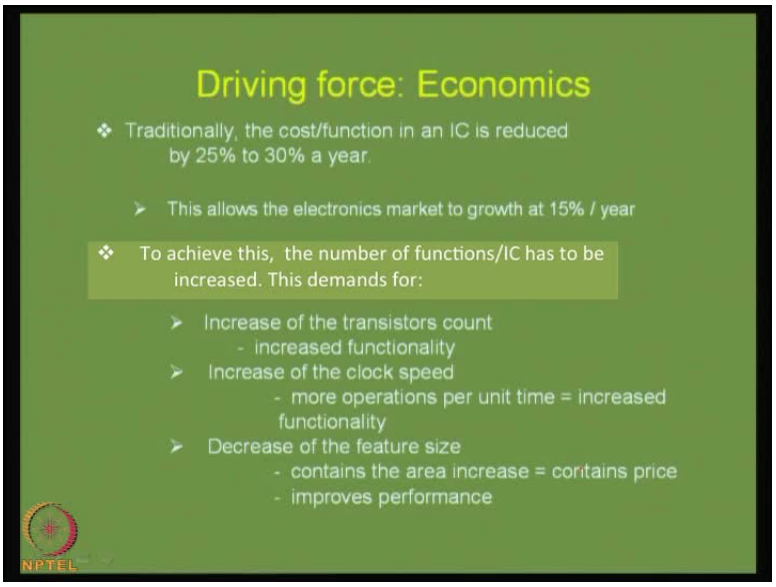

So the driving force or economics will be that the cost per function of an IC is reduced by up to 30 percent a year. This allows the growth mark in the market at 15 percent per year which is required. To achieve this growth the number of functions per IC has to be increased, it cannot be stagnant. This demands increase in the transistor count which the designers are doing it and they have to build it with increased functionality, increase in the clock speed, which means more operations per unit time and which is indicative of increased functionality.

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Decrease in the feature size, it contains the area increase, it contains the price rise and it improves the performance. So, all of these are well inter related. How to increase productivity, increase equipment throughput? So we need to have more equipment and

high throughput yielding equipments. The original equipment manufacturers OEMs as you call them, have a great part to play in the definition of the roadmap, because without the equipments that can give this kind of well-defined feature sizes on semiconductor devices, we would not be able to achieve this kind of economic growth, the yield should be very high, overall yield that means fewer defects.

Increase the number of chips on a wafer that means reduce the area of the chip, smaller feature size and redesign; you convert your older designs to new design and largest wafer size possible. Now you must know for example, (Refer Slide Time: 45:25) this wafer, this is a very small wafer, if you look at the diameter of this wafer, it is very small, in industry the current standard is 300 and people have started using 450 mm or thinking of using 450 mm feature sizes. What is this 450 mm; this is the diameter of the wafer. So, 450 mm will very soon be a large scale volume manufacturing standard, you can imagine a 450 mm wafer being processed with high manufacturing yield, as the silicon area increases as the diameter increases, obviously you want to get high manufacturing yields. So, is there a limit, can we go beyond 450, is there an equipment that can tackle 450 mm and beyond, these are questions that needs to be answered. So it depends much on the equipment manufacturers.

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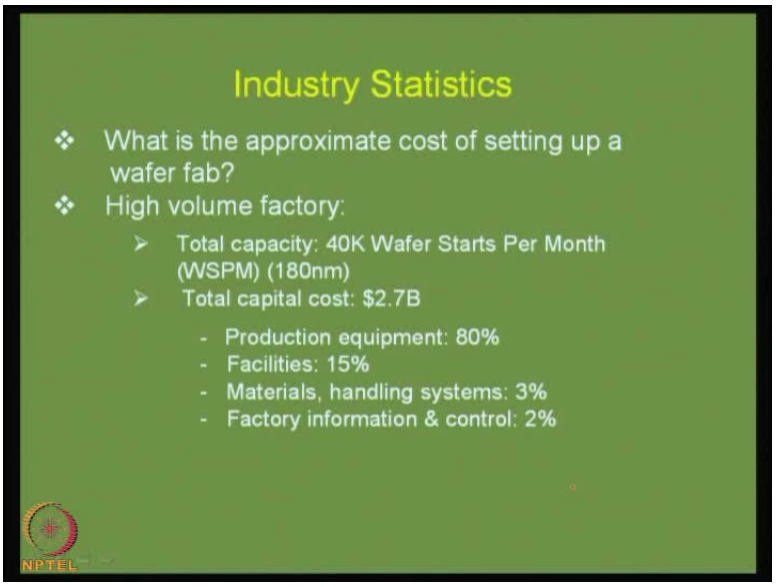

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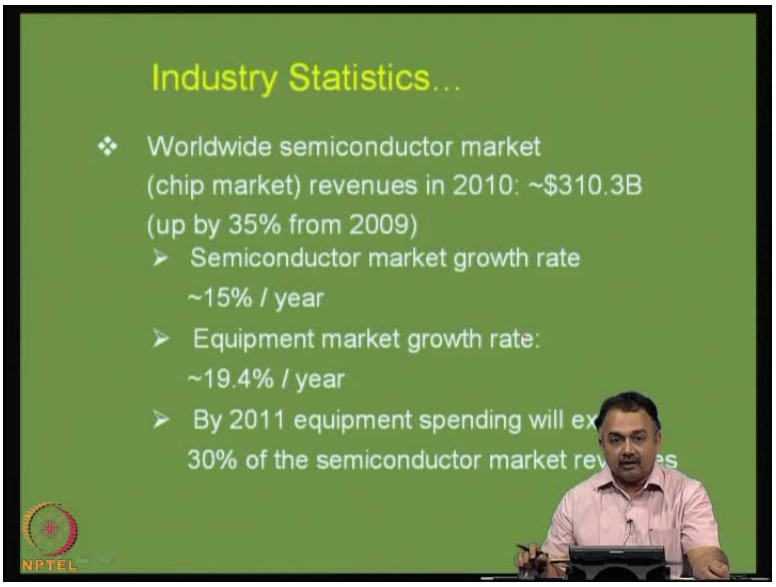

So the industry statistics is, all of you must know about this because, it is just not the packaging information; we need to know some numbers about economics, what is the approximate cost of setting up a wafer fab? If it is a high volume factory with a capacity of 40K wafer starts per month at 180 nanometer technology line width, the total cost is around 2.7 billion dollars and you can look at the percentages required out of these 2.7 billion dollars for production equipment, facilities, materials handling and systems, factory information and control. So the facilities of fifteen percent would include very important aspects like clean room for IC manufacturing. Worldwide semiconductor market revenues as of 2010 is around 310.3 billion dollars, it is an upward rise of 35 percent from 2009, the growth rate is 15 percent per year, equipment market growth rate is about 20 percent per year and by 2011, equipment spending will exceed 30 percent of the semiconductor market. I think it is better to know some of this kind of very general information that is available today from various sources.

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So if you look at another roadmap which is called the Packaging Roadmap where we talk about different types of systems, this is a low cost system and this is a high performance system. These are two different ends, low cost means it has to be low cost at the expense of some performance issues, but high performance can be expensive example, high performance systems used in military and space, they do not bother about cost, they require high reliability. So, you can look at cost per pin here it is in 2014, the expected roadmap projection is 1.44 cents per pin whereas, for low cost it is only about 0.42 cents per pin. Power we need to tackle about 180 watts from the surface of the die, here it is much less just about 3 to 5 watts, performance range in frequency 150 megahertz, here we are talking about a high frequency range. I/O pins count very large, how to handle them? Whereas, in low cost it is only about 200 to 800 or 900 pin count. So these are the challenges for a packaging engineer.

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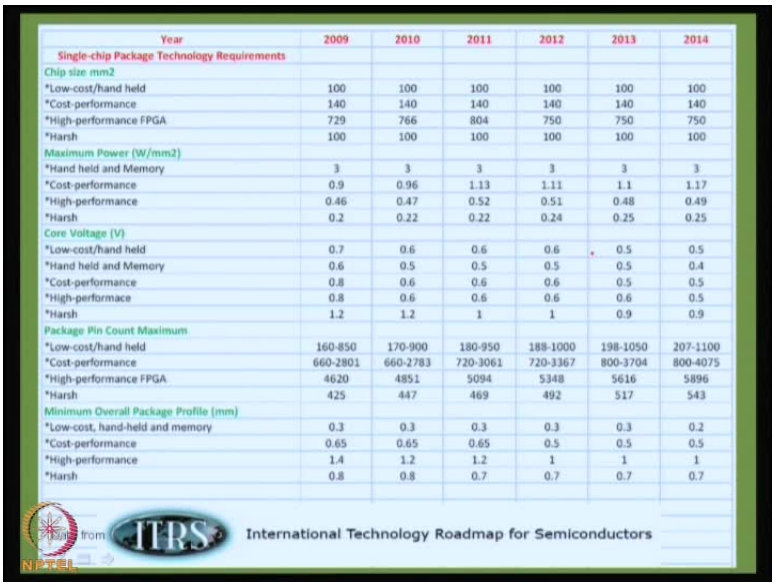

Year	2009	2010	2011	2012	2013	2014
Single-chip Package Technology Requirements						
Chip size mm2						
*Low-cost/hand held	100	100	100	100	100	100
*Cost-performance	140	140	140	140	140	140
*High-performance FPGA	729	766	804	750	750	750
*Harsh	100	100	100	100	100	100
Maximum Power (W/mm2)						
*Hand held and Memory	3	3	3	3	3	3
*Cost-performance	0.9	0.96	1.13	1.11	1.1	1.17
*High-performance	0.46	0.47	0.52	0.51	0.48	0.49
*Harsh	0.2	0.22	0.22	0.24	0.25	0.25
Core Voltage (V)						
*Low-cost/hand held	0.7	0.6	0.6	0.6	0.5	0.5
*Hand held and Memory	0.6	0.5	0.5	0.5	0.5	0.4
*Cost-performance	0.8	0.6	0.6	0.6	0.5	0.5
*High-performace	0.8	0.6	0.6	0.6	0.6	0.5
*Harsh	1.2	1.2	1	1	0.9	0.9
Package Pin Count Maximum						
*Low-cost/hand held	160-850	170-900	180-950	188-1000	198-1050	207-1100
*Cost-performance	660-2801	660-2783	720-3061	720-3367	800-3704	800-4075
*High-performance FPGA	4620	4851	5094	5348	5616	5896
*Harsh	425	447	469	492	517	543
Minimum Overall Package Profile (mm)						
*Low-cost, hand-held and memory	0.3	0.3	0.3	0.3	0.3	0.2
*Cost-performance	0.65	0.65	0.65	0.5	0.5	0.5
*High-performance	1.4	1.2	1.2	1	1	1
*Harsh	0.8	0.8	0.7	0.7	0.7	0.7

And if you look at this exhaustive roadmap information it talks about the roadmap from 2009-14 in various segments like, you talk about chip size in mm square, maximum power, core voltage, package pin count maximum, minimum overall package profile, for a gap for example, if you can see low cost hand held memory the package profile today is 0.3 mm only whereas, for other devices like high performance it can go up to 1.5 mm Package count today 2010 for high performance devices its around 4800 pins maximum. These are the well-defined roadmaps for various sectors in the industry it includes automobiles, hand held consumer, communication products and so on.

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So the challenges in packaging for the industry will be process integration, device scaling, electrical issues especially with regard to signal integrity, RF radio frequency and analog mixed signal design, photography or photolithography will be the bigger challenge to Moore's law. So we are going to look at, in this particular topic we look at what are the new methods or alternatives to Photolithography, to meet these kinds of expectations, light source especially, what new light sources can be used for patterning and mask material that can be used, obviously there is a constant lookout for new materials because, we need to look at low dielectric property and in some cases high conductivity. Manufacturability of the interconnect structures that is copper or other conductors, power management, how to test it, so any device or package needs to be designed for testability. So, the buzz word today is design for reliability, design for manufacturability and design for testability.

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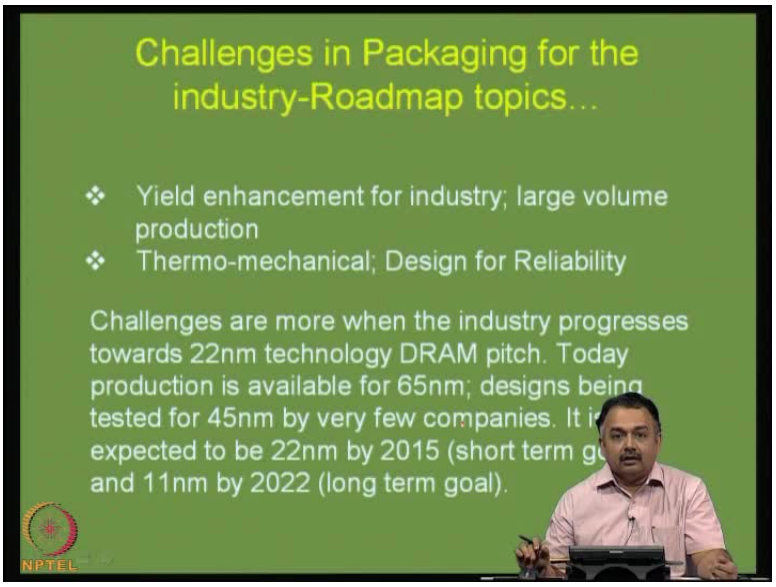

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Equipment challenges are very important, manufacturing cost and cycle time, performance requirement of the market, assembly and packaging issues, resource conservation and environmental concerns; we will also look at green issues, very important, we will see about green packaging. Continuing, yield enhancement for industry, large volume production, this is a very important requirement for the industry thermo-mechanical design and design for reliability. So, the future challenges for the semiconductor industry or the packaging industry will be towards 22 nanometer technology DRAM pitch. Today production is available for 65 nanometers; designs are being tested for 45 nanometers by very few companies. It is expected to be 22

nanometers by 2015 and 11 nanometers by 2022. So, you can imagine the challenges that we have to work with 11 nanometers in 2022.