## **An Introduction to Electronics Systems Packaging Prof. L. Umanand Department of Electronic Systems Engineering Indian Institute of Science, Bangalore**

## **Module No. # 04 Lecture No. # 17 Electrical Issues – 3 Layout guidelines and the Reflection problem**

Good day to all of you. In this session, we shall continue our discussion on the electrical aspects of packaging. We had discussed at length on the three important parasitic elements: that is the resistance, capacitance, and the inductance due to the tracks on the printed wiring boards, and also saw how we go about estimating approximately the values of these components, or at least getting a feel for the nature of the way the values will change with change in width of the conductor tracks or the spacing between the tracks.

Now, in this class we will try to see how these non-idealities will affect the performance of the circuit and how we can go about avoiding these problems to some extent.

You should note that many of these problems have many degrees of freedom in the sense that uncertainties due to many issues - like you could have a neighboring equipment which is having high power high frequency and inducing interferences onto loops which is there on one PCB. So, the neighborhood is important, the power levels are important, the way you route the power and supply grounds are important; so, there are too many possibilities and too many uncertainties. Therefore, what can be done is try to follow some guidelines. You will still have these problems, but the number of iterations will reduce and thereby as you go along, when you learn more and more about these aspects, the turnaround time for making the printed wiring boards will keep decreasing.

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In that view point, you should take many of these solutions that will be discussed in this class. To start with, let us discuss something about some Layout Guidelines. If you are making a printed wiring board, the first thing that you will do is have a Circuit Schematic. The Circuit Schematic is the culmination of your paper design exercise. You would have thoroughly analyzed the circuit design. The circuit on paper may be even simulated the circuit and after having done that, you have frozen the circuit and the values of the various components, and that circuit which you have now reasonably finalized, would be the one that you will be putting it as Circuit Schematic for making the printed wiring board. The schematic is normally entered through a schematic entry package - like one of one of them would be here gEDA, open source EDA. You have OrCAD cadence tools and many other tools which can be used for taking the schematic.

After you have taken in the schematic, you will have to give the physical dimensions to components. You need to fix these physical dimensions by way of footprints or footprint symbols. Footprints basically map the electronic symbol or a electrical symbol to a physical symbol that is the told. The map, probably an orphan, which has the electronic symbol into the electrical symbol containing probably dual in line package or an SMD package one of these which has the leads coming out of the integrated circuit package.

After giving the physical dimension by way of footprints, you need to layout. That is, you will have to position the components onto a rectangular grid which would measure up to the real PCB or printed wiring board dimensions. While we are at the layout, you should mention that the printed wiring board dimensions will actually come from the application. So, you should be pretty clear where this particular printed wiring board is going to be applied or where it will be ultimately mounted; may be it would be mounted in the 19 inch rack or it may be mounted on to a custom enclosure or it could be an extrude enclosure. All these details, the designer of the printed wiring board should discuss with physical equipment designer and they should be a close collaboration at this stage before deciding the size of the printed wiring board, the overall dimension of the printed wiring board. Within these dimensions, the layout of your circuit components should be made. Then post the layout.

After the layout, comes the routing stage. You will now route the component connections; that is, you have the components which are placed on the printed wiring board within the dimensions of the proposed printed wiring board. The various connections or the tracks that needs to be laid out from e one component lead to another component lead are actually the information taken from the circuit schematic part transferred on to the layout and routing part of the package. So, the routing can be done manually or auto routing, but we generally recommend that you do the routing manually to actually fix many of the problems.

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And then of course, you will be generating the necessary files called the gerber files which will go for the fabrication of the printed wiring board. Let us discuss something about this aspect, the layout aspect - the layout guidelines which can have a bearing on your routing and the issues that we have been discussing till now that is the parasitics,

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So, when we come to the layout guidelines, the first aspect that I feel that a good printed wiring board designer should address is the overall dimensions of PWB - printed wiring board - or printed circuit board - PCB. Here, it is important for the designer to address the issues of the adjust; take for example, the board here. If you can see the board here, you see that this particular board is resting inside the card guide, which slides in and out like that. You should be able to see here; the adjust - at this point the card guide and that is where the PCB slides in at this point. I think it is clear to you. These card guides may be metal or nonmetallic, but one important thing about this card guide is that you should not have any components for that space of 2 mm or so such that all the space here and so also on that side, so also on this side where you are going to have card guide that amount of space about 2 mm should be clear; should not have any track routing on these edges. Utmost, if it is not possible to manage, you could utmost have ground track which is going on these edges otherwise it is advisable not to have any tracks.

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There is also another issue of mounting holes card guide space and mounting holes. You need to address this space also right at the beginning. For example, if you take a board like this. This is in that various stage of fabrication not yet completed but, in the process of getting fabricated. You see these holes here. These are the mounting holes. The PCBs dimensions are marked at these rectangles. It will be cut to size and these mounting holes should be pre fixed before you do any layout and routing.

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Then, fourth point is the connectors. You should take care of the position of the connectors right at the beginning. Look at these. You see the connectors here the d type connector and few terminal mount connectors here and you have connectors on this side. Look at the connectors placed here you have the connectors another d type connector. These occupy quite some amount of space in your printed wiring board and these are the external links from the PCB or this is where the internal circuit gets link to the external ward. So, the connectors should be placed according to how the external links are, where it connects is decided; so, this is where some amount of discussion with the physical equipment designer also matters a lot.

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Only after you have finished placing all these, you go on to the layout of the components. You have to layout the components in the order of criticality. So, when you layout the components, you do not have a formula for this; it is intricate. You will learn more and more as you make more and more PCBs, criticality of the components sensitivity to various issues like values of the parasitics, shorted interconnection distance or length. These are some of the issues that will determine how you go about placing the components.

In general, most of the time we would like to have very short interconnection lengths fact lengths so that is our primary motive but, sometimes we may not be able to establish that for all the components, so, you may have to make some iterations here.

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Routing Supply and Ground  $J_{SUPPV} > W_{SISNAU}$ 

And after you place the components, you go towards routing. When you are routing the tracks, you route first the supply and ground. These are very important. In fact, the functioning of your entire printed wiring board depends upon the stability of both these supply and ground. This is in fact the most crucial part of your design. If you can make your ground and supply  $V_{cc}$  very stable, then you are on the route to a very successful printed wiring board design and fabrication. So, most of the effort goes into trying to make your grounds as good as possible. One of the generic rules is the width W of the ground conductors should be greater than the width of the supply tracks; which of course, should be greater than the width of your actual signal tracks.

This is important in the sense that you saw that we want to have very low impedance between the supply and the ground, large capacitance between supply and ground so that it is able to supply these spiky currents of the digital circuits such that you have distributed decoupling capacitor already running along the printed wiring board.

There are many ways in which one can have the supply and ground interconnected on the printed wiring boards. But, it is recommended that you have supply and ground on two different layers - supply on layer 1 or say for example, top layer if it is a two sided board ground on layer 2 or bottom layer for the two sided board. If it is a four sided board, then you can dedicate one intermediate layer for ground, one layer for supply, and two layers for the signals. But, in a two sided board, they are very difficult to strict to this rule but, however majority of the tracks can be made to adhere to this rule. You can have, let us say the supply lines going horizontal and the ground lines could go vertical and so on; so that you have a crisscross fashion and you connect the interconnection easily. Two possible ways I will show which are normally used in the design of the double sided boards. Probably it may be help for you to start off and from there you iterate and then may be make your own innovations.

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Let us say that we have components laid out in this fashion. It could be integrated circuits ICs or it could be analog components or it could be discrete components - any of them. Let us say we have a matrix of components, which are laid out like this. Let us say one of the lines could be the supply lines. Let us say we have the supply connecter pin here, ground connecter pin here, you could you could go in this fashion. Take the ground you could route the ground like this.

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So, you have a possibility of contacting every component for a possible ground wire. Of course, maintaining the ground wire as thick as possible. I am not showing the thickness to scale but, imagine that you have something like that or even thicker something like this. Then you have the supply line  $V_{cc}$  line, which goes in like that and goes horizontal right through like that and then of course, there is thickness associated with all these I am not showing it here so that I do not clutter up the page. You maintain the rule that we said before. The rule of ground conductor width much greater than supply much greater

than signal you can overlap them here to get better capacitance ground to supply capacitance.

This is one way of routing, where you have made available the supply and the ground plane to each of the components. Here you see that the supply, the red line - this is in top layer let us say, this is  $V_{cc}$  and the ground in the bottom layer.

Now by trying to keep majority of the ground and the supply here in this zone, you can make the ground very thick ground as thick and then the supply on the top layer to overlap on the thick ground layer so that you can try to have a good level of distributed capacitance at this portion; so that each of these lengths will have some capacitive impedance here to supply the spiky currents.

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This is one type of ground routing, which is very common. There is another type of ground routing, which is also pretty common especially for the two sided boards. Let me illustrate: let us say we have some components placed like this some of them here and now these components like before could be digital, analog, discreet components any of them but, they all require ground and supply connection for them to operate. Let us say somewhere here we have  $V_{cc}$  connecter and then you now have the ground connecter. Let us say from the thick ground line, you take out these two lines and goes right through on both sides in the edge of the printed wiring board and then you have the  $V_{cc}$  of the supply line slightly thinner than the ground but, overlapping I am not able to show

overlap here but, what I am trying to indicate is make overlapping and on the other layer if ground is on the bottom layer, the red or the  $V_{cc}$  is on the top layer.

We take the  $V_{\rm cc}$  interconnection right through underneath the components like this and likewise you could have ground layer on the bottom side or on the top side. Depending upon how the routes merge, you could directly connect them as such or you could connect them and then pass it through a PTH plated through a hole. This is also fine. You could do that either from the ground or from the supply. This way you have again connection to all the ground and supply connection to all the components. Notice that the ground and supply lines are going together parallel so that you are maintaining a capacitance for every centimeter run of the track length and thereby having a good distributed capacitance.

Of course, for the case of multilayered boards, you are dedicating one full layer for ground and one full layer for the supply and thereby you could have much better capacitances than before. When you do the design, let me show you here, in this particular PCB, you see that all the remaining spaces in the board are filled up with copper of course, this is tinned copper. All these remaining spaces are filled up with copper and then connected to the ground, then your ground becomes very stable. So, it is always a good practice to fill up the empty spaces with copper and then to connect them to the ground. By this, what happens is that for electromagnetic field to interfere it is much more difficult and then you have a good ground to signal capacitance but, very high impedance for the electromagnetic in different aspect. Do not disturb the ground plane that much.

That is one important part. After you have a full a decided the ground and supply lines, then you go for routing the signal lines and that of course depends upon the various components and the circuit you will have to iterate a bit on that and try to stay within these ground lines and connect them to with as short as possible distance that you can with the available area there and spacing.

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This is one aspect. Another important aspect while we are on the ground is that on a single board you could have both analog and digital circuit. Let us say, if this is the printed wiring board dimensions, you have the mounting hole here and somewhere here Let us say you have the connecters and let me indicate two of the connecters important ones. Let us see  $V_{cc}$  and let us say you have a ground. Whenever you have both digital and analog parts in the PCB, you have to separate them into two parts all the analog part you place them to one side of the PCB do not mix them except at the final stage. All these analog parts will have a ground and let us say you bring all the grounds, star them at one point, and bring them here to the connecter. Then, let us say you have all the digital parts I am just indicating by some gates now all the digital circuits could be ICs or it could be discrete ICs or microcontroller processers, all the grounds connects of the digital part bring it separately to this point. Do not connect any of the digital part of this ground. The grounds of the digital part do not connect them on the PCB at all to the analog part of the ground here.

You have an analog ground, this is called the analog ground and this is called digital ground and these two grounds are not mixed. You need to connect it at the most stable point which is at the entry point to the PCB or further out.

Now at this point, you see that all the digital current spikes will flow only in these parts of the line and get to this point. They are no way going to flow in the analog part of the ground and disturb the sensitive analog circuit Analog circuits are very sensitive to ground instability and you can have a very quick deterioration in the performance if you make connections of the digital and analog grounds weak in the PCB. Utmost, you can connect it here at this point but, connect it at if the power supply is actually still further, power supply board still further somewhere here you can connect it at that point, if that is the most stable ground reference in your whole system. So, this is the very important aspect you have to split up the analog and the digital ground I keep saying that repeatedly because this one common mistake which people do and forget and then later on it can cause the real havoc if you have the spiky currents flowing through the analog systems because the power supply rejection for very high frequency is not so good and it could corrupt the outputs of the analog circuits.

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These are some tips for good layout and design routing. We shall discuss one more problem, which is the major issue in printed wiring boards and that is called Reflections. You may have heard of reflection, you may have heard of transmission lines. If you take the case of high speed digital circuits you will see that most of them have wave shapes something like this, pulses square and all these type of circuits have a high frequency part even though your clock frequency may be low; this part is a very high frequency and this has lot of harmonics which can go to megahertz and gigahertz ranges. So, if you see the rise time, the one which I am drawing here, the rise time going from low to high is a very high frequency and if you say that rise time is  $t_r$ , the rise time. It is the time taken for the voltage waveform to rise from 10 percent of the value to 90 percent of the value. That is from 10 percent down here to 90 percent up, that is generally defined as the rise time and that is a very small number of the order of nano seconds.



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If you consider the bandwidth of the system, the bandwidth of the system is related to this rise time. This bandwidth of the system is related to this. It is generally of the order of magnitude is given by 0.35 divided by  $t_r$  the rise time, T this can be in thousands, it could be megahertz and gigahertz, a very high number. When you have frequencies of that order of magnitude, then you will see that the waves propagate at the wavelengths and the propagations of the waves at every track. If I take the track that is a signal and a ground you take a signal track and the ground and if you have some source here you will see that the frequency is so high that the wave propagation from here to here and then back here is of the order of the rise time of the signal.

Normally in low frequencies signal, the wave propagation is so fast compare to the rise time of the signal. Normally we do not consider these effects but, when you consider that the wave propagation is of the order of the magnitude corresponding to the rise time of the signal, then you will have a reflection effects, the voltages are not what we expect. These can cause overshoots and undershoots and probably trigger the signal when we do not want it to trigger a particular digital state when we do not want to do that. Therefore, this effect will come under the analysis or what we call the transmission lines transmission lines and transmission line effects where we do study the reflections due to differential impedance matching, where we do not have impedance matching.

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So, it is good to have an idea of what is happening due to the reflection at high frequency circuits, so that we may take some corrective measures at least. So, let us now look at this problem called the reflection problem, which is very predominant in high frequency circuits and it is a real trouble in most of today's high clock and high pitching rate digital signals. On the slideshow here, let us see the problem of reflection. Let us see what happens to two ends of a transmission line when a constant voltage signal is suddenly imposed at the source end. Let us take two tracks. This is a signal track and this is let us say the return track or the ground track. These two tracks here and this is the source end and is the ground end. Let us say that the wave impedance is related to square root of l by c. When I say wave impedance, just the moment of diversion here, Z the impedance is given as L by C where L is the inductance per unit length C the pico farads per unit length square root of that. This would approximately give you the wave impedance at w or  $Z_0$  of that particular transmission line and it is a character of that transmission line because it is a made up of the coupling capacity here and the per unit inductance value which are basically characters of those two lines.

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So, this is the characteristics impedance of the transmission line generally given in this form if the resistive part is negligible. Getting back to the slide, seen from this source end, we see wave impedance  $Z_0$ , and seeing from the load end we see also a wave impedance which is again another  $Z_0$ . Now  $Z_0$  is the function of R L and C that we have seen before when we had been discussing the parasetics R L and C and on the source side we will call the voltage here  $V_i$  and on the load side let us call it as the voltage  $V_0$ . On the source side we have a source connected in this fashion now let us say we have a source with its source resistance  $R_s$ , so,  $V_s$  and  $R_s$  of the source resistance and on the load side we have load  $R_0$  connected as shown here. Now this is the transmission line situation where if we give high frequency as step input 0 to some voltage here. That

voltage will come to this point  $V_i$  point at this node it will go through the transmission line and part of it will they also get reflected back again.

So, this will go forward and at this point, load side reflects back and then once it comes back, it can get reflected multiple times. Now at this boundary, when it gets reflected we have a coefficient called the reflection coefficient, the amount that will get reflected or sent back again, that is given by rho $<sub>0</sub>$  the output side or the load side reflection</sub> coefficient  $R_0$  minus  $Z_0$  divided by  $R_0$  plus  $Z_0$ . Look at this, here the numerator  $R_0$  minus  $Z<sub>0</sub>$  if the load and the transmission line characteristic impedance they both are matched; if  $R_0$  equals  $Z_0$  then there is no reflection. The reflection coefficient becomes zero, so, impedance matching becomes very crucial when you are talking of transmission line effects and high frequency issues.

Likewise, as I was saying, the signal that is reflected back from this side can get re reflected once again reflected back from the source side hence so on can keep happening and the coefficient of reflection at this side is called rho<sub>s</sub> and it is given by  $R_s$  minus  $Z_0$ Note here that  $R_s$  and  $Z_0$ , if they are not matched then you will a reflection coefficient else if they are matched if  $R_s$  and  $Z_0$  are matched  $R_s$  minus  $Z_0$  will be zero and you will not have a reflection.

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**REFLECTION PROBLEM**  
\n**R<sub>o</sub> = 300 ohms Z<sub>o</sub> = 50 ohms**  
\n**R<sub>s</sub> = 25 ohms V<sub>s</sub> = 3.6V (TTL)**  
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$$
\rho_o = \left(\frac{R_o - Z_o}{R_o + Z_o}\right) = 0.71
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\rho_s = \left(\frac{R_s - Z_o}{R_s + Z_o}\right) = -0.33
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$$
V_i = \left(\frac{Z_o}{R_s + Z_o}\right) \cdot V_s = \left(\frac{50}{50 + 25}\right) \cdot 3.6 = 2.4V
$$

Now let us take a practical problem. Let us say  $R_0$  is 300 ohms that is on the load side we are terminating it with 300 ohms, we have a source which has a internal resistance of 25 ohms series and let us say 50 ohms is the characteristic or the wave impedance of the tracks. The transmission line, which is nothing but, square root of inductance per unit length by capacitance per unit length. Now on the source side let us give a TTL compatible voltage let us a 3.6 volts and if you use these values and calculate the reflection coefficient on the output side, you will get the reflection coefficient to be 0.71 for these values and on the source side  $R_0$  being less than  $Z_0$  you will get a negative value minus 0.33 as a reflection coefficient.

Then  $V_i$  is nothing but,  $Z_0$  divided by  $R_s$  plus  $Z_0$ . It is the attenuation ratio into  $V_s$  which is nothing but 2.4 volts. In the final analysis at the output  $V_0$  we would get 300 divided by  $R_s$  plus 300  $R_0$  divided by  $R_s$  plus  $R_0$  that would be the ratio that we would ultimately get at the output side.

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Now, let us see what happens taking it to account, the reflection. Let us say we want to see a graph versus time of  $V_i$  the source side of the transmission line and another graph here verses time of the output side  $V_0$  side. Now on the source side, let us say we have the grid and this grid is now split as 1T 2T 3T 4T 5T so on. This 1T is the time taken for the wave to propagate from the source side to the load side. It is the wave propagation time one way from the source to the load and most of the electro electromagnetic waves propagate add 3 into 10 to the power of 8 meters per second but, there is a issue of dielectric we have a dielectric medium and due to that it may be slightly different from 3 into 10 to the power of 8 meters per second and on the load side also let us say we split up the time axis as one 1T 2T 3T 4T where T represents one wave propagation delay time from the source to the load or from the load to the source.

Now, final settling value of the output is 3.232 volts that is if you provide at the input 3.6 volt TTL compatible as we saw in the previous slide we should get at the output 3.32 volts immediately because we have an output of 300 ohms termination on the source impedance of 25 ohms if there were no transmission line effects, it would have been 300 divided by 300 plus 25. 300 by 325 which will give you voltage value at 3.32 which would immediately settled to this value. Let us say what happens due to transmission line effects of the reflection problem. Let us say we have a one boundary on the source side another boundary on the load side; on this boundary we have a reflection coefficient of minus 0.33 as we calculated before and on this boundary we have a reflection coefficient of 0.71 again calculated like before.

Now 2.4 volts is coming at  $V_i$  if you apply 3.6 volts 50 ohms divided by 50 plus 25, 2.4 volts comes here and that is at zero time  $\frac{1}{\pi}$  and after 1T one propagation time has elapsed,2.4 volts has passed on to the output side. The moment it has reached the output side the output load and the transmission line impedance wave impedance do not match. Therefore, the portion of it will get reflected and we show that there is the reflection and multiplied by the reflection coefficient. Look here 2.4 multiplied by the reflection coefficient of 0.71 will be 1.7 volts that is getting reflected and reaching here and it reaches here at 2T and this 1.7 volts which has the reached here has reached this boundary, the source side and the wave impedance do not match. Therefore, it further gets re reflected but, now both the reflected coefficient rhos which is the source side reflection coefficient so 1.7 into rho<sub>s</sub> will give you rho<sub>s</sub> was minus 3.33 it becomes minus 0.56 now that is reaching at 3T at this point.

At this point again, it gets reflected, because of this, reflection coefficient gets multiplied minus  $0.56$  into rho<sub>0</sub> which is minus  $0.4$  and then this further gets reflected here minus  $4$ into rhos as minus 0.313 and reaches here at 5T and so on; it keeps going. So, you see that finally, it keeps going decreasing ultimately it will go to zero exponentially as into vertically.

Now, at every point of this reflection, you have 2.4 reaching here and 1.4 which is going out at this node point. Voltage at this load side will be whatever is arriving and whatever is leaving. It is an algebraic sum so the value that you will expect to see here is 2.4 plus 1.7 and that is the value that you will see here which is 4.1 volts.

Now, 1.7 volt out of it is travelling here, so, it has reached here after 2T so after 2T, 2.4 was already there here plus 1.7 minus a 0.56 algebraic sum is whatever is arriving and whatever is leaving is 3.54 so that gets added on to what is previously existing and comes here and then minus 0.56 are arriving at this point and this port what was the existing was 4.1 minus whatever is arriving here and what is leaving here you get the algebraic sum which is 3.14. 4.1 minus 0.96, so, it goes down into 3.14, the voltage here and what arrives here is minus 0.4 and what leaves is plus 0.13 so algebraic sum of this and added to the previous value of 3.54 will give you 3.57 so that is the value which will we see on the scope here and that value at 5T will reach almost 3.36 and then further on you will see that it will gradually tend towards 3.332 volts so you see that you do not immediately get 3.32 volts, it gradually starts moving has overshoots and undershoots and most to 3.32 volts.

Now, this is a serious problem because, if the overshoots are significant or the undershoots is significant, it could switch off the subsequent stage. You could have a bouncing affects you could have a double bouncing effects because of all these reflection problems let us say if this had gone sufficiently down then you could see that the output stage circuitry would go low rather than go high and then once again when it comes back it will go high so you will have a double pulsing and malfunctioning of the circuit so this is one of the serious problem with reflections.

These are in effect the major problems that you will come across when you see when you use printed wiring boar. The problem of parasitics like finite track resistance, finite capacitance, finite and distributed inductances and the problem of reflection at high speed circuits now all these combine together to cause lot of problems when you are doing the printed circuit boards and we recommend that you follow the guidelines that were illustrated in the layout routing rules so that you reduce the iteration number of iteration towards making a better printed wiring board. Thank you for now.