

An Introduction to Electronics Systems Packaging

Prof. L. Umanand

Department of Electronic Systems Engineering

Indian Institute of Science, Bangalore

Module No. # 04

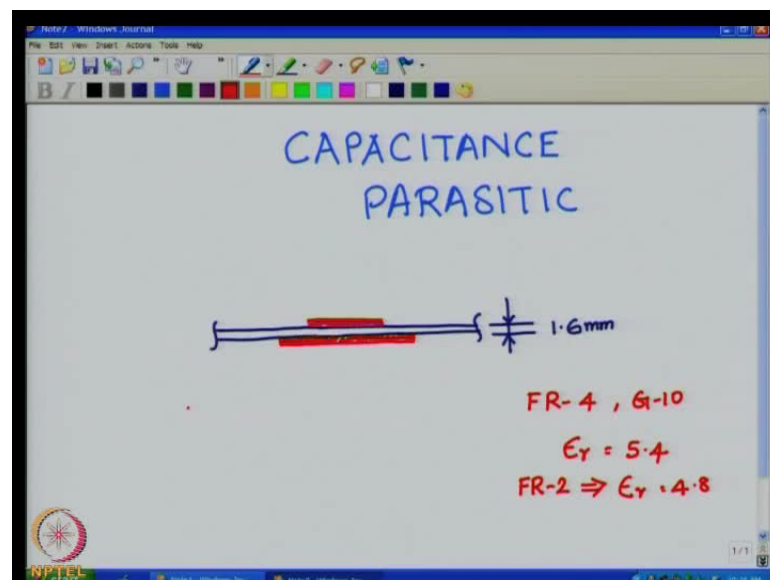
Lecture No. # 16

Electrical Issues – II

Capacitive and Inductive Parasitic

Good day to all of you! In this class we will continue from the previous class where we were discussing on the parasitics present in the printed wiring boards. In the last class we had some discussion on the resistive parasitic that is, what is the track resistance or what are its effects and how we go about estimating the track resistance.

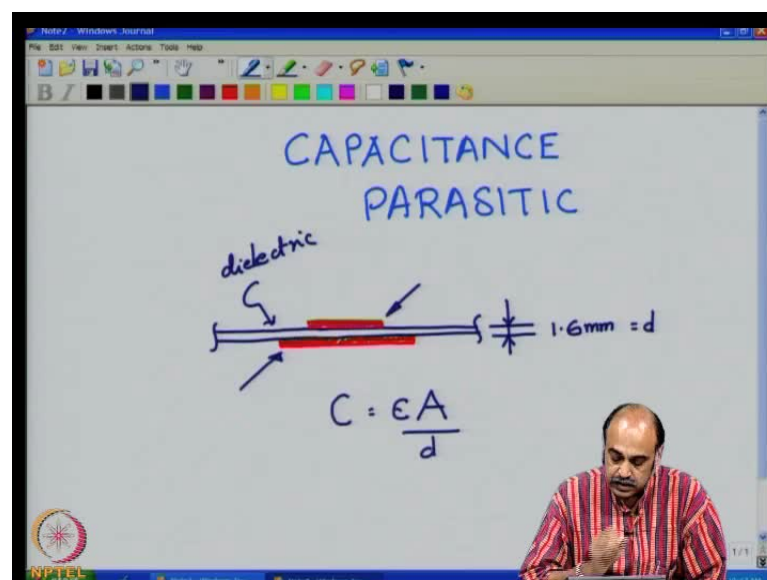
(Refer Slide Time: 01:07)



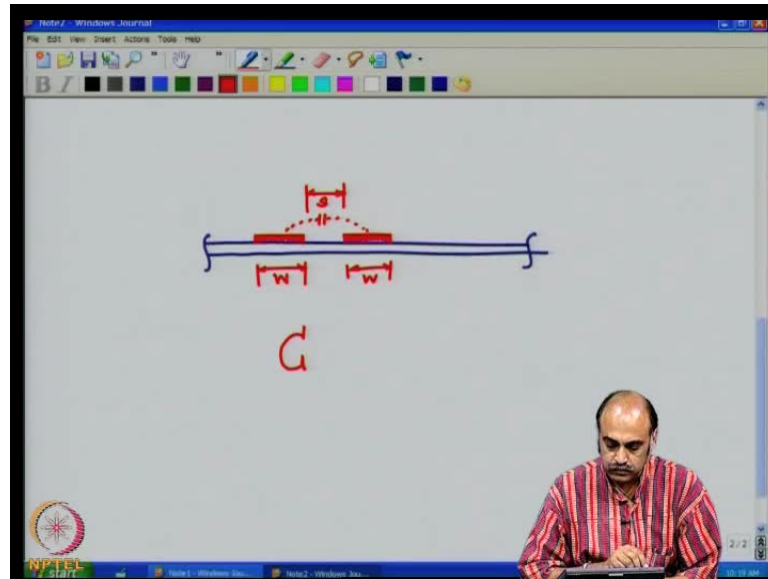
Today, we shall continue and try to understand how the parasitics like capacitance and inductance also come into the picture and have a bearing on the operation of the circuits. Coming to the Capacitance Parasitic, let us start with the discussion on the capacitance parasitic component on the printed wiring board and how it is going to have an effect on the operation of the circuits. If you consider the printed wiring board of some thickness and we know the thickness of the printed wiring boards in most cases will be around 1.6 mm and you have the copper tracks which are placed on both the layers; both the sides, top and bottom.

Let us say we have a copper track on the top layer and let us say we have a copper track on the other layer, the bottom layer; it is a doubled sided PCB. Now, these copper tracks are separated by only this dielectric component which is the PCB material, which is an epoxy material, which has a finite dielectric strength. It is called conspermitivity. The dielectric constants are different for different materials and for the most of the printed wiring board materials, for example, these FR-4 type or even the G-10 type of boards, you have an ϵ_r , this is called the relative dielectric constant of the order of around 5.4 and if it is FR-2 type of board FR-2, FR-3 type of board, you have an ϵ_r or relative dielectric constant of around 4.8.

(Refer Slide Time: 04:07)



(Refer Slide Time: 05:13)



So, it will vary from board material to board material, but they are the order of magnitude that you would come to experience with the most common boards. This copper track here and this copper track here, separated by this dielectric of some known relative permittivity, we can estimate the capacitance C ; because they now act as two parallel plate capacitances, ϵ the dielectric constant A by d ; where A is the overlapping area and d is the distance, which is in most cases 1.6 mm. So, this is one way of having capacitance in the printed wiring boards. You could also have capacitances on the same side this is the printed wiring board (Refer Slide Time:05:27) you could have a conductor with some track width let us say W and you could have another conductor carrying another signal, having some track width let us say same W , with some spacing S . This is slightly more complex because you could have tracks on the bottom side and then the length of the track need not be always parallel, could vary, and there are many other issues uncertainties which will come in here, because here also you can estimate the capacitance, which occurs between these two tracks.

(Refer Slide Time: 06:49)

CAPACITANCE PARASITIC

dielectric

$C = \frac{\epsilon A}{d}$

1.6mm = d

(Refer Slide Time: 07:02).

Adjacent tracks

G

(Refer Slide Time: 07:25)

CAPACITANCE BETWEEN ADJACENT CONDUCTORS

Coupling Capacity

$$pF/cm = 0.122 \cdot \frac{t}{s} + 0.0905 (1 + \epsilon_r) \cdot a$$

Where $a = \log \left(1 + \frac{2w}{s} + 2\sqrt{\frac{w}{s}} + \frac{w^2}{200} \right)$

- 1 s = dist. between two adjacent conductors, mm
- 2 t = laminate thickness, mm
- 3 w = conductor width, mm

NPTEL

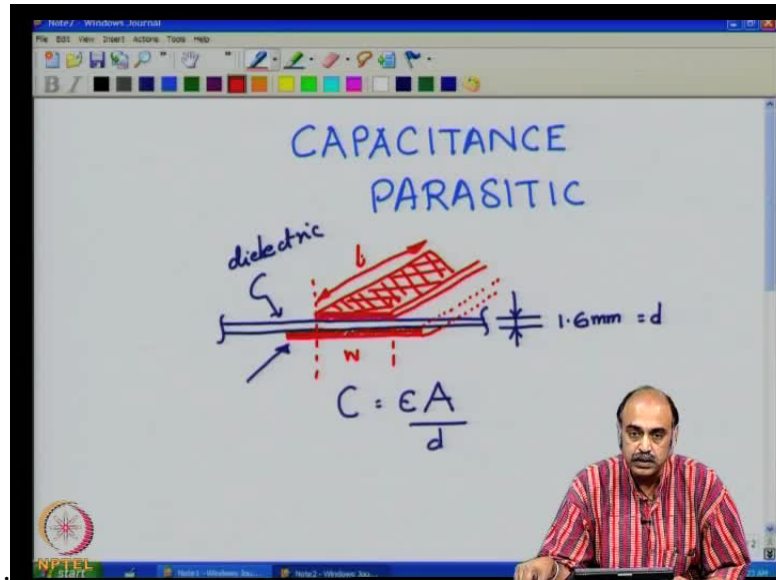
.Let us now see first, how we go about estimating the capacitance and then have a discussion on the effects of capacitance in the circuits. First let us consider capacitance of two conductors on opposite sides of the board; then we shall come to capacitances which are on adjacent tracks. Coming to the capacitance between conductors on opposite sides of the PCB, let us first find an estimate of C and we just now saw the formula it is given by epsilon A and by b, here the various symbols will be indicated now what it means the capacitance here is the expressed as pF.

You see here, that there is a constant multiplication factor 8.86 into epsilon_r, this is actually epsilon₀ into epsilon_r, epsilon₀ is the absolute the electric constant, absolute permittivity which is around 8.854 into 10 power minus 12, now the 10 power minus 12 portion is taken out here and the capacitance expressed as pF. You have epsilon_r which is the relative dielectric constant which varies from material to material you will have to find it from the science tables or the manufactures data sheet.

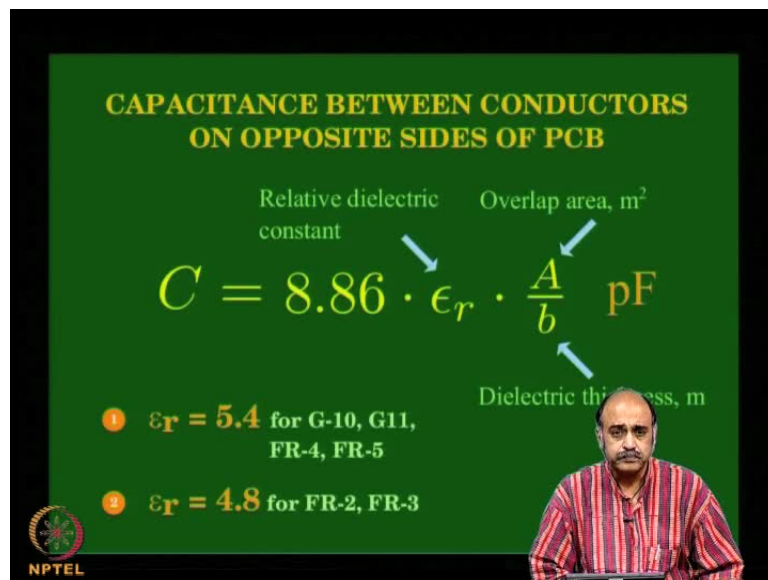
b is the dielectric thickness. Dielectric thickness, we are expressing it meters. The dielectric thickness is more or less fixed when you are talking of capacitance between conductors on opposite side of the PCB, because the dielectric is the PCB itself, the laminated self and the thickness is more or less fixed in most of the common PCB which is 1.6 mm. The next variable here you see is A, upper case A, overlap area in

meter square. Overlap area is basically the common area between the two tracks if you see you have a track on the upper layer and a track on the bottom layer

(Refer Slide Time: 10:06)



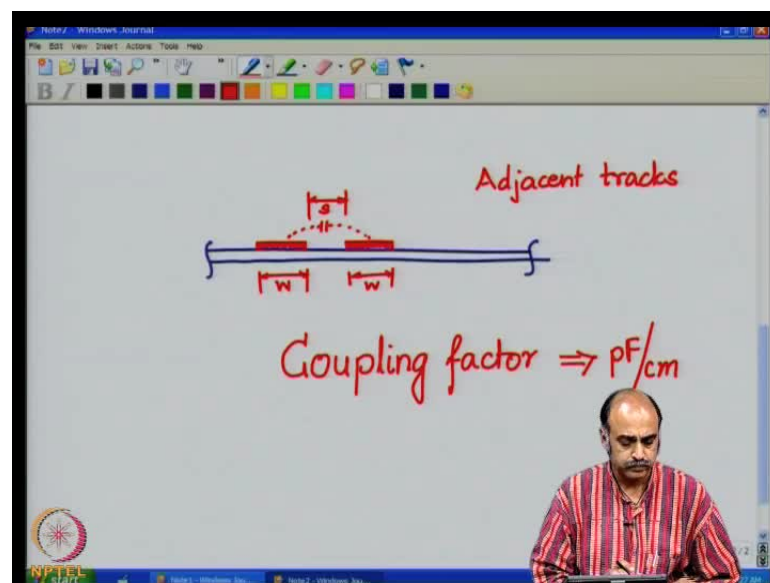
(Refer Slide Time: 11:42)



So, if I come back to my white board here, you see that on this you have a track on the upper layer, which goes like this and the track on the bottom layer, which goes dotted as I am showing here. Now, this is the smaller of the track and therefore, this area to whatever length is the area that is common to both the tracks and now these two common areas are the ones which will act like the two plates of a parallel capacitance. So, you just

take these common areas and find the value of A; which would be the smaller of the width of these two tracks and if that is W and the length of the track which is L then W into L would be the common area. Coming back to our slide, you see that there is one more variable there, ϵ_r which is called the relative dielectric constant. The relative dielectric constant is something which is material dependent and it is a value 5.4 for some materials like G-10, G-11, FR-4, FR-5 which are the common laminate materials and you have a value of 4.8 for FR-2, FR-3 type of materials and for any other type of material grade you will have to find it out from the data sheet of science tables.

(Refer Slide Time: 12:57).



Now let us find out what is the capacitance between adjacent conductors. When we say adjacent conductors I would like to bring to your attention that I am meaning assignment like this. W is the width of one track and W here width of another track then you have the spacing between S then we need to find what is the capacitance. You see that you have air as the dielectric here if you see in these spaces you have the air as the dielectric and you see the distances are not constant; they keep varying and then you have the laminate material itself as the dielectric, so it is a eutectic combination and difficult to have a close form solution. However, people have come up with some empirical rules which can be used for finding the capacitance what is normally given in the empirical rules is called a factor called the coupling factor and this is expressed in pico farad per centimeter run of the track. So for every centimeter run of the track, you will have so much p F resulting due to this particular position of the tracks, the adjacent tracks. So this is an empirical

relationship and let me give you the empirical relationship with its various symbols that is generally found in the literature and probably you could use it as a basis for at least getting in the nearer around the value of capacitance that you would get because of a particular routing.

(Refer Slide Time: 15:01).

CAPACITANCE BETWEEN ADJACENT CONDUCTORS

Coupling Capacity

$$pF/cm = 0.122 \cdot \frac{t}{s} + 0.0905 (1 + \epsilon_r) \cdot a$$

Where $a = \log \left(1 + \frac{2w}{s} + 2\sqrt{\frac{w}{s} + \frac{w^2}{200}} \right)$

- 1 s = dist. between two adjacent conductors, mm
- 2 t = laminate thickness, mm
- 3 w = conductor width, mm

NPTEL

Now going back to the slide, you see that the coupling factor which is expressed as pico farads per centimeter run of the track or the coupling, it is also called coupling capacity, is given by this kind of equation $0.122 \cdot \frac{t}{s} + 0.0905 (1 + \epsilon_r) \cdot a$ where you have a which is logarithmic which is the log of function which is formed from W which is the width of the track and S which is the spacing between the tracks. So, S is the distant between the two adjacent conductors given in mm and t is the laminate thickness again given in mm and we know the laminate thickness in most of the common PCB it is 35 microns or 35 micro meter and W is the conductor width in mm. These are the symbols and the empirical route. It may be tough for you to find out the relationship just by looking at this equation, so it is advisable that you put it into as a program and try to get a nomograph which will give you an idea of the capacitance varies with width and space and any other variable.

(Refer Slide Time: 17:28)

Capacitance between conductors on opposite sides of the PWB.

line width = 2 mm
Total common length = 250 mm
line width of bottom track = 4 mm

GND LINE ← → SUPPLY LINE VCC

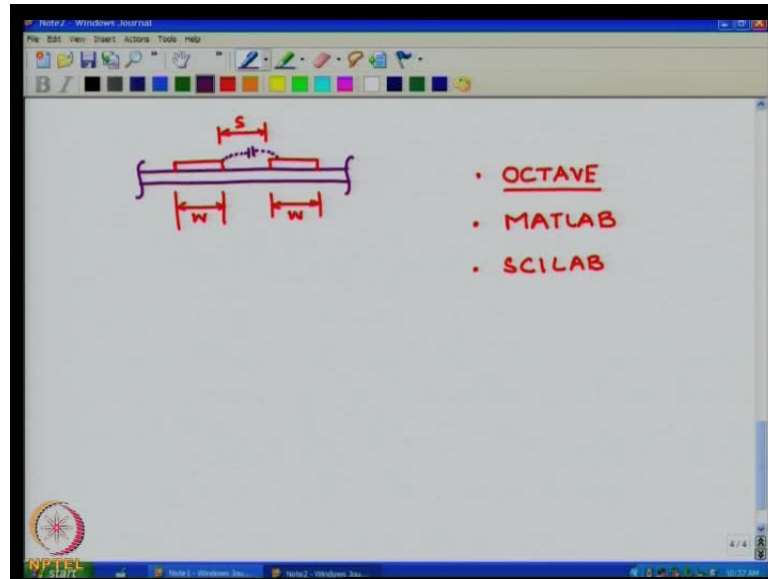
250mm
2mm
4mm
1.6mm

$$C = 8.86 \times 5.4 \times \frac{2e-3 \times 250e-3}{1.6e-3} \approx 15 \text{ pF}$$

The diagram shows a cross-section of a PCB with a 2mm wide top track (GND LINE) and a 4mm wide bottom track (SUPPLY LINE VCC). The tracks are separated by a 1.6mm dielectric thickness. The common length of the tracks is 250mm. The calculation below uses the parallel plate capacitor formula with the area of the smaller track (2mm x 250mm) and the dielectric thickness (1.6mm).

So what we shall do now is do some calculations to get an idea on the numbers; so for this, let us go back to our white board. First let us do some calculation for capacitance between conductors on opposite sides of the PCB printed circuit board or printed wiring board. Now we have seen the variables on symbols on the equations let us takes some numbers. Let us say that the two tracks have line width let us say we have a line width of 2 mm and a total common length that is the upper and bottom track have a common length of around 250 mm as an example and the width line of the bottom track is 4 mm so let us say this is our situation which would look something like this. You have a width of 2 mm a bottom track of 4 mm and you have 1.6 mm thickness and the track runs for 250 mm long so this is the situation and if you apply the formula 8.86 into 5.4 this is our ϵ_r this is our ϵ_r remember into the area now the area is nothing but this is the smaller of two tracks having a track width of 2 mm and the length of 250 on the side so we will write it as a 2 e minus 32 mm which is 2 e minus 3 meter into 250 e minus 3 meter which would give a meter square then divided by 1.6 e minus 3 is the distance the dielectric thickness so this should approximately I have pre calculate it will be around 15n pico farads pF.

(Refer Slide Time: 23:31).



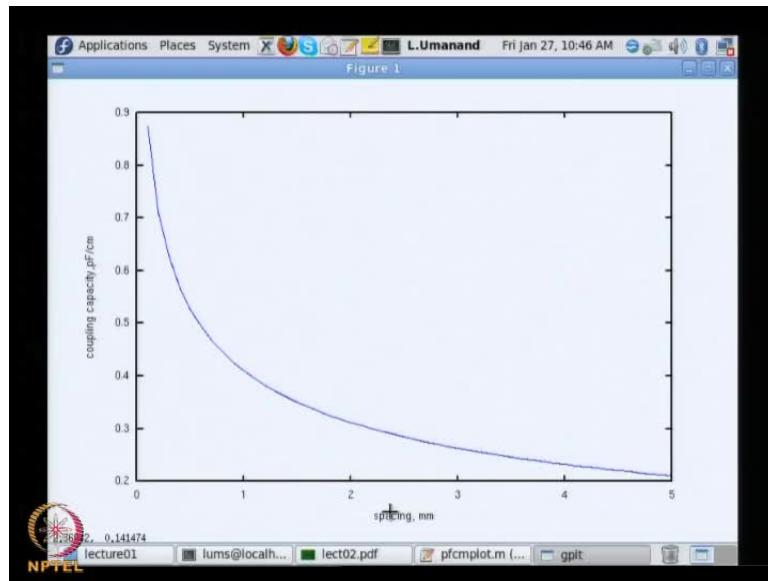
So when you are talking of tracks between the opposite sides, you see that this top track could easily be a supply line; supply line meaning the V_{cc} line and the bottom track could be a ground line. Normally the ground line is much thicker than has a greater width than the supply line and this capacitance between the supply line and ground line for these kind of specification a 2 mm supply line, 4 mm ground line for a 250 length common line you have around 15 pF. These can be used as decoupling capacitors when it is distributed, de coupling capacitors as these two lines are connected to various digital circuit loads which as like we saw in the last class the output stages of the gates being totem pole or composed of top and bottom switches, During switching transition, you have huge current spikes. So this capacitance between ground and supply is always good to have a higher value capacitance lowering the impedance such that the supply in the ground lines is more stable. Coming to the other problem of trying to estimate the capacitance between adjacent tracks, this is slightly more tricky; however what we shall do is try to estimate using a simple program and I would recommend that you also try to do that by means of a program whichever is convenient to you I am right now here going to you use an open source package called OCTAVE, you may have heard of it you could also use a MATLAB you could use another open source package called SCILAB and probably there are many more.

Right, now let me try to demonstrate to you the way the capacitance between these two tracks; our interest is the capacitance between these two tracks; some kind of a

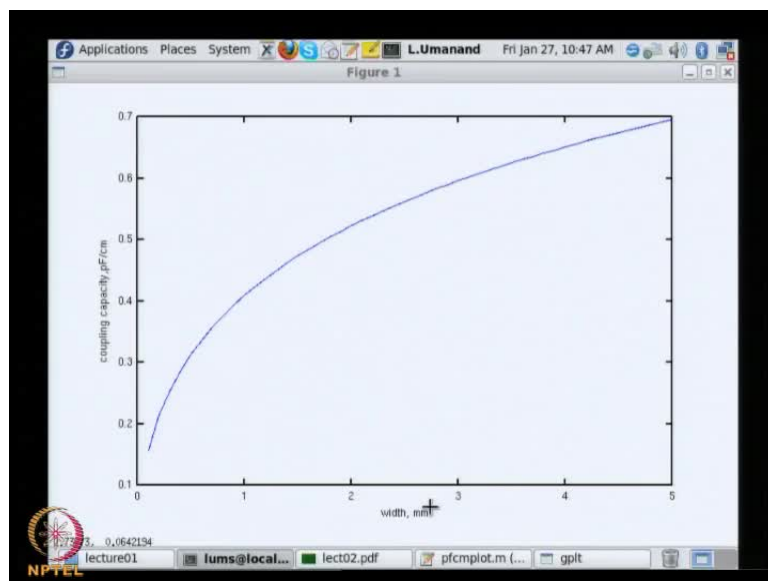
nomograph, a graph which will give as an idea of the relationship between the widths and the spacing between the conductors. Let me take up a terminal window, let me go to the octave environment and you are right now in octave environment and you are ready to execute a program. Before executing the program I would like to show you what is inside this particular function. This is a simple script file. Basically it is the same equation that I just put few moments ago. Look at this which I shall probably mark for your benefit. This is the same equation that I had been discussing $0.122 \text{ into } t \text{ dot slash } S$. Let me tell you why I am using $\text{dot slash dot plus } 0.0905 \text{ into one plus } \epsilon_r$ which is ϵ_r . Basically I have defined ϵ_r as $5.4 \text{ into } A \text{ or dot star } A$. A is nothing but here the log to base ten of function, which is consisting of the two variables W and S like given in the equation. Now W is the width which I am taking it as a 1 mm t is you could see here t is 35 mm laminate thickness and now this is something which is different I would like to see a nomograph plotted with x axis as the spacing between the conductors. What I am right now doing here is trying to get a graph with respect to the spacing S . S is nothing but values raging from 0.125 in steps of 0.1. Now S becomes an array when you are using array, I cannot do direct multiplication or division, so this dot operations this dot operations what they basically do is they try to do the operations on every element of the array. This is a scale or value W which is operating with this particular operator on every element of S .

Likewise, the multiplication and so on and then we would like to see a plot of the coupling factor or coupling capacity with the x axis being mm and the y axis being the coupling capacity in pF per centimeter; then after that we would also like to see not only with respect to s and also with respect to the width of the track W . So next time is the width of the track as vector from 0.125 with steps of 0.1 and S is just 1 mm, the spacing between the tracks of 1 mm and we apply the same two equations and then we plot. This is what we I would I want to do end of the function the function is named as $p f c m$, p f per centimeter plot so let us plot and see. Now going back to the terminal window in octave here I will call that function $p f c m$ plot. Let us see this figure.

(Refer Slide Time: 29:43)



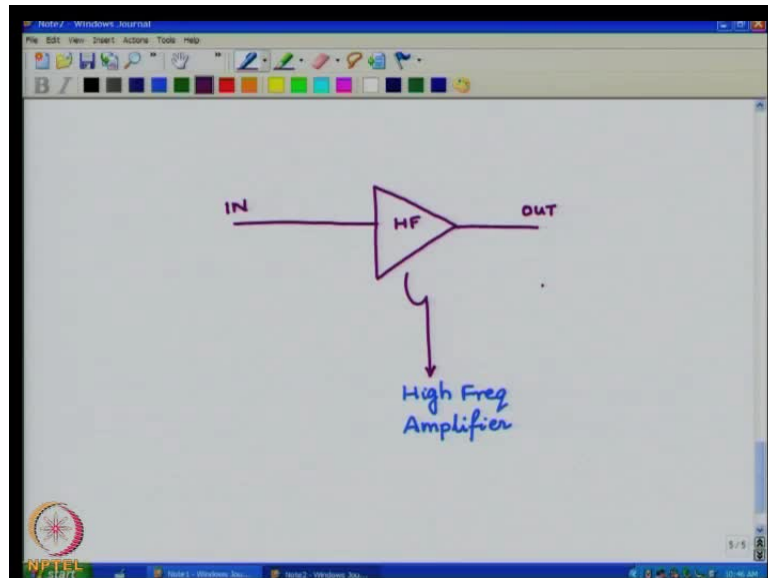
(Refer Slide Time: 30:55)



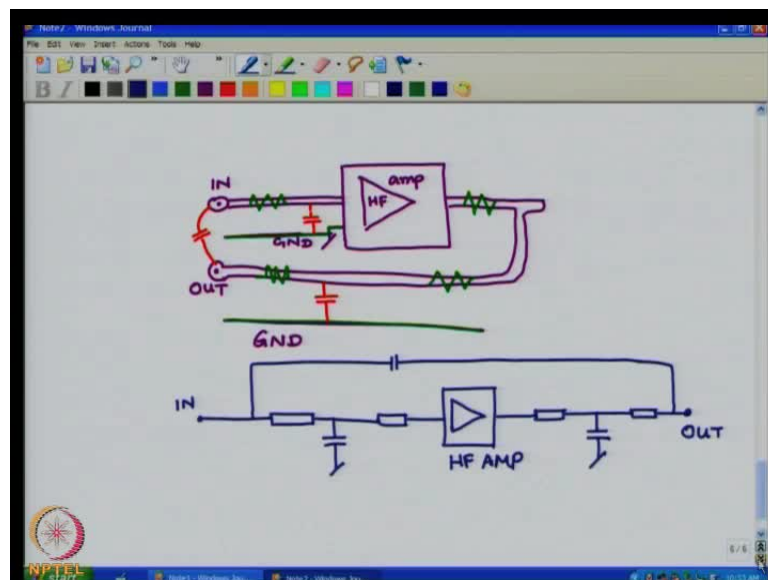
This y axis gives coupling capacity in pF per centimeter, the x axis gives you the spacing S ; remember, come back to the figure here, S is the spacing between the tracks, W is the width and we are interested in finding the capacitance between these two tracks; keep that in mind and try to look at this figure in that view point. The capacitances per centimeter, if you take 1 centimeter length you have this amount of capacitance and this capacitance is decreasing as a function of S . More the spacing, smaller the value of capacitance and that is what we expected to happen. What happens for the other? Look, there is a change now we now change the x axis to width in mm and y axis is still the

coupling capacity in pF per centimeter. As the width increases, the coupling capacity increases; so more the width higher is the coupling capacity. Therefore when you want to have ground and supply lines, let us say one layer is supply line and another layer is the ground line you try to make the coupling capacity as much as possible so that you get more capacitor or less impedance between the supply and the ground so that they are able to give much more value of spike currents when the digital circuits go through transitions.

(Refer Slide Time: 34:15)



(Refer Slide Time: 34:29).



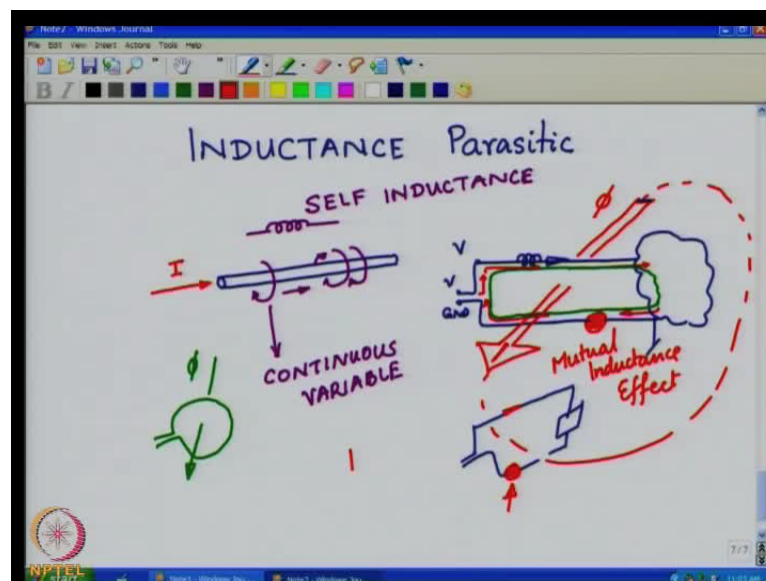
Increasing the width will give you more capacitance between the two lines. This is what we would be learning from this exercise on the capacitance. Coming back to the white board, I would like to bring to your attention that the capacitance between the lines has not only positive effects but sometimes you have both and you have negative effect also. You will have to be cautious what is going to happen when you do a particular routing. For example, see a circuit like this; Let us say you have a high frequency amplifier. This is a high frequency amplifier and to this, let us say you have some input and you have an output. I am showing this high frequency amplifier just as block with an input and an output but you should know that the input and output of a high frequency amplifier may be routed differently on the printed wiring board. For example, they could be routed like this; let us say you have the input IN and you have one route I will still continue to put the frequency amplifier in a block there may be many circuits within that. This is your HF amp and probably the route could go in this fashion.

Let us say the routing is in this fashion. Because this is an amplifier, you will have a ground point somewhere; you will have ground lines you may have ground lines here; it depends upon the routing. You could probably show the ground line in green to make a distinction. Now, this is a ground line coming from the other parts of circuit. The problem is I could have a capacitance between this track and this track; there is capacitance between the in track and the ground line here; I could have a capacitance between this output track here and the another track the ground track here so which could be something like this not only that you could also have a parasitic capacitance between these two tracks; the input track and the output track. This is the output track for you to know. When a situation is like this you consider the non-idealities. We have considered only two non-idealities; still we have discussed about them which is the resistance and the capacitance.

This has also inductive non-idealities however will come to the inductive non-ideality later but just taking these two non-idealities, you will see that you also have due to this track resistance a resistance here, you could have a resistance here, a resistance here, and here so on so effectively what would happen it would look like you have circuit wise I have IN and I have a resistance a capacitance may be resistance like that then you have your high frequency amp you have resistance capacitance and you have the output and not only that you also have a direct feed through capacitance coming to the outline

something like the similar effect a feedback kind of a capacitance- between the input and the output and this similar effect also be quite disturbing thing in the functioning. So if you see effectively this high frequency amplifier is having a low pass filter at the front end and a low pass filter at the post that is output end and then you have a similar effect capacitance coming to the picture; all because of these parasitics as you see quite dangerous parasitics so what effectively happens is that here the bandwidth of the high frequency amplifier gets limited.

(Refer Slide Time: 41:05)



It becomes because of these low pass filters the bandwidth is much limited compare to what you would actually have design. So these are some of the effects that would come into play if you are not careful; you probably would have to decrease the value of this capacitance. How does one could go about decreasing the value this capacitance? These are some of the issue that we need to have a look at probably by putting guards probably by putting in between tracks which will increase the inference between the ground which will increase the impedance between the input and output so let us see how those effects are avoided to some extent after we finish the discussion on the inductance. We will revisit the issue of capacitance and also again the issue of resistance after we have finished the third parasitic, which is the inductance and then see as a whole how we try to avoid major problems and also some set of guidelines where if we follow that the iteration will come down.

The third component, the parasitics which becomes quite important to us in dealing with circuits on printed wiring boards is that of an inductance, which is parasitic, which is a very dangerous parasitic that combined with the capacitance can cause quite a lot of havoc in the electronic circuit; what you thought you have to design for will definitely not be the same circuit when you put them into the PCB especially for high frequency signals and you should keep in mind that though the supply lines which we think are DC; you just need a DC model for the supply the ground lines but unfortunately you see that in high speed circuits and digital circuit; during transition as I have been always saying you have spiky currents and these spiky currents have rise times and these rise times are very high frequencies so actually high frequencies spiky currents flow through the ground and the supply lines and disturb the stability of the potential on the supply in the grounds and these can really cause great havoc in the high speed circuit let us see what we would like to look at in the inductance. If you have just a single conductor even if you have a single conductor with some current flowing through and let us say that current is I , by the Fleming's right hand rule, if you point the thumb in this direction and the direction in which the fingers coil around the conductor will give you the direction of the flux which is going to be around the conductor.

Any current that flows through the conductor will give you a flux around in this fashion. The flux is a continuous variable meaning it is the state variable it cannot change instantaneously. Because of the nature of the flux variable being continuous variable, the dynamics of the current is limited; because of this particular effect, if the current changes supposed to change value immediately; then that would mean immediate change in flux which nature does not permit and therefore current will not change immediately. That effect is called the inductance effect and that is what we represent by these inductors. Equivalently, when there is a flow of current, there is a flux which is setup around the conductor. There is some energy which is stored and that energy is a continuous variable and you cannot immediately remove it or immediately put energy into that one.

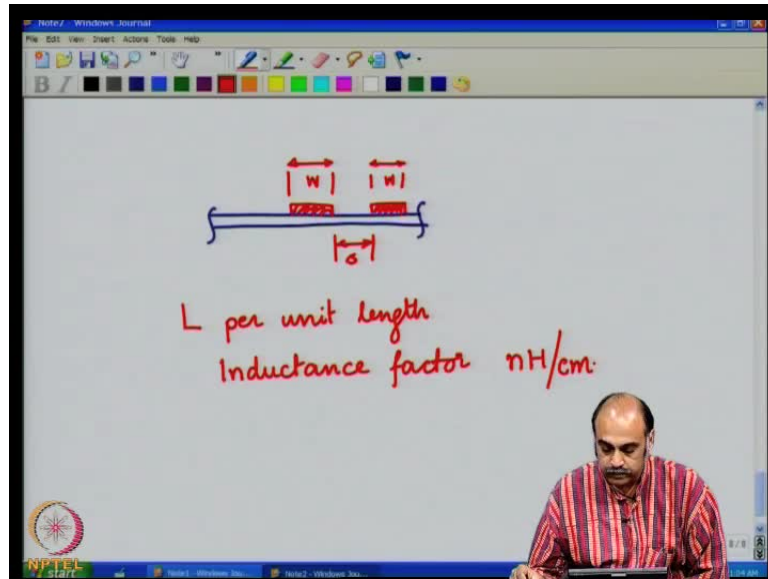
There is some dynamics involved; now this is called the self-inductance of the conductor. Self-inductance of the conductor is one such issue that you will come across. Another problem you would come across is when, let us say you have a circuit and this at a positive potential v and you have some circuit which does some job. There is a

current which flows in here and then there is a ground and this ground is coming through the tracks to some point. So let us say the track like that comes to the connector this is the ground and this is the v now if you look at just the current, the current takes off from here like that goes in this fashion goes into the circuit and does lot of operation comes out through this and back again here; so if you look at this part it is like a loop. This is a loop so if a current flows in a loop or a coil, there is a flux ϕ or b which is setup which goes perpendicular to the cross sectional face of the coil area or the coil face in this case you have the loop and therefore, you will have a flux which goes perpendicular to the face of the coil and it will go and then complete the loop from some other circuit through some other circuit or may be even free air.

Now a flux which is going through this loop would imply that the current in the loop cannot change instantaneously, which means an inductance is setup here it is a parasitic here or here all distributed but being showed lump. So an induction can be setup just by a current carrying conductor. Self inductance could also be setup by current flowing in a loop by a current going in a forward path and return path; this has not only the self inductance because of the current flowing in it, it also produces flux in a perpendicular to the face of the coil of the loop. It has dangerous consequences in the sense that if I am having another circuit here, let us say another circuit here unconnected with that probably doing some other job and it is now this flux when it goes back, it has to **all** flux or close paths it has to always reach where it started.

So this will pass through a loop of another circuit and it will induce a voltage here; proportional to the value which is there in this loop. So, current flowing here can induce a voltage in this loop or a current flowing in this loop can induce a voltage in this loop. This is called mutual inductance effect. We have the mutual inductance effect, self inductance effect, series inductance effect. All these effects can really change the way the circuit behaves when they are put on to the printed wiring boards. How do we go about estimating the value of the inductance? Let us take a simple case first of finding the value of the inductance we take just the PCB and then we consider a conductor and let us see what we need to do to get the value of inductance.

(Refer Slide Time: 50:56)



(Refer Slide Time: 54:14)

INDUCTANCE BETWEEN ADJACENT CONDUCTORS

per unit Inductance

$$nH/cm = 9.21 \cdot \log \left(\frac{s+w}{t+w} \right) + 6 - a$$

Where $a = 4 \cdot \left(\frac{s+w}{10l} + 0.0967 \cdot \left(\frac{w}{w+s} \right)^{2.082} \right)$

- 1 s = dist. between two adjacent conductors, mm
- 2 t = laminate thickness, mm
- 3 w = conductor width, mm
- 4 l = parallel run length, cm

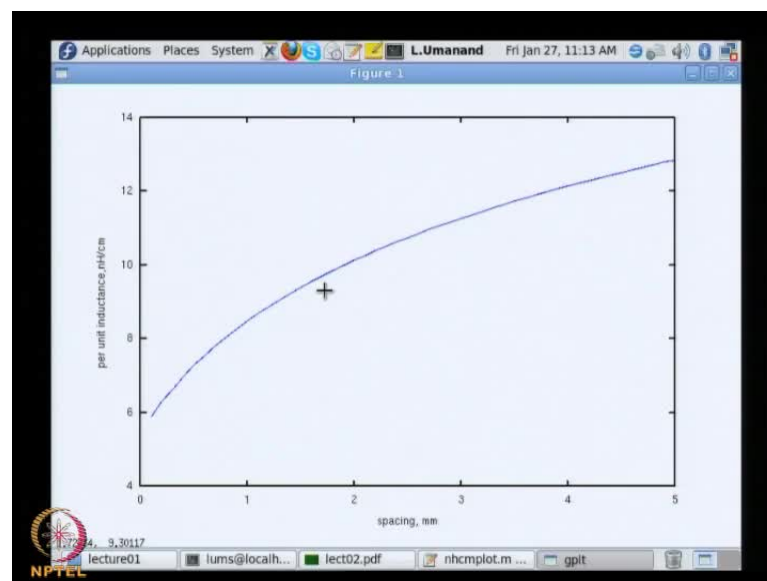
NPTEL

We have a conductor of width W; here we could also have another conductor here of width W and spacing S just like what we had written down for the capacitance. But, keep in mind that there is lot of uncertainty. This is also an empirical rule that I will be giving you now which will give L per unit length; so you can call it as an inductance factor Nano Henry per centimeter that is what we will be having. Let us go back to the slide and see how we go about estimating the inductance value so we had a left off at this point let us now look at the inductance between the adjacent conductors which is given in terms of Nano Henry per centimeter. Per unit inductance is given in terms of this

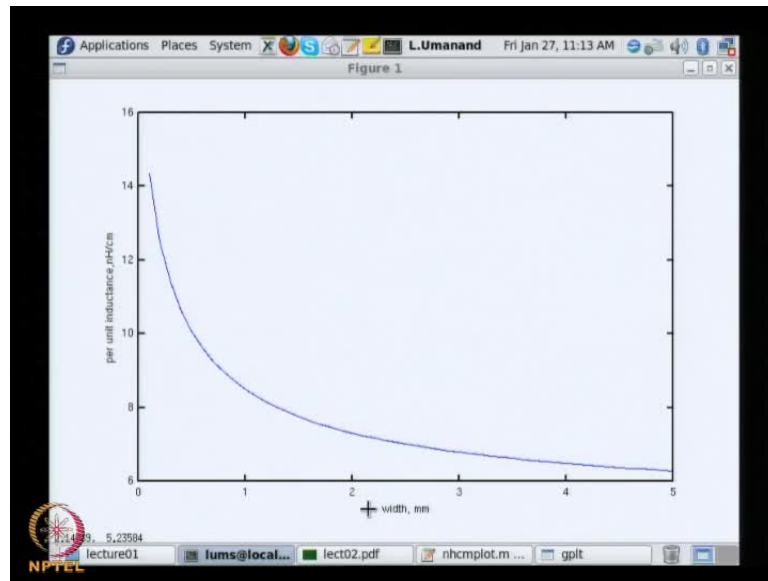
empirical relationship 9.21 into log base 10 s plus w by t by w t is the thickness of laminate plus 6 minus A where A is given by another empirical relationship like this.

Where L again is the length of the track; so the various symbols the s which is used here and here is nothing but the distance between the two adjacent conductors in mm t is the laminate thickness mm and as we know it is 35 microns for the most common laminate w is the conductor width and l is the parallel run length meaning in centimeter because we are giving it in n h per centimeter so what is the length of the conductor that you are interested in so just like we did for the capacitance I have here for you another function called Nano Henry n h c m plot wherein we want to see what is the nomograph or how does the Nano Henry per centimeter vary with the spacing between the conductor and the width of the conductors.

(Refer Slide Time: 55:54).



(Refer Slide Time: 56:52).



Just like before I have put in the two equations I put in the equations for the inductance per unit length here and I use the dot operators just like before because the first case I want to see with respect to the space giving width as one width as one mm for the track and in the other case I am giving the spacing between tracks as one mm and then you have the plots for the two figures one with respect to spacing another with respect to the width. If you execute this in octave, let me open octave and then execute Nano Henry c m plot function; we see the plot where on the x axis, you see spacing between the tracks of the conductors and here the per unit inductance in nano Henry per centimeter length see that with the spacing the inductance value is increasing so if you space the tracks more and more wide you are creating a larger and larger loop area and this larger and larger loop area results in more inductance and this has more mutual inductance capability which can link to other circuit. That is one important point you should remember. The other figure with respect to the width, you see here the width in mm and the per unit inductance Nano Henry per centimeter this is decreasing from 40 Nano Henry; in this particular case for one mm one mm width in spacing what happens here is that as the width is increasing the inductance value is decreasing.

So more the width, lesser is the loop area and lesser is the self on the mutual inductance that result out of it therefore, you should note that when we were talking of supply in ground lines we need to have wider tracks. Wider the track, lesser will be the inductance. Wider the track more is the capacitance we want more capacitance less inductance

therefore, it is good to go for wide tracks for the supply in the ground lines so that have more stable grounds. So we saw that in the last class and this class we had look at the various parasitics mainly the resistance capacitance and the inductance parasitic that will appear on the printed wiring board and in the next class we will see how we will be able to take care of some of the problem that come out of these parasitics. Thank you!