

## **An Introduction to Electronics System Packaging**

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**Module No. # 04**

**Lecture No. # 15**

**Electrical Issues – 1**

**Resistive Parasitic**

Good day to all of you! Today we will discuss issues related to the electrical aspects, when it comes to packaging or Printed Wiring Boards.

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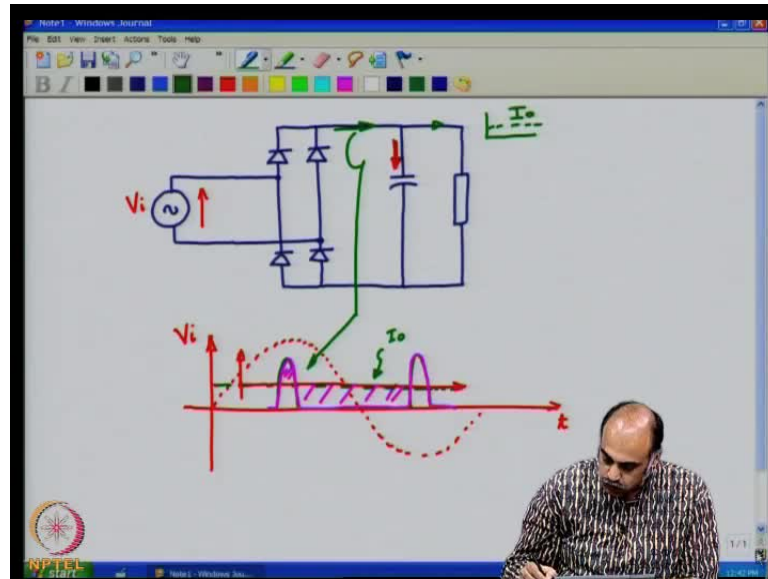
The Printed Wiring Board that you see here ultimately, is something that we will want to demonstrate some circuits, which will be mounted on Printed Wiring Board. The components will be mounted on the printed circuit boards like this, various components

like the capacitors, transformers, inductors, capacitors again, heat sinks, so on and so forth. You have the ICs. So, it becomes important that we have an idea of the electrical issues or electrical aspects that will actually reflect on the goodness of the design or the quality of the product, in terms of functioning of the circuit, in terms of also the reliability and the maintainability of the circuit. This is essentially the core issue that we will be addressing in this class and probably in the next two or three classes too.

When we come to the issue of electrical aspects, we think that the copper connections that we make on the Printed Wiring Boards are ideal and most of the circuit diagrams that we draw on paper and then design for it does not account for these non-idealities, but you should understand that the Printed Wiring Boards are made of copper, which has finite resistances and the currents flowing through that will have induced EMFs and therefore, the inductances and capacitances come into play and also the permittivity, the dielectric constants of the material used for making the Printed Wiring Board, all these affect the electrical parameters of the circuit. Therefore, one must take care when designing the Printed Wiring Boards and try to conform to certain broad guidelines.

You should note that there are so many issues and so many uncertainties it may not be possible to take care of all the issues in one layout and routing. Therefore, probably you may have to make two or three iterations, before you come at the optimal layout and routing for a given circuit; but when you take care of these guidelines which will handle some of the issues that I will be mentioning shortly you will be able to reduce the number of iterations and that is the intent of this particular discussion.

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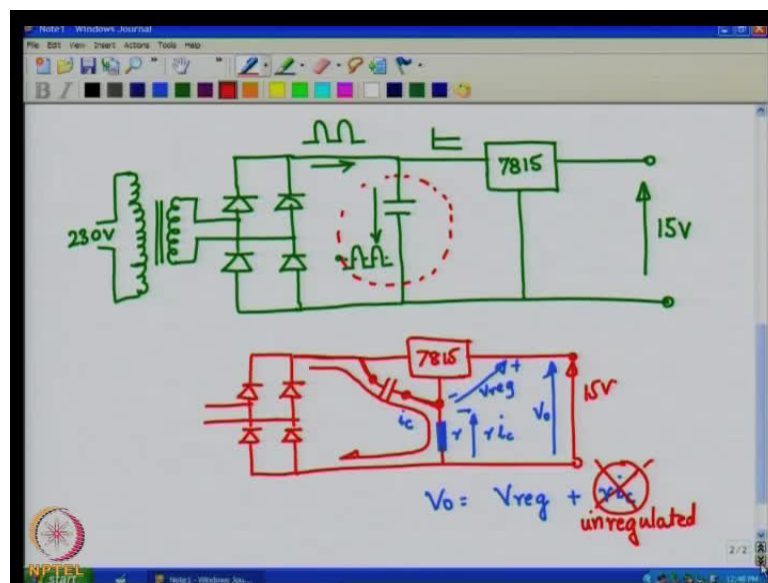


Let me start by giving you some scenarios where you could see some problems. Let us say, I will take the example of a circuit like this: You have an AC source and this AC source is connected to a rectifier. It is a simple circuit. The idea here is not to learn about the circuit but to learn about the issues that will arise in the circuit when it is implemented in a Printed Wiring Board or a Printed Circuit Board PWB or PCB, that it is called. This is a very common circuit most of you would be familiar with this. This is called a diode bridge rectifier. The output of which is connected to the capacitance as you see here and the load could be anything else and many other things could be connected to the load as well. Now if you look at this particular aspect here, I will draw your attention here to the current that will flow through the capacitance. The current that flows through the capacitance is of this particular nature.

Let us say that the input waveform here is of this form, time versus  $V_i$ , where  $V_i$  is the input voltage and I am going to show that in dotted. So assume that it is the sinusoidal 230 volts grid voltage. Now, the current that flows through this capacitance here, would be of this form. At somewhere around here, you will see the peaking type of current like that, something of this form (Refer Slide Time: 06:35). So this is the type of current that you would see at this point, through this capacitance and the current through the load here (Refer Slide Time: 07:00) would be an average of that, this is  $I_o$ , which is the average of this. Now I must say that the current through the capacitance is actually an AC component, which is actually, 0 with respect to this dotted line.

So I should say that the current which was here is the green one, which I am showing and let us say this dotted line here is the average; then the capacitance current the red arrowed current would be having a zero based on this, something like that. More colors here, so you will see that it goes in this fashion. Get the essential idea is that the chart here gets cancelled with chart here and it is a pure AC current that is flowing through the capacitance.

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Now for a circuit which is like that, we shall now, show the problem that would come in the PCB or the Printed Wiring Board. We have the bridge rectifier as shown here and one of the normal applications of this bridge rectifier is to connect it to a regulator. Now, let us say I connect it to a regulator like this. Let us say you would require 15 volts regulated output here. A 7815 series regulator is connected in this fashion. You take the output from a transformer and the transformer primary is connected to 230 volts.

Now remember that the current which is flowing here is of this nature. The current which is flowing here (Refer Slide time: 10:18) is of this nature; shifted in average, this is 0 and the current which is here is the average value; so, that is what is flowing through this.

Now let us say that within the PCB, the circuit is something like this. Let us focus only on the positioning of this. One possible positioning is, where you have the rectifier

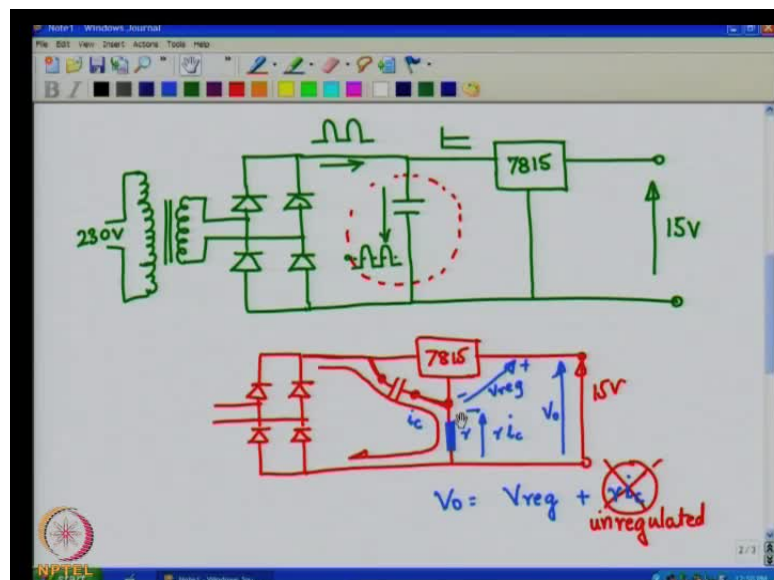
portion as such, there can be many possibilities. Let us say that we have the regulator connected in this fashion and the capacitance is connected like this (Refer Slide Time: 11:33) because you have the tracks coming in this fashion. The capacitors are fixed like that you have the regulator which is connected like this. So physically let us say the capacitor tracks are running in this fashion on the PCB. So what happens, you have a current flow, a spiky current flow like that and if all were ideal, there is no difference between the circuit shown in red and the circuit shown in green. However you should understand that everything is made of copper, the tracks on the PCB are made of copper. There is a finite resistance here and this is going to show up as a drop across this resistance  $r$  into if this is the current  $i_c$ , which is flowing through the capacitance we shall call it as  $i_c$  so this extra drop  $ri_c$  is going to be felt here and what is its effect here on  $v_0$ .  $v_0$  is nothing but this drop plus minus plus this drop so if you say this is the  $v_{reg}$  voltage, which is actually the 15 volts coming out of 7815 then  $v_0$  we can write it as  $V_0$  equals  $V_{reg}$  regulated voltage coming out of 7815 plus  $ri_c$ . Now this portion (Refer Slide Time: 14:02) is unregulated, is something that we do not want it to come to the output but this is an error that will come on to the output, deregulate the output by virtue of a routing, which is as such like this where by the capacitor current flows through this parasitic component,  $r$ , which is trying to couple some of the unregulated portion to the output. This is one of the issues that can occur when you are doing the PCB routing layout and routing and one must be careful about this let us look at the resistances a bit more closely, when we take of the PCB track.

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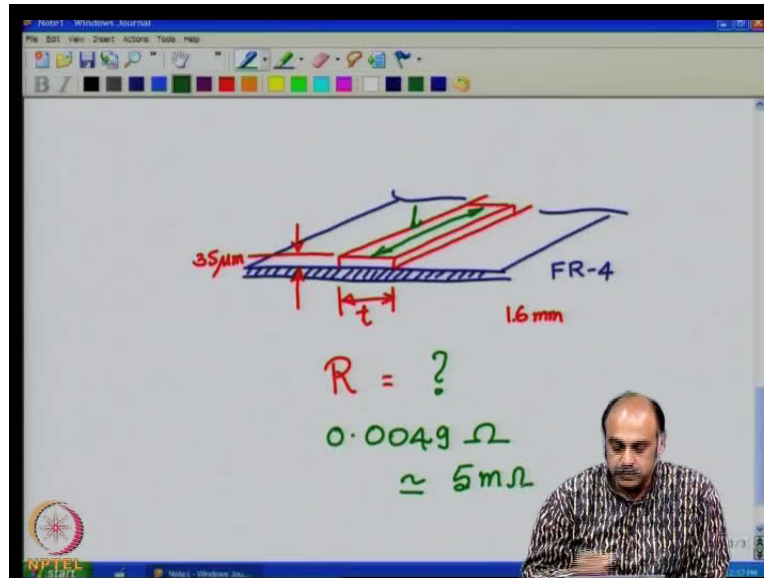


For example, now look at the board here. You see this board. Now if you look at this board you see it is made up of many tracks. It appears silver but they are all copper tracks and they are tin plated to prevent the oxidation of copper. So these copper tracks have finite resistances. This is a single sided board. There is nothing on the back. This is just a single sided board, but there are boards with multiple layers so for the purpose of explanation, I want you to focus on the various tracks. Various tracks have various thicknesses. The connector tracks here have different thicknesses, the ground lines have different thicknesses, the signal lines have different thicknesses, the supply lines have different thickness, I mean the width. All these are going to give some finite resistance.

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So when we draw connection circuit connections here like this on paper. The lines that we draw here are not zero resistance lines. These are all resistance lines. There will be a resistance as we saw here; a line that you draw here contains resistance so any current flowing through that is going to cause a drop which will have a detrimental effect on the circuit operation. So let us have a look at the values, some numbers. What are the values of the resistances? So if you take Printed Circuit Board, let me draw these two lines to indicate the laminate thickness so this is the material which is generally an epoxy material or you could say glass epoxy. They have different names the more common ones FR-4, G10 so on and on this we have a copper track. Let me indicate that by red. Now this copper track has a resistance and we need to find out what is the resistance of this copper track for some particular known distance. So let us say that we need to consider this particular small segment. There is a thickness associated now. This thickness of the track here is actually not controllable once you buy a laminate of a specified thickness that is pre-defined now this would be 35 micron meter which is the most common copper laminate thickness that you would use. All these boards here that you see thickness of the copper would be 35 micron. If we see the thickness of the dielectric that would be around 1.6mm and on that dielectric you have this copper which is 35 micron you will get 70 micron also you will also get 120 micron; however 35 micron laminate is the one which is usually used.



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**RESISTANCE OF COPPER TRACKS**

For Copper @20oC,  
1.7241e-8 ohm-m

For a track length,  
1cm = 1e-2m

Resistivity,  
ohm-m

Length, m

$$R = \frac{\rho l}{A} = 0.0049 \text{ ohms}$$

Area, m<sup>2</sup>  
For a 35μm laminate,  
1mm track width  
= 35e-6 x 1e-3 m<sup>2</sup>

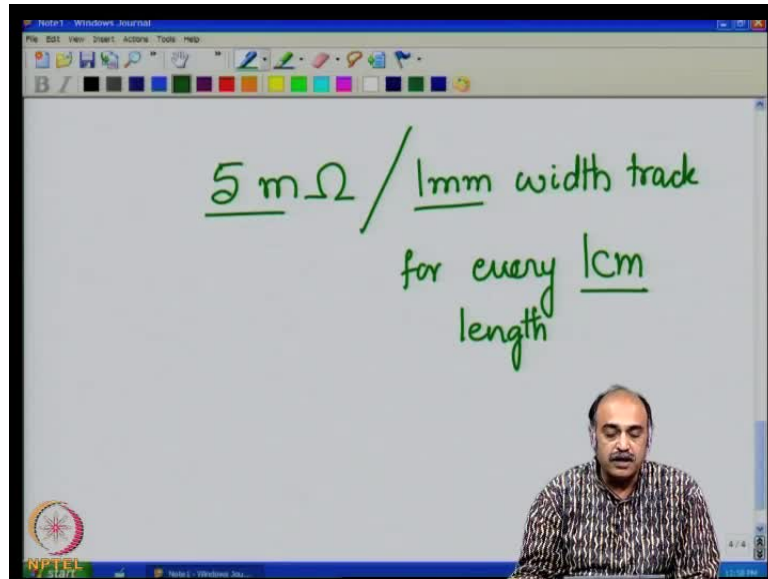
NPTEL

Now such a particular laminate with (Refer time: 20:00) copper on that let us estimate the resistance R for some specifications. Let us say we need to estimate for some thickness t and for some length let us say a length l, what is the value of the resistance? So this is what we want do. Let me take to you PPT slides. Now here if you see the resistance R is given by rho l by A where rho, the Greek symbol rho is called the resistivity. It has a unit ohm-meter and you have the Length l as I was just mentioning before we are talking about the length of the track; length of the copper on the Printed Wiring Board laminate and then you have the area of cross section. The area of cross section is the area that is presented to the flow of current. Now the area of cross section is nothing but the thickness of the laminate 35 microns in general case into the width of the laminate.

Now for copper, the resistivity can be obtained from the science tables, at 20 degree centigrade; the resistance value is as given, 1.7241e minus 8 into 10 to the power of minus 8 ohm meter.



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Then let us try to find out what is the resistance for a track length of 1 centimeter. 1 centimeter in meter would be  $1 \times 10^{-2}$  meter. Then for 35 micron laminate that is the copper thickness on the dielectric board 1 mm track width would be  $35 \times 10^{-6}$  meter square. This would result in a track resistance of 0.0049 ohms. What is 0.0049 ohms? You should remember that 0.0049 ohms is approximately 5 milli ohms. So a bit of thumb rule here, so that quickly you can remember is 5 milli ohms for 1mm width track for every 1 centimeter length of the track.

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**EFFECT OF TEMPERATURE**

For Copper,  $+0.0039/^{\circ}\text{K}$  temperature coefficient of conductivity

85°C - 20°C,  $\Delta T = 65^{\circ}\text{K}$  Temp difference

$$R_{T_1} = R_{T_0} + R_{T_0} \cdot c_T \cdot (T_1 - T_0)$$

R at temp T<sub>0</sub>      Change in R due to temp. difference

For a 35μm laminate, 1mm track width = 0.0049 ohms @20°C

= 0.00614  
~25% more

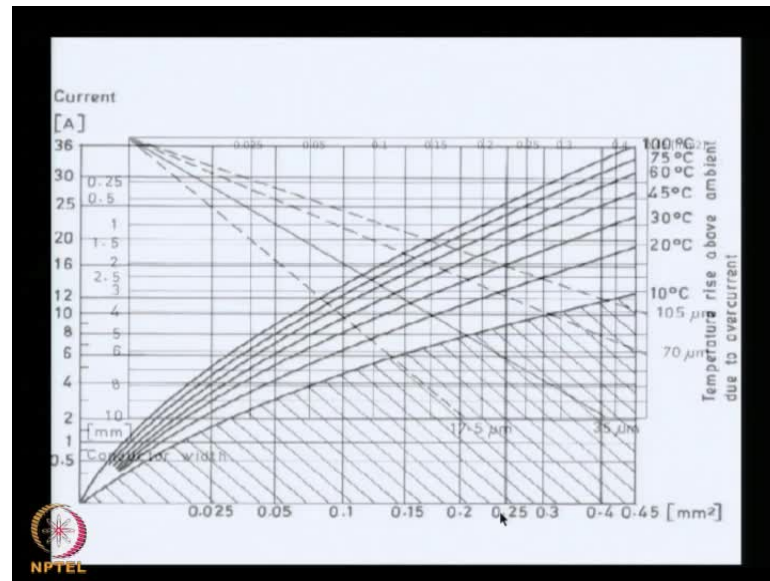
So this would be easy to remember because this would give you an idea of the kind of drops that you will be encountering when you are designing the layout and the routes of the PCB or the Printed Wiring Board PWB. 5 milli ohms for every 1 amount track width for a length 1 centimeter could be a significant amount when you take the whole track lengths. Now let us go back to their slide and see this issue we have with resistances, that is the effect of temperature. Not only do we have finite resistances due to the track width, temperature also plays havoc to our circuit and its functionality. So consider the resistance of the track at some temperature  $T_1$  that is equal to let us say the resistance at some temperature  $T_0$ ,  $T_0$  is our reference temperature. Most of the cases in science tables you will see that the resistance can be calculated for 20 degree centigrade just like within in the previous slide, the resistance was calculated for copper resistivity given for temperature 20 degree centigrade.

To that, you need to add a correction. Now this is the correction;  $R_0 C_T T_1 \text{ minus } T_0$ .  $T_1$  is the temperature at which we want the resistance value and  $T_0$  is the reference temperature. Now,  $R$ , the temperature that we have calculated at  $T_0$ , reference temperature most of the time 20 degree centigrade now change in the resistance due to the temperature difference  $T_1 \text{ minus } T_0$ . Temperature difference  $T_1 \text{ minus } T_0$  where the temperature  $T_1$  and  $T_0$  are normally expressed degree Kelvin and difference can also be expressed in degree Celsius. Now  $C_T$  is a new term you see here that is called the temperature coefficient of conductivity again obtainable from the science tables  $C_T$  is called the temperature coefficient of conductivity. For copper, it is 0.0039 plus 0.0039 per degree Kelvin, the plus sign is used because of most of the matters on the materials, the resistance increases with temperature but there are some cases where the resistances will decrease the temperature, called the negative conductivity but for copper it is positive plus 0.0039 for every degree Kelvin raise in temperature or every degree Celsius raise in temperature.

Now if you give some numbers now let us say the temperature difference that you want to calculate for is 65 degrees that is the temperature at which you want the resistance value is 85 degrees. The temperature at which you can calculate the nominal temperature is 20 degree centigrade because from the values of the resistivity, let us say you are able to calculate the resistance value at 20 degree centigrade; now for this extra sixty five degrees temperature difference, you have to make the difference calculation in the

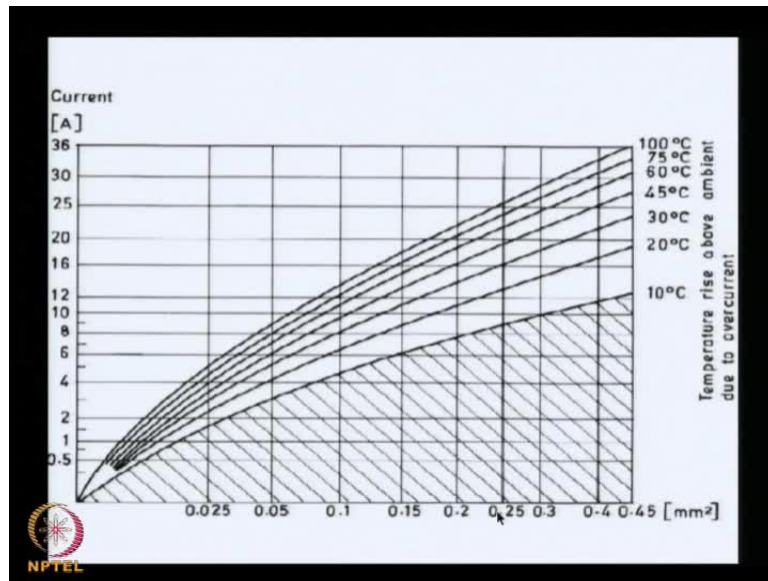
resistance and let us say for 35 micron laminate 1mm track width, we had calculated previously, 5 milli ohms approximately at 20 degree centigrade the value when you substitute all these, you will get 0.00614 which is actually 25 percent more if you compare with 0.0049 and 0.00614, take the ratios you will get 25 percent more for this 65 degree Kelvin extra higher temperature.

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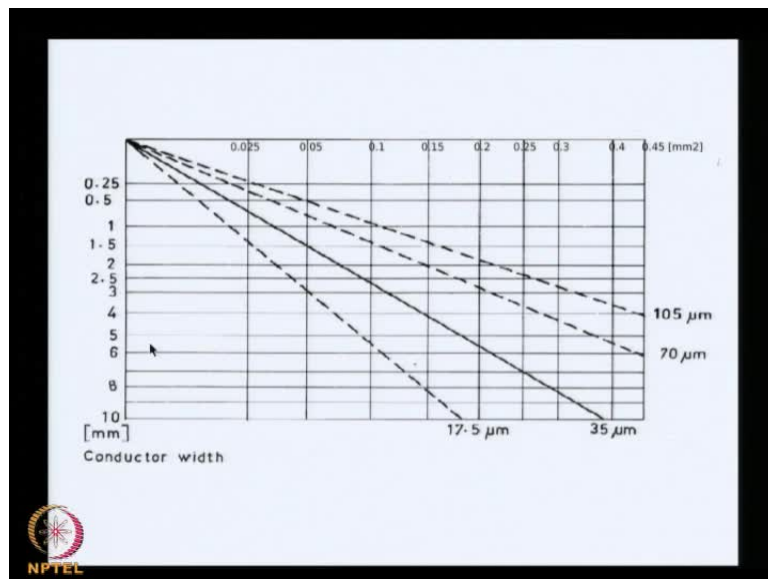


Therefore, we have a serious problem in the sense that we cannot neglect the resistances. You have to be concern about it and then carefully route the tracks. Here on this picture you see a graph here on the x axis you are seeing the mm square, the cross section area presented to the flow of current. On the y axis you are seeing the current and on the y axis on this side you are seeing the temperatures actually they represent the various curves here the family of curves for different temperatures.

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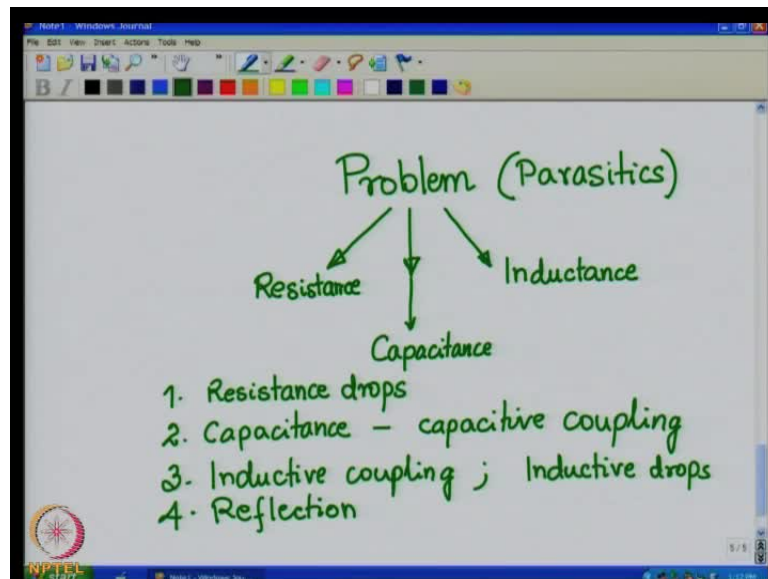


If you say for 20 degrees you would like to pass 16 amps then you take the x intercept and say that approximately here it cuts the 20 degree line at this point and then straight down if you go, it would be around 0.35 mm square so you will need a cross section area, track cross section area of 0.35 mm square. Likewise, you could do that for any of the curves at any other temperature like 60 degree takes the 60 degree line and depending upon what current that you want to pass, you then make the intercept taking down into the x axis and then look at what is the area of cross section that you will need for the track. Once the area of cross section for the track is known, then you could go to this

graph where you see on the x axis, the cross section areas and on the y axis you see the track width or the conductor width in mm.

So for a 0.35 mm, you could pick a particular laminate thickness of the copper. As I was saying you can have different laminate thicknesses that are available but the most common one is the 35 micron copper laminate thickness so you would project the cross section area on to that laminate thickness line and then go on to the y intercept and then find out what is the track or the conductor width that is needed for that particular application. So this way you could use these two graphs together to find out what should be the conductor width that I should apply in the routing rules for a given current.

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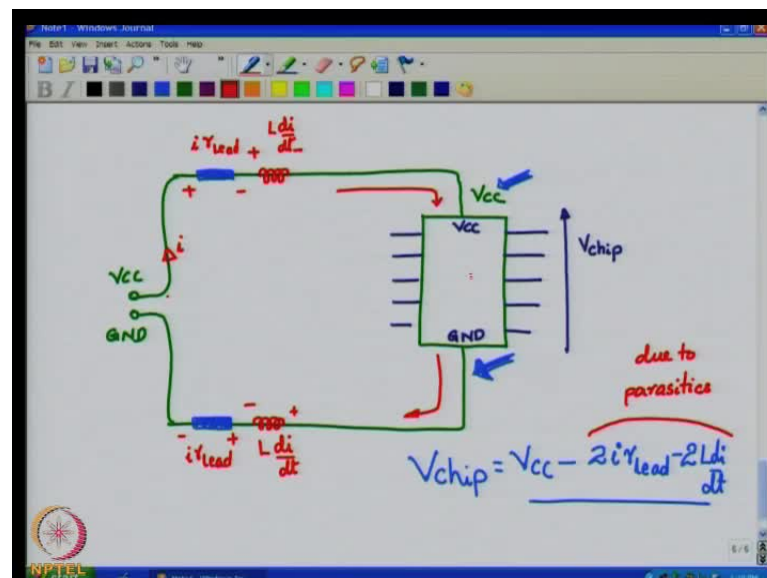


Now one is the problem of finite resistance as we were seeing. We have also another problem, the problem of finite capacitance. We also have the problem of finite inductance, now all these problems due to the parasitics can cause functionality problems in our electrical circuit. The first one is being the resistive drops that we just discussed the second one due to the capacitance, there could be capacitive coupling between two tracks and this can result in capacitive cross stocks. Then you can have inductive coupling resulting in a mutual inductance between two tracks and then cross tracks due to that. The inductance can also cause further problems not only in coupling between tracks; it could also cause inductive drops. This is also a major problem that needs to be addressed.

And then you have another problem, the problem of reflection. At high frequencies, when you use high speed digital circuits the clock frequencies or the waveform in most cases are pulses they have very fast rise times and these fast rise times mean very high frequencies and the tracks will behave like transmission lines and because of the transmission line effect, you will have reflections both at the sourcing side and the destination or the load side and the waveforms will not be neat pulses but due to the reflections it will vary and you will have overshoots and undershoots as we will see later on.

Now these problems are the ones which are more common and that we need to address I am just only stating the problems but we need to also see how we take care. For the resistance case, we just saw that the drops across the resistance can cause the problem functional problem in the output where a current flow through a capacitive circuit can flow through track drop track resistance and get coupled to the output and cause deterioration in the regulation of the output. Likewise, you could have a problem with capacitance and inductance too.

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Let us say for example, you have a digital circuit like this. This digital circuit is connected on one side to a  $V_{cc}$  and on the other side to a ground. These  $V_{cc}$  and ground lines are actually tracks which get connected like that. These are also tracks let us say it goes and terminates at a particular connector pin or at some other portion of the Printed

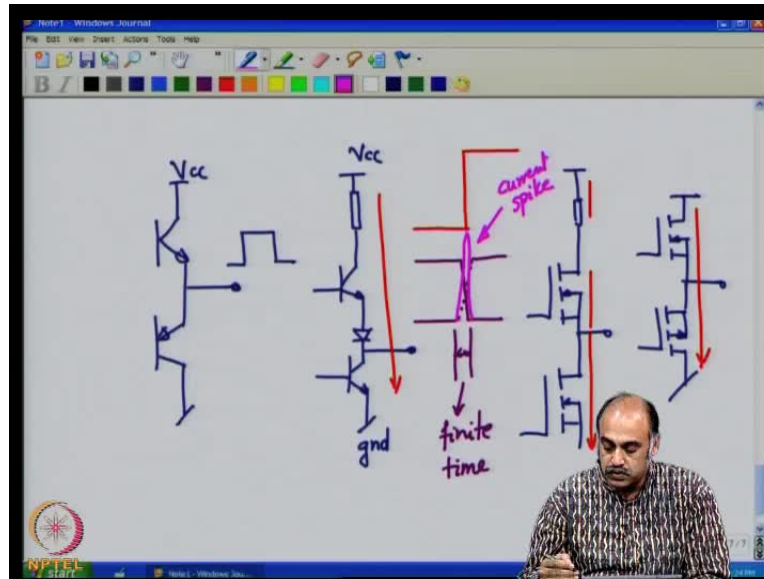
Wiring Board which is connected to the  $V_{cc}$  pins of the particular power supply connectors.

Let us say this is our  $V_{cc}$  and this is our ground pin. If you look at, not only do we have resistance, which we are now lumping it and putting it here. Actually you have the resistance on resistance lumped for all these supply lines. You can have a resistance lumped for all these ground lines, let us say like this, And then apart from these resistance you could have a track inductance as seen here. Again a track inductance for the return path depends upon the length of the line. All these could be lump together and put a shown here. This green block is some IC, some digital IC high speed IC, which probably has clocks, and probably other buffers connected to it. We are now focusing only on two pins of this IC, which is the  $V_{cc}$  pin and the ground pin.

Now let us look at the voltage that is appearing across the  $V_{cc}$  and ground pin of the IC we will call it as  $V_{chip}$  just directly across the IC. Now if you look at this particular circuit, you have a current which flows from  $V_{cc}$  through like this into the  $V_{cc}$  pin. It flows out like that. So you have various drops (Refer time: 42:00) associated with each of this component, you have a plus minus drop for the resistance, plus minus drop for the inductance. Let me write it down, let say  $i$  is flowing through this, instantaneous value; you have  $i$  into  $r$ , let us say  $r_{lead}$ , you have  $L$  into  $di$  by  $dt$ . I have again plus minus another  $L$  into  $di$  by  $dt$  return path and another plus minus and you have  $i$  into another  $r_{lead}$ . So if you assume that the tracks are equal in length, then  $r_{lead}$  on the supply side and  $r_{lead}$  on the return side  $L$  on the supply side and  $L$  on the return side let us for the moment, assume to be same so that we can write down  $V_{chip}$ .  $V_{chip}$  is equal to  $V_{cc}$  minus 2 times  $i$  into  $r_{lead}$  minus 2 times  $L$   $di$  by  $dt$ . So, what you would actually see at this point is not  $V_{cc}$ , but  $V_{cc}$  minus this amount due to the parasitics this is non-ideality due to parasitics.



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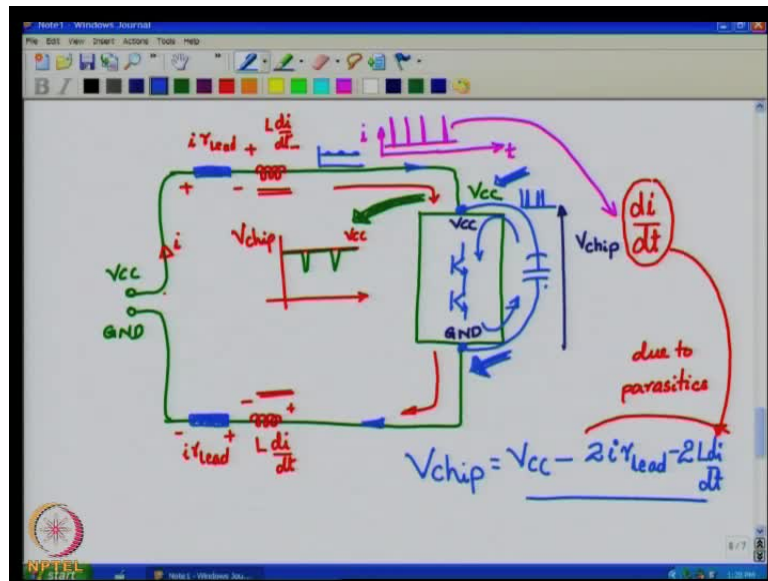


Now you may say that the current  $i$  which flows here may be very small for digital ICs and therefore, these drops can be insignificant and can be neglected but you should note that they are not actually very insignificant. Most of these ICs are made up of gates and if you look at the various stages of the gates and at the output stage of the gate you will have probably totem pole structure with something like this; if it is TTL kind of a structure this output stage you have  $V_{cc}$  and you have the ground, this is a totem pole structure. You may also have structures like this, MOSFET structure or you could also have structures there is p n p, n p n types or p type n types, there you could have  $V_{cc}$  ground you could have structures like this you could have the p type in the at the top and n type in the bottom so many such structures are possible.

And then you will see that most of the cases you will have the outputs of the gates because they need to switch you need this is the one which will come out of the gate and this is supposed to be a switching or the pulse, the waveform which will take either a low or a high value everywhere it has to take a low or a high value these switches what we call the bottom switch or which is the one connected of the ground or the top switch connected to the supply the top switch connected to the supply bottom switch the top and the bottom switch never are they on together it is either the top switch which is on or the bottom switch which is off mutually exclusive. However there is a time there is a very small time, when let us say the bottom switch is on and the top switch is off. Now the bottom switch is turning off and the top switch is turning on so there is going to be a

transition from this switch to this switch or vice versa. During the transition, this bottom switch is going from on state to off state, the top switch is going from off state to on state, so there is a very small period of time when during the transition both are conducting during that time the  $V_{cc}$  is connected to the ground through a very small resistance and during those transitions you could have a current surge or a current spike with just flows through flows through like that.

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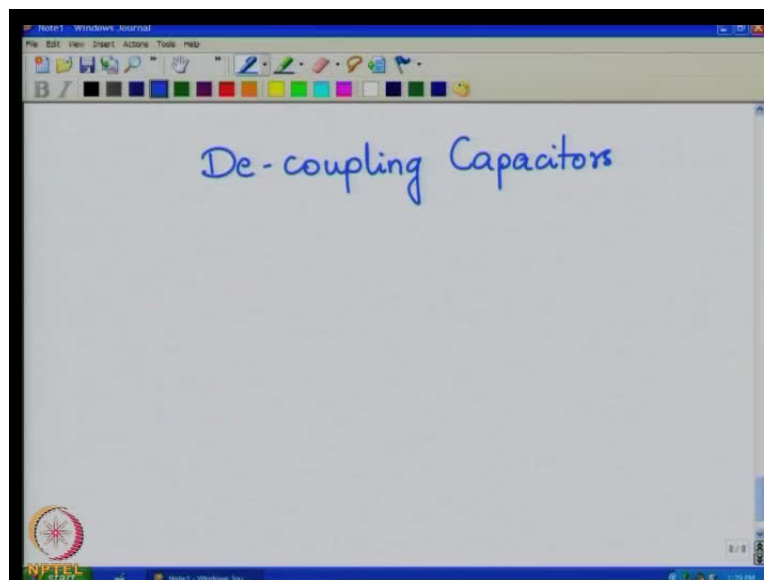
So during transition if you see that you have a transition from low to high. At every such transition, the top switch let us say for example, (Refer Slide Time: 49:00) which is turning on, which means it would be going from a high state to a low state, low resistance state and the bottom so each is going from a low resistance state and going to the high state. Now this transition period is finite time and during this time you will have quite a large current spike like that. This is your current spike. (Refer Slide Time: 50:00) Now that current spike for one gate you could have a quite a large current spike few millions and then when you take mini gates, you could have quite a significant amount of current spike again that depends upon the technology which is used in making this a IC

So which basically means that the current which flows here can be need not be a constant DC like that it will be spiky at every transition you will see a large current spike which results due to the output stages of the gates having either totem pole or a bridge or an

arm structure where you have mutually exclusive switching switches however during the transition time there is a period where you can have these kind of spikes.

Now when you have these kind of spikes, now this spike is having a very high  $d_i$  by  $d_t$  in a very short duration during the raise time or during the transition time which is in the order of few nanoseconds you have a current quite a large current and  $d_i$  by  $d_t$  is quite heavy quite large and now this  $d_i$  by  $d_t$  is going to result in inductive drop here and here  $L d_i$  by  $d_t$  which is a major cause for the voltage here to fall so if you look at the voltage  $V_{chip}$  versus time it is no longer just  $V_{cc}$  this is  $V_{cc}$  but it is going to at every transition you will see a dip so you will see the voltages, the supply voltages at this point is really in a bad shape so this supply voltage needs to be corrected, One of the ways that we normally would correct the supply voltage is by putting a capacitance directly as close to the  $V_{cc}$  and ground pins you put the capacitance this called a decoupling capacitance so whenever there is a switching or a state transition within the IC the spike currents are drawn from the capacitance which is acting as a buffer and they are not drawn from the  $V_{cc}$  so for the spike currents are actually transferred here in to the capacitance giving that one and here you see much more stable current waveform which is a going through these leads therefore, the  $L d_i$  by  $d_t$  drop can be significantly reduced.

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Now such capacitors are called decoupling capacitors. These capacitors what you see here are called decoupling capacitors which actually provide decoupling between the

track inductances and the ICs which is drawing the spiky currents, The decoupling capacitors can also be brought into effect due to the tracks, which are there on the Printed Wiring Boards because when you see the tracks the tracks are nothing but (Refer Slide Time: 55:00) the two plates of the capacitance and in between you have this dielectric which is the PCB themselves and you can design the tracks width and the grounds such that some capacitance is brought into effect between the supply and ground and they can act as the de-coupling capacitor. These would be the beneficial effects of making use of the parasitics for solving some circuit related problems. We shall, of course, see decoupling capacitor how they can be build we shall also look at what the values of the capacitors and inductors would be and the effect that these have on the circuit in the following classes. Thank you for all.