An Introduction to Electronics Systems Packaging
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Module No. # 03
Lecture No. # 14
Multichip modules (MCM)-types
System-in-package (SIP)
Packaging roadmaps
Hybrid circuits
Quiz on packages

We will have continue with the chapter on packages; as you know, we have covered an extensive amount of detailing on the definitions for single chip modules, the definition for multichip modules and we have also seen various acronyms, and also we have looked at the advantages of using the advanced packages of today like BGA and CSP, and also briefly we touched upon multichip modules.

So, will start with again defining what a multichip module is, and look at some of the methods to fabricate MCM, much of it will be covered during the PWB technologies chapter, because as you know today, we are working more with organic packages for cost, efficiency and also for high performance applications.

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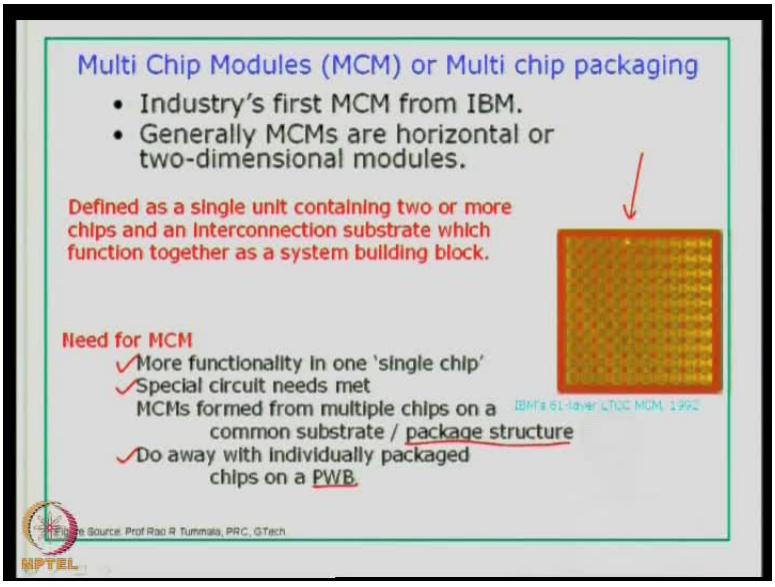

So, if you look at multichip modules MCM or multichip packaging, compared to SCM

which is the single chip module, here we have a single unit which contains two or more chips on a common substrate and interconnected together on the common substrate, so that it can form a system level building block. So, definition for MCM can be, a single unit containing two or more dies or chips and an interconnection substrate which will function together as a system building block, the substrate can be organic, it can be ceramic too.

The industries, first multichip module came from IBM, and generally, multichip modules when you talk about their structure; they are typically horizontal or two-dimensional modules. If you look at the figure here, is a typical ceramic multichip module fabricated by IBM in 1992. So, multichip modules are not new, it is the question of what kind of substrate and the methodology to create a high density multichip module that becomes very interesting.

Why is the need for a multichip module, because if you compare with single chip module what we are trying to do, when we go in for a multichip module, it gives more functionality in one single block, or you can call it as a single chip, because as a package if you look at the multichip module, you have these units interconnected on a common substrate and they can be encapsulated. So, when you handle these multichip modules, it will look as a single chip, but in essence it will have more than 2 dies or chips interconnected on the substrate.

So, its provides more functionality, special circuit requirements are met by going in for multichip module, which if you try to do it using different single chip modules then, the real estate occupied by the total combination of these dies will be very large. So, you try to do as much integration as possible on a single substrate. Multichip modules are formed from multi chips on a common substrate we have seen that. So, it is important to create a package structure or a substrate or a package substrate that can handle these interconnections, because basically, we are going to do fan out of the I O’s from the die on the substrate.

We can also do away with individually packaged chips on a printed wiring board, because if you look at this scenario, where you trying to - as I mentioned earlier - individually packaged chips mounted on a printed wiring board, then it is going to occupy a lot of space, so at the chip level, at the package level you are trying to integrate.

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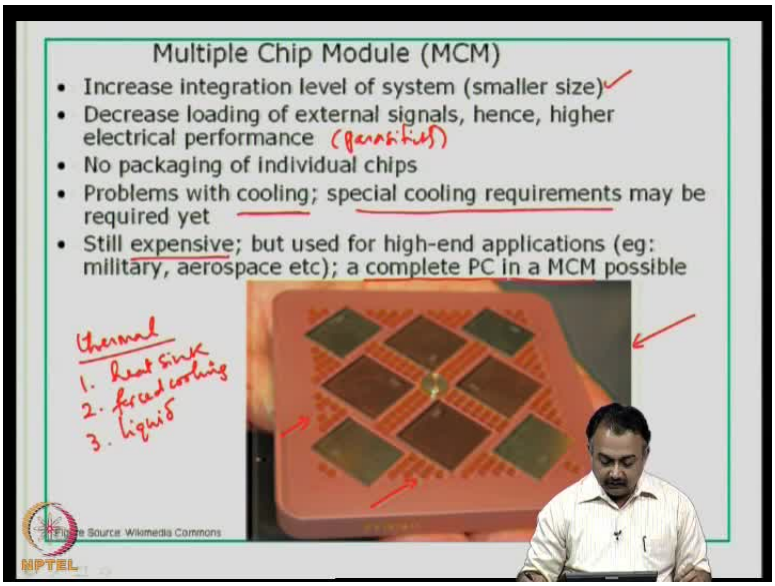

Now, what are the other benefits of multichip modules, it increases the integration level of system, therefore, you are able to work with smaller sizes that are the main advantage of multichip modules. Now, electrically if you look at, you are expected to get better performance by using a multichip module, because it will decrease the loading of external signals, which otherwise, if you look at a printed wiring board which contains individual chips, interconnected to perform a common function that it is intended for, then the loading will be very high, there can be a lot of electrical parasitic that will be affecting the entire system, and therefore, you will have poor electrical performance.

Therefore, this multichip module, if it is well designed with the physical properties of the substrate taken into account, whether it is an organic or ceramic substrate, and then, increase the number of layers to handle these signals and power delivery, then we are going to get a highly efficient, high performance multichip module.

As mentioned earlier, no packaging of individual chips. There are going to be problems with cooling, because we are trying to integrate a lot of chips on a common substrate therefore, you will be met with problems in thermal management, so that has to be handle carefully. Therefore, if you look at the substrate, you have to look at the thermal dissipation property, dielectric constant, thermal conductivity and so on, when you choose the substrate.

In addition to that, we have to look at special cooling requirements, what are the special

cooling requirements for a multichip module? Because, in some cases, the amount of heat dissipated during the power of optic device for the system can be very high, therefore, you have to look at employing better heat sinks to remove the heat; you have to probably use embedded heat sinks. The other alternative is you have to use forced cooling methodology to remove the heat from the various chips of the dies. And in some cases, if you are looking at multichip modules that are being used for high end servers or high performance applications, liquid cooling is also used.

So, thermal management becomes a very important issue, so the various alternatives are you can either use a heat sink - various types and new materials - then forced cooling, air cooling or it could be using some kind of a liquid, it could be water, it could be liquid helium kind of a material that is being used by a few companies for their various high end servers or high performance application products. Therefore, thermal management becomes an important topic in the design of multichip modules. Therefore, it could be expensive, compared to looking at chip on board configuration or simply assembling different single chip modules on a common substrate.

But, multichip modules are designed with the particular application in mind, therefore, in some cases for strategic applications, military, aerospace and so on, cost is not a factor, so cost is not the driving factor, it is the performance is the reliability that we look at. Therefore, for high end applications, even though it is expensive it is being used. So, simple system is, if you can build a complete PC in a multichip module, then you are looking at better efficiency compared to the kind of large mother board that are being used today in computing systems.

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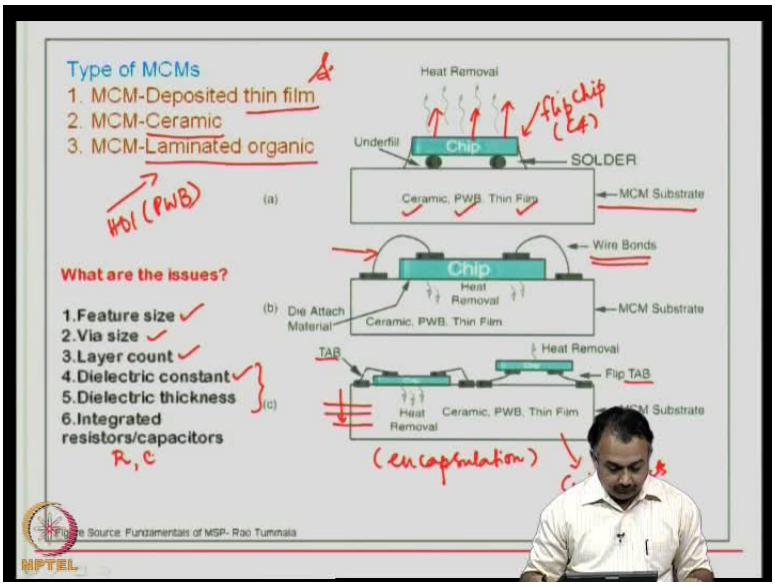

So, here is a picture of a multichip module, where you can see different dies assembled on this surface of substrate - ceramic substrate - and then interconnected, there are also passives that are used in conjunction with the active devices. Now, what are the types of multichip modules; that we can look at, the first thing is known as MCM-D; MCM-D stands for deposited thin film structure, the second one is MCM ceramic which means, that the MCM is built on a ceramic substrate.

The third one is known as MCM-L also known as Multichip Module Laminated organic substrate. So, in the first case, we are going to deposit thin film for creating conductors on the substrate, so typically this is something like a silicon process, fab process. The second case you are going to use a ceramic substrate, so you are going to utilize the properties of inorganic ceramic substrates. The application areas for MCM-D and C are quite different from that of MCM-L. MCM-L can be viewed as typically, a high density interconnect like a PWB structure, it is only a high density system that we are building because we are using organic substrates, and the process technology for MCM-L is almost similar to that of a high density or multilayer printed wiring board fabrication.

Now, if you look at the accompanying picture here, if we have a MCM substrate like this, where you can have a ceramic or an organic or a thin film, then you can have the first level interconnection by using a flip chip, so this is the structure of a flip chip or a C 4, as you know by now. So, you will have an under fill, you will have a solder bump

interconnected on to the MCM substrate. The heat is of course, as briefly mentioned earlier is dissipated through the surface of the chip to the external environment. So, you can have a flip chip on an MCM substrate, then you can have wire bonding done on an MCM substrate.

So, here again all the three possibilities of having a ceramic, organic or a thin film can arise. So, here you will see that you have a chip that is bonded on to the substrate by gold or aluminum wire bond, so this is the second method of first level interconnection that can take place. And the third one is TAB - Tape Automated Bonding, here again you can have flip tab as well as a normal, say, sub tab configuration. So, the three first level interconnection on chip connection choices that we have seen before is possible with multichip modules. Again, encapsulation here is a very important process to protect the die after the interconnections are established. So, you can imagine multiple connections of the die on to the common substrate, and again on the substrate you can have interconnects made out of copper to complete the MCM structure.

So, basically what are the issues? The issues in terms of going for a multichip module choice, the first thing is feature size compare to because when you use a single chip module, some of the disadvantageous can be taken care of when you going for a multichip module. The first thing is the feature size, when I say feature size, we are talking about interconnect line width, pad sizes and so on.

The via size that is used for interconnecting various copper conductors through multilayers structures. So, the conductor of the top layer needs to be interconnected to the conductor at the intermediate as well as the outer layer on the other side of the substrate, and for these we use via structures. Vias which can which have to be very small if you want to build a high density interconnects structure, so that the design of multichip module has to take care of lower line width smaller via sizes.

The layer count typically, can vary from 2 to 12, 18 or 24 layer multichip modules structures. Now, optimization in this case is very important, layer count depends on the pad density or the pin density of the total number of components that are employed in this multichip module. And the kind of fan out that is required from the die to the substrate, because you have to take care of the power delivery, the ground pads, the ground layers, and signals to be effective in electrical performance.

The dielectric constant of the substrate becomes very important, you can play around with different materials; different fillers can be used in the case of ceramic substrate as well as organic substrates. Dielectric thickness is again related to the process, say for dielectric thickness and dielectric constant, will give the choice or a better design utilizing these properties will give better electrical performance.

Because it is normally a multilayer structure, then you can try to integrate your resistors and capacitors into the structure of the multichip module substrate. Because these resistors and capacitors are now part of the interconnect system along with the active devices, because if you encapsulate having these actives and the passive devices we are going to get complete system in hand.

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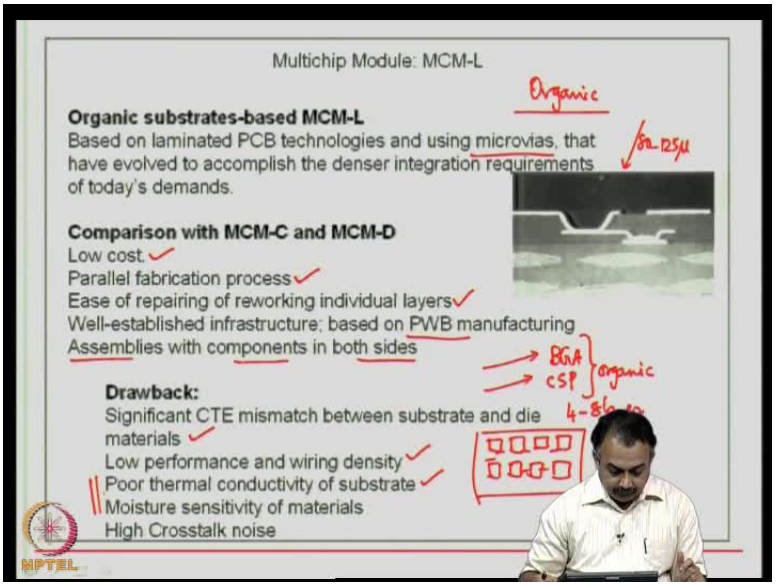

Now, briefly in one slide I would like to mention about the multichip module L type fabrication process. Remember, we are going to discuss these technologies in detail when we look at PWB technologies later. So, in a MCM-L type of structure we are going to use organic substrates, so that is the key part of it.

Now, if you look at the PCB technologies, we are going to use what is known as laminates. Earlier I had showed you samples of BGA and CSP which are made out of organic substrates, and has you would have seen this structure which have illustrated earlier.Typically, they are 4 to 8 layer organic substrates and these interconnects in each of this layers are connected by what is known as microvias and these microvias as you

see here in this picture are of the order of 80 to 125 microns.

So, one of the essential requirements is that you have to build this MCM-L substrates using PCB technologies and you have to achieve higher integration that can comply with current demand. So, MCM-L will be typically used for manufacturing BGA components, CSP components, but at the same time you can imagine an organic substrate in which various dies are placed on the organic substrate, and then they are interconnected and these interconnects pass through various layers.

So, MCM-C and D are much expensive processes, so MCM-L is supposed to be low cost, because it follows organic processing and PWB processing. It is a parallel fabrication process in the sense that, if you look at the formation of conductors or via structures, it is a parallel fabrication process; the output can be very high. Ease preparing of reworking individual layers; that means, when you build the inner layers of the multilayers structure in a MCM-L, you can look at the defects and repair them before encapsulating the entire module.

So, this is one of the advantageous of MCM-L, the infrastructure is well established because, globally if you look at the PWB manufacturing process, it is a well matured technology, well matured establishment, therefore you do not have to build or spend more money or capital for fabricating MCM-Ls. Therefore, PWB manufacturing setup can be well integrated for MCM-L. If you look at the finished MCM-L which is basically a high density PWB, you can assemble components on both sides that is the basic advantage of using MCM-L. Because you can easily connect through vias, the top and bottom layer, for example, of an 8 layer MCM-L, and therefore, you can use surface mount devices on both sides to increase the density of the MCM-L.

The drawback is that, when you use silicon die, there will be a huge or significant CTE mismatch between the substrate and the die materials, which I have explained in the previous session, low performance and wiring density compare to MCM-C and L, poor thermal conductivity of the substrate, because we are using organic substrates and the inherent property of the organic substrate is that the thermal conductivities very poor compare to ceramic substrates, now you can improve it by adding more pillars or composite materials.

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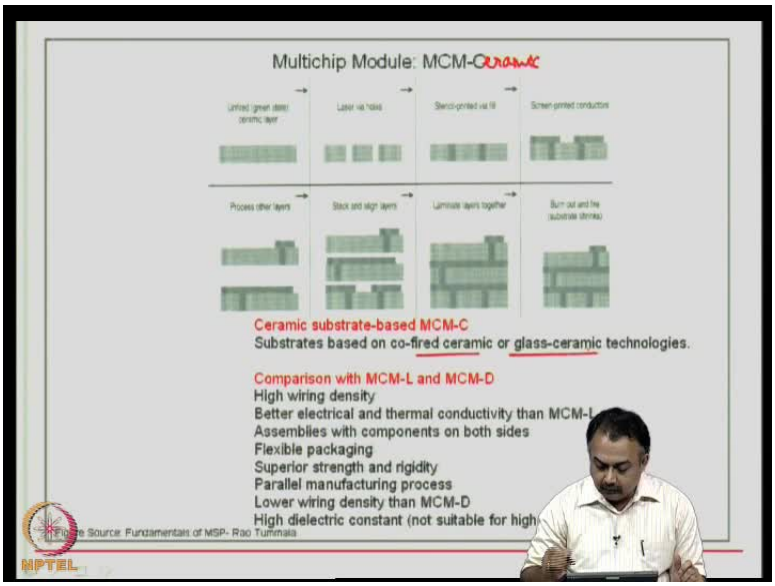

Moisture sensitivity in organic materials is very high, therefore this drawback in terms of electrical poor electrical performance because of moisture absorption is going to be there, but if you look at cost, then people tend to go in for MCM-L. The MCM-C, that is, ceramic process is expensive compared to MCM-L; it is based on co-fired ceramic or glass ceramic technologies.

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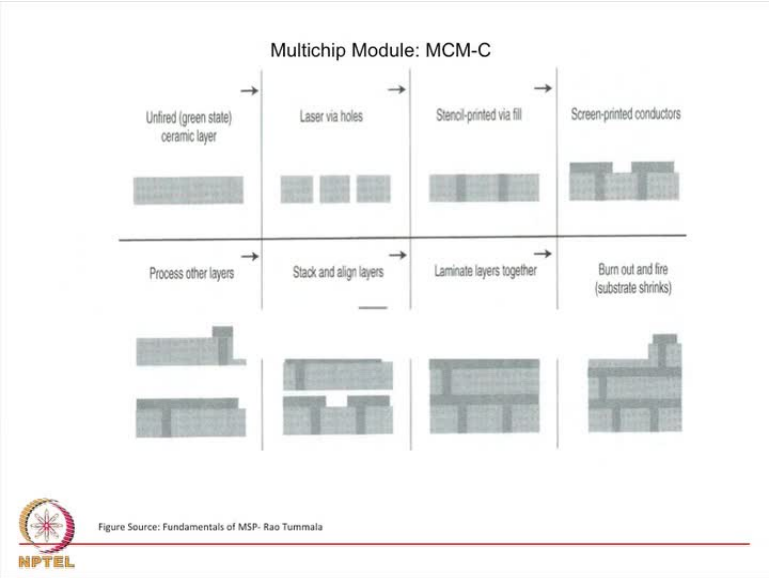

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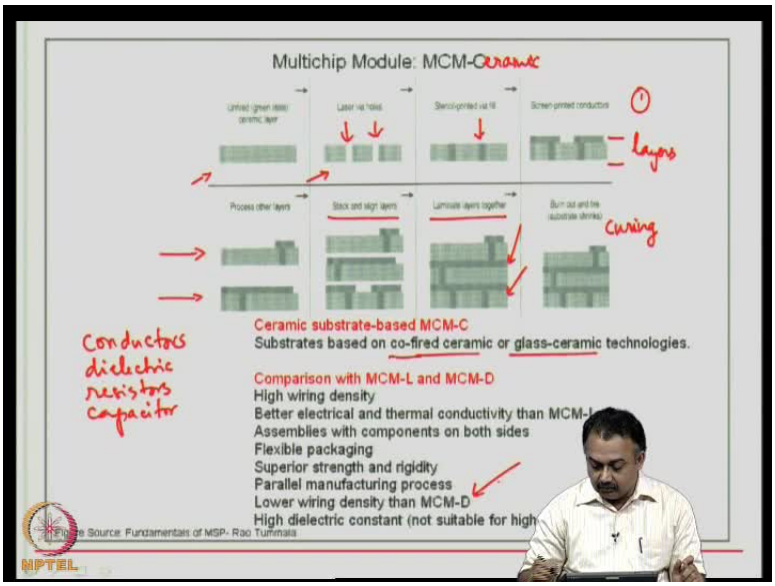

So, the substrate is ceramic, glass composite material, and when we say co-fired what basically happens is, for building MCM-C you require conductors, you require dielectric materials, and then, you may also require resistors and capacitor materials.

Now, these are available or used in the form of inks, compare to the plating process or the thin film deposition process in MCM-D, if you look at this figure, basically, we start with the unfired or a green state ceramic layer in the first case, then you prepare the interconnect holes by laser drilling. So, you can see here that the vias are generated on the green ceramic material, when we say green, it is a uncured ceramic material. Now, these vias are filled with conductors, so that a connection is established between the top layer and the bottom layer, so this is how the layers are generated in MCM-Cs structure.

Then similarly, you can build multilayers like this, so this is, the first row indicates one step or one process sequence which will complete a dielectric combination as well as a conductor buildup. So, you can build as many layers as you want, stack these layers according to the design, you laminate them again, now you can see here the various layers are interconnected by this via holes, and these vias are made conductive by screen printing or tensile printing a conductor inks.

Now, what you do is, you do a curing process by co-firing, so the word co-fire is used in this context of the green ceramic material and the conductors, in addition to other layers where you can have resistors and capacitors, these are co-fired at a particular temperature

and the actual properties are then obtained only after the firing process is completed. In a green state the actual properties are not attained, and there be shrinkage, so in the design stage you have to give leverage for shrinkage of material.

So, compare with MCM-L and D, you will get a high wiring density, better electrical and thermal conductivity because of ceramic substrate compare to organic, assembly with components on both sides is possible, flexible packaging because, you can decide the lamination structure and the buildup.

Superior strength and rigidity because of the ceramic substrate, you can use different types of dielectric materials for different layers. It is a parallel manufacturing process; that means, you get the throughput, for example in the via of fabrication can be very large. Low wiring density compared to MCM-D, but a better wiring density compared to MCM-L, high dielectric constant, therefore, it is not suitable for high frequency applications.

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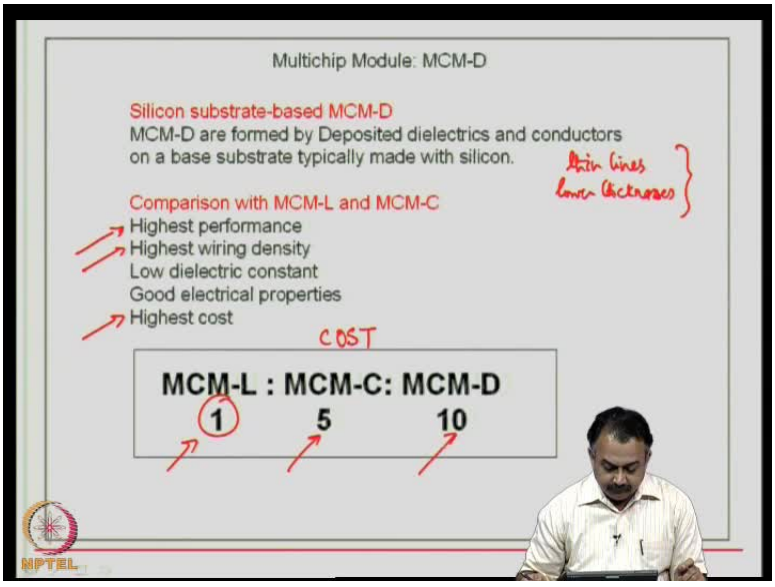

Now, if you look at MCM-D, D stands for Deposited thin film, the fabrication is similar to silicon substrate based process and these are formed by depositing dielectric materials and conductors on a base substrate typically made with silicon. So, it is something like fabricating or using a wafer fabrication process, but on a slightly macro skill because it is a package substrate.

Compared with MCM-L and MCM-C, this is got highest performance because of superior material properties, both the dielectrics and conductors, and also because, your able to work with thin lines and lower thicknesses, whether it is a dielectric material or the conductor, therefore your able to get better electrical performance. Highest wiring density, again because of these feature sizes being better, low dielectric constant, good electrical properties but highest cost, so if you look at cost as an issue, in comparison between MCM types, if you look at 1 for MCM-L, then MCM-C is 5 times costly compared to MCM-D which is 10 times that of MCM-L. But as I said, the choice of MCM-C and D will depend on the end application.

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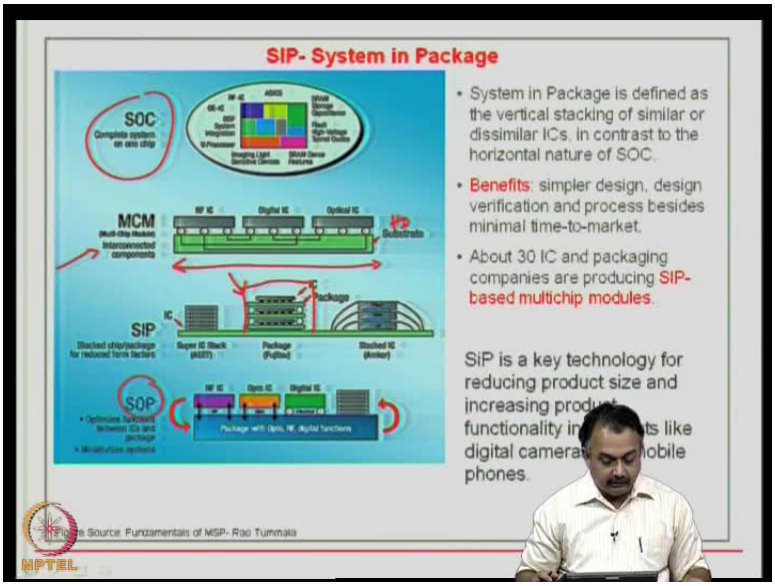

So, that completes the multichip module introduction, we will now look at another package format that is now widely being used, but selectively known as System in Package. System in package is not available of the shelf, it is the concept where you can establish some kind of a vertical stacking of similar or dissimilar Ic's, in comparison to the horizontal nature of MCM that we have just seen. So, if you look at this figure here, the different definitions is, the first thing is what we have seen what is SOC - System On a Chip, where we are trying to build a complete system on a chip.

So, you can have an ASIC, you can have a D-RAM or an S-RAM or some kind of a processer, circuit that is built at the chip level, and then you integrate them, interconnect them at the chip level, you get system on a chip. The MCM that we have seen just now is

basically using a common substrate and a 2D kind of integration on a single substrate. You can have different ICs here active devices, it can be an RF IC, a digital or an optical IC, and then, you will have a high density substrate that we take care of interconnects.

Now, compared to these, SIP is basically looking at, for example, vertical stacking of similar or dissimilar IC's. If you look at this package for example companies like Fujitsu, Amkor and many others bring out this custom built system in packages. So, here you can see this particular block, that the IC's are vertically stacked and then interconnected again to a common substrate, they can also be interconnected to the adjacent dies. So, the design would involve establishing interconnects either by using wire bond or flip chip interconnects.

The system in package substrate can be organic, it can be ceramic, but the requirement is that it has to be a high density interconnect substrate. And then we have system in package, basically is a very key technology for reducing product size and increasing product functionality, which is not possible, for example, with an MCM type of a structure or if you want to reduce the overall package size. So, this comes as a package, there will be a definite encapsulation that will be done after the various dies are joined together and interconnected.

And these are typically used for small products; handheld products, like mobile phones, digital cameras and so on. Now, there is another terminology call system on package which is now catching attention of all the industry globally, where you are looking more at optimizing function between ICs and packages, and we are trying to build many etherized system. So, we will come to the definition of system on package shortly, so system in package is a very specialized fabrication activity that is practice by about 30 to 40 companies globally, and they produce system and package based on your requirement.

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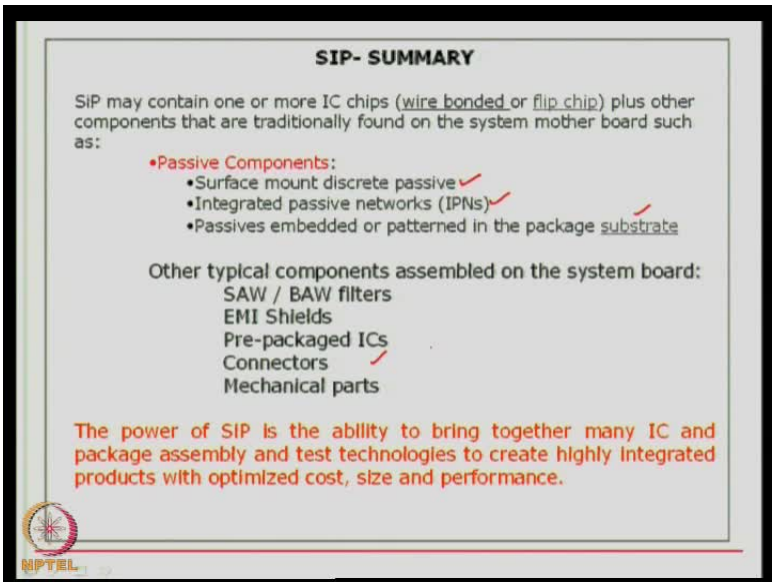

So, the summary of system and package is that you can use active components; you can use passive components along with the active devices. So, it may contain two or more devices - active devices - which can be wire bonded or flip chip interconnected. And you can have surface mount discrete passives, passive networks or embedded passives in these structures and then, encapsulated finally to give a system in package. The other typical component that can be used could be connectors, some other mechanical parts, EMI shields, filters and so on.

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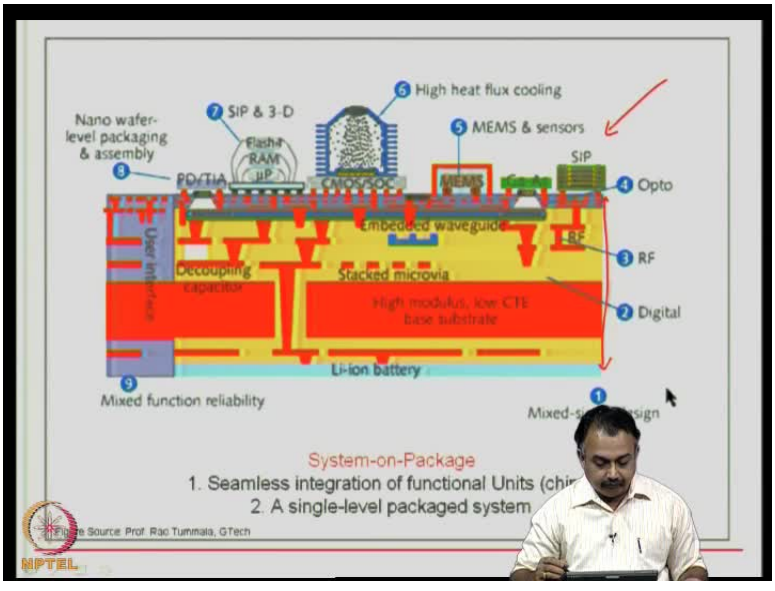

Now, the system in package objective or the driver for SIP should be that it should reduce the cost, in comparison with a multichip module and it should have high performance, better electrical performance including thermal reliability. Now, this is the system on package that I was talking about. If you look at system on package, what it basically does is, it gives you a single level packaged system typically on organic substrate like your refer FR4, polyamide and so on, and it is basically a seamless integration of functional units.

So, if you can imagine a cross section that is shown here, this is taken from George tic, because one of the institutes which pioneers in system on package technology. So, we can look at the cross section here, the batteries embedded, there is a user interface, this is a high density interconnects structure that you are seeing here, it could be organic at reduce cost. you can have embedded RF components, You can have embedded RF components, then embedded waveguides, stacked microvia structures of the order of 50 micron and so on, of the die of the microvia, decoupling capacitors embedded again, and of the surface you can see, active devices like system in package mounted on the SOP, gallium arsenide, deposited thin films structures. You can also have embedded actives in this structure MEMS, then CMOS system on a chip, then you can have 3-D structures and so on.

So, this is basically increasing the component density on an organic substrate. And one of the requirements to bring down cost is that, which should be high modulus, low CTE organic substrate. So, you can consider this as a board with a very high density ok and providing all the features like an SIP, MCM and an SOC can do, but SOC, SIP and SOP are different in terms of the approach, whereas one is IC centric, the other is package centric.

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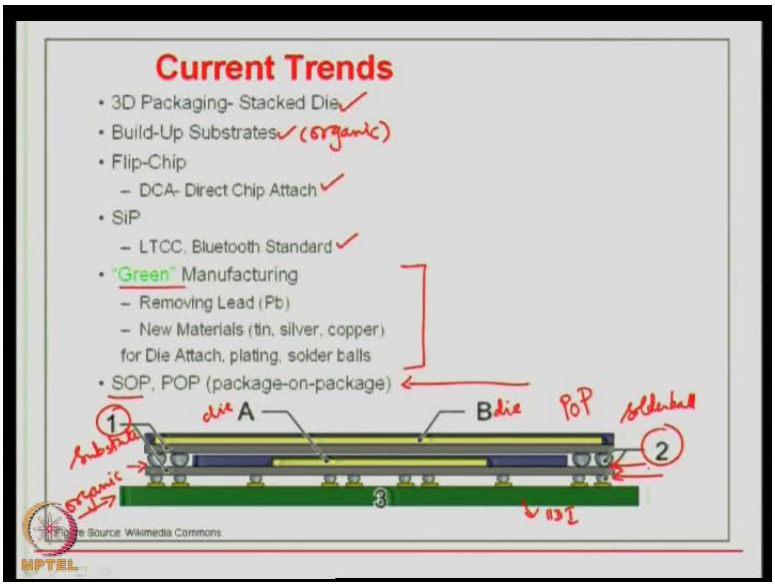

Now, as a summery, what are the current trends in packages? People are going in for 3D packaging or stacked die that we have seen. So, if you look at system and package, for example, or you can see there is a stacked die structure. Now, stacked die involves a lot of care in choosing the die size and the type of interconnect that you will establish between the various chips that you are using, then you have buildup substrates, typically, in organic and ceramic also you can have buildup.

Buildup involves realizing very small microvia structures and the ability to add layer by layer, and test each layer before adding another is a key issue in buildup substrate technology. More people are using direct chip attach or flip chip. SIP is used in all communication products, Bluetooth standard products, then we are moving in to green manufacturing; that means, lead has to be removed, we have to look at alternatives for lead, new materials for conductors and new materials for die attach, plating, solder balls and so on.

So, there is always greater demand for using new materials in each of these areas that we have seen, and new packages today will come with new materials. Then, we have seen what is SOP, and the latest thing to happen in packages is the arrival of package-on-package.

If you look at this figure here, this is a POP - Package-On-Package, so what are the component of a package-on-package, here you see, that A here defines one die and here

B defines another die, and the section 2 here mentioned is the solder ball, and here 1 depicts the substrate of the individual package. If you look carefully at this cross section you will see, that there are 2 packages - completed packages - so which includes the die B that is one package, which ends in a BGA type of interconnect, then there is a second package which houses the die A and also contains a BGA kind of a interconnects structure. The dimensions of these individual packages, and solder balls, the thickness, the thickness of the substrate everything can vary, but in essence you are looking at two different packages.

The package B is actually mounted on package A; that means package A should contain provision for assembling package B on top of it by solder ball connection. And this second solder ball grid from the package A is mounted on to an organic substrate, so this organic substrate again will be a high density interconnect, and this is known as package-on-package. Now, with very great expertise, you can repair by removing package B from A but again you are going to look at the effects of soldering during repair and rework on the bottom die also.

Therefore, repair and rework as of today is going be a big challenge, but presenting a POP like this, is similar to a stack die, but the fact is that a lot of thought has to go in to the design of package-on-package, because one of the package sits on top of another package, and therefore, provision for landing pads for one of the dies has to be well designed, so these are the current trends in packaging.

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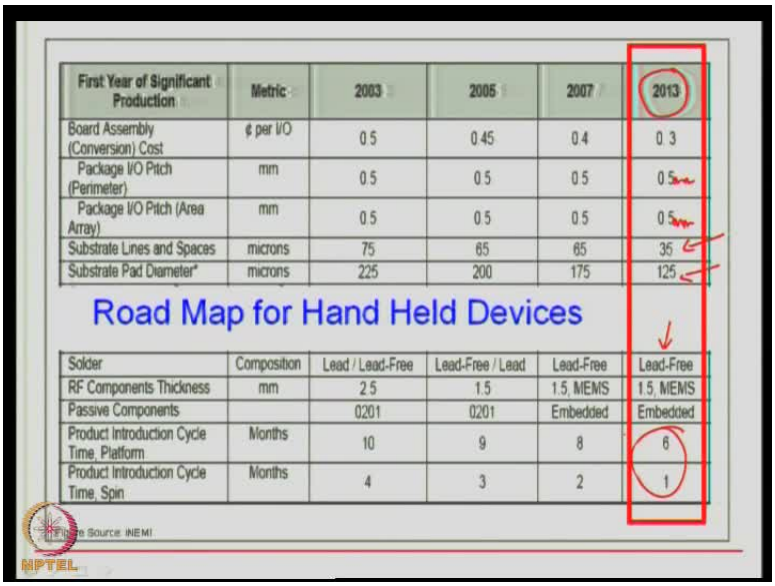

First Year of Significant Production	Metric	2003	2005	2007	2013
Board Assembly (Conversion) Cost	¢ per I/O	0.5	0.45	0.4	0.3
Package I/O Pitch (Perimeter)	mm	0.5	0.5	0.5	0.5
Package I/O Pitch (Area Array)	mm	0.5	0.5	0.5	0.5
Substrate Lines and Spaces	microns	75	65	65	35
Substrate Pad Diameter*	microns	225	200	175	125

Solder	Composition	Lead / Lead-Free	Lead-Free / Lead	Lead-Free	Lead-Free
RF Components Thickness	mm	2.5	1.5	1.5, MEMS	1.5, MEMS
Passive Components		0201	0201	Embedded	Embedded
Product Introduction Cycle Time, Platform	Months	10	9	8	6
Product Introduction Cycle Time, Spin	Months	4	3	2	1

Source: iNEMI

Now, finally, I will take you through the road map for packages and package assemblies, which employ these advanced packages. So, if you look at hand held devices, the road map today and what I have indicated here for 2013, you can look at the demand and the direction which the industries progressing.

So, if you look at substrate line and spaces typically, we have to work at around 35 microns, substrate pad diameter is 125 microns, package I O pitch for area array is 0.5 mm. So, typically for BGAs are, this is the standard today, even for CSP; that means if you go below 0.5, then it is a CSP. Then, if you look at package, I O pitch perimeter package, it is also 0.5 mm and broad assembly cost is something like 0.3 cents for I O.

So, there are challenges for hand held devices because, unless you meet these requirements you cannot be a leading edge manufacture, in terms of solder. You have to work with lead free materials, no more lead, RF component thickness 1.5 mm, so the profile of the package is very low, passive components have to be embedded, and again there are demands for turnaround time for manufacturing.

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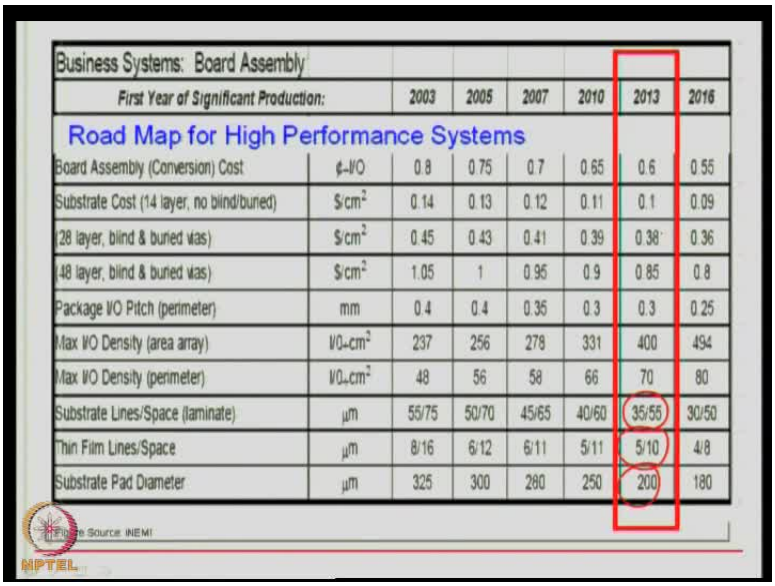

First Year of Significant Production:		2003	2005	2007	2010	2013	2016
Board Assembly (Conversion) Cost	¢-I/O	0.8	0.75	0.7	0.65	0.6	0.55
Substrate Cost (14 layer, no blind/buried)	$/cm^2	0.14	0.13	0.12	0.11	0.1	0.09
28 layer, blind & buried vias)	$/cm^2	0.45	0.43	0.41	0.39	0.38	0.36
48 layer, blind & buried vias)	$/cm^2	1.05	1	0.95	0.9	0.85	0.8
Package I/O Pitch (perimeter)	mm	0.4	0.4	0.35	0.3	0.3	0.25
Max I/O Density (area array)	I/O-cm^2	237	256	278	331	400	494
Max I/O Density (perimeter)	I/O-cm^2	48	56	58	66	70	80
Substrate Lines/Space (laminate)	µm	55/75	50/70	45/65	40/60	35/55	30/50
Thin Film Lines/Space	µm	8/16	6/12	6/11	5/11	5/10	4/8
Substrate Pad Diameter	µm	325	300	280	250	200	180

If you look at road map for high performance systems, again right from 2005 to 2015 you can see the progress or the directions with which the industries progressing or substrate line and space. For example, 35 micron, 55 micron space, thin film lines 5 micron and 10 micron space, substrate pad diameter is 200 microns, area array maximum I O density is 400 I O' s per centimeter squared that is the kind of density we are looking at. So, if you look at multilayer systems again, the cost has to come down even as we increase the multilayers structures.

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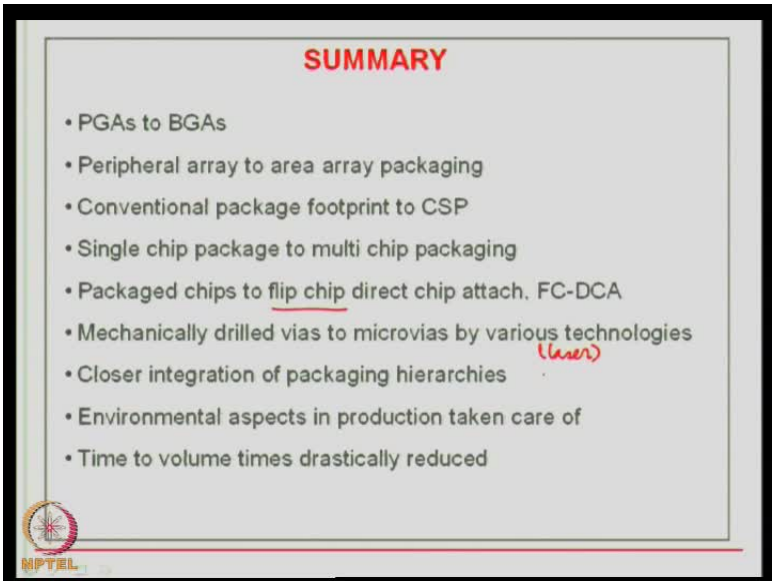

So, summary for this chapter on packages is that, if you have gone through the various sessions that these packages encapsulated. BGA is the work cross, so we are moving from PGAs to BGAs, we are moving from peripheral array packaging to area array packaging. We are moving from conventional package footprint to CSP type of footprint, and CSP pitch as you know is very small, single chip packaging to multichip packaging is the order of the day.

Packaged chips to bare die, that is flip chip C 4 interconnect or direct chip attach on board technology is available. So, more designs will come with flip chip direct chip attach, we are moving away from mechanically drilled vias to microvias by various technologies like laser and so on. There is closer integration of packaging hierarchies, if you look at the various hierarchy products that we have seen, fortunately there has been very close integration, environmental aspects in production has to be taken care of and time to volume has been volume time has been drastically reduced.

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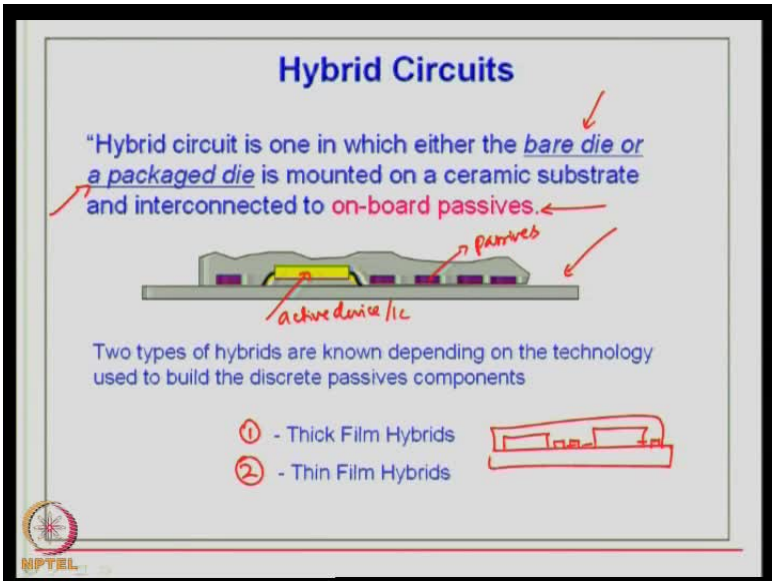

So, this is basically the summary of this particular chapter and before we close I want to introduce a new term called hybrid circuits, which in some sense is closely related to the type of package, that we are - packages that we are aware of - especially, when use ceramic packages, but we will deal with hybrid circuits and MCMs when we come to the technology part.

So, hybrid circuits are one in which either the bare die or a packaged die is mounted on a

ceramic substrate and interconnected to on-board passives. Just as we have seen MCM-C a similar definition, you can look at the substrate here in this figure, then you have active device or an IC, and these are the passives, resistors, capacitors and so on.

So, there is a bare die or a package die which is mounted on a substrate and interconnected to on-board passives, so these kind of hybrid structures, where you can either use a bare die or a packaged die, in conjunction with on-board passives. You can also create passives (()) by printing resistors and conductors at the time of fabrication or at the time of buildup.

So, this kind of technology is known as hybrid circuits, there are two types of hybrid circuits; one is known as a thick film and the other is thin film circuit. And depending upon the technology that is used to build the discrete passive components, so typically, what you can think about is, there will be substrate, you can probably use a bare die or a packaged die and then, you will be realizing these resistors and capacitors on the board and then you will be interconnecting them, and then probably you can also use some kind of a encapsulation.

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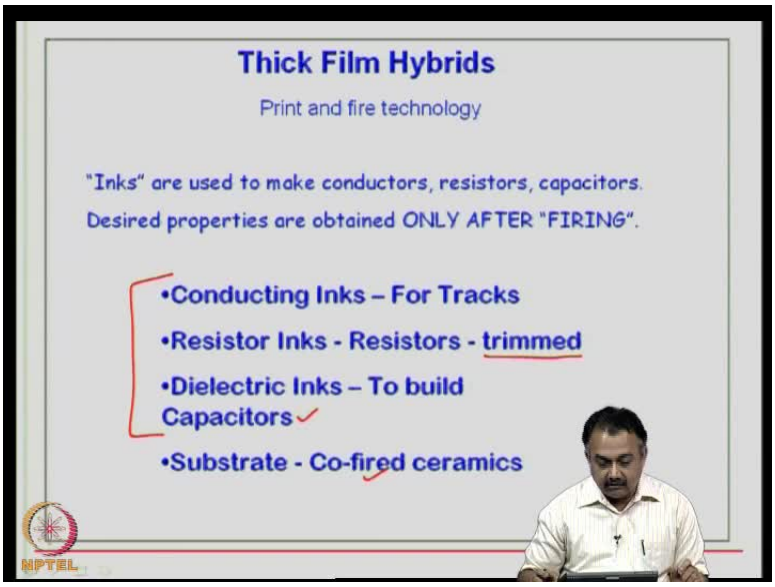

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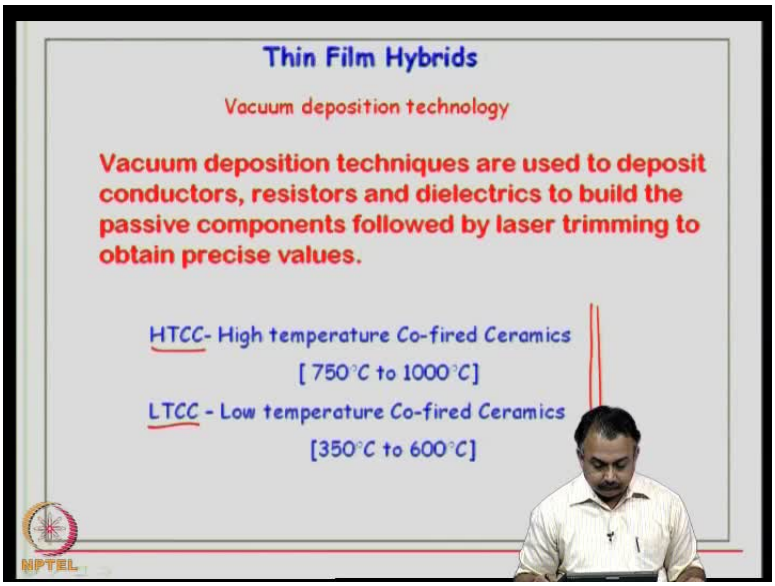

So, what is the thick film circuit? It is basically a print and fire technology, where you are going to use inks to make the conductors, to make the resistors and to realize the capacitors, and the desired properties are obtained only after firing, this is similar to the MCM-C. And you will use conductors for tracks, resistor inks for the various resistor functionality that you are required, you can fine tune the value of the resistors by laser trimming, and you can use dielectric inks to build the capacitors structures, and finally you can co-fire all these 3 materials to get the desired properties.

A thin film structure is obtained by vacuum deposition techniques and you can use this method to deposit conductors, to deposit resistors and dielectrics, and then build the structure, and you can also do laser trimming to obtain precise values. The temperature is used for low temperature co-fired ceramic is from 350 to 600, and then for a high temperature co-fired ceramic process, it is 750 to 1000. So, this is the important information regarding the temperature ranges of handling these devices.

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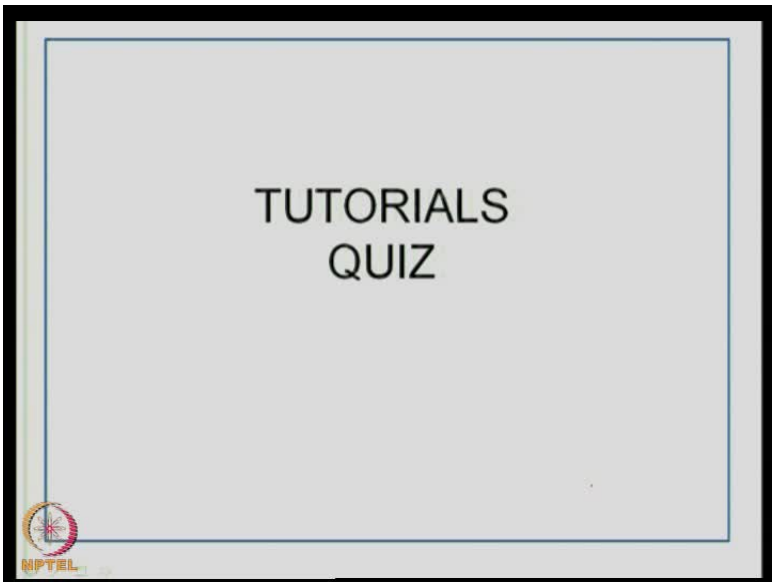

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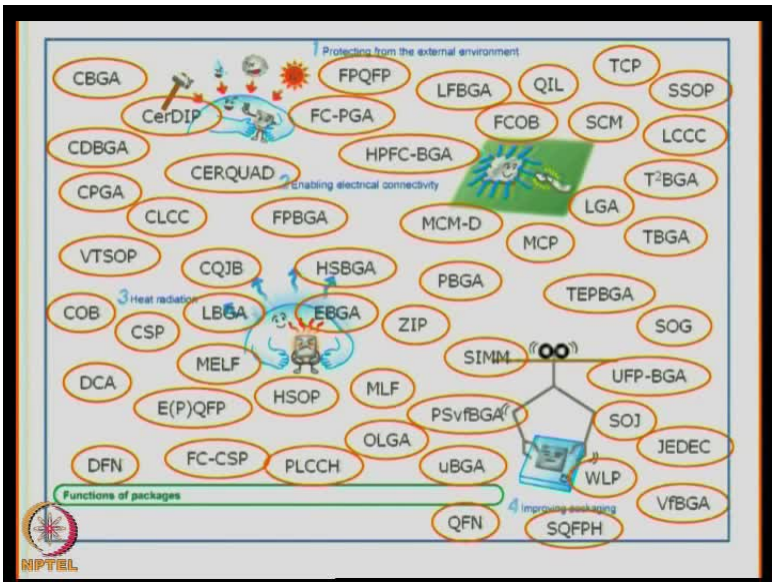

So, we are now at the end of this chapter, and we will spend some time briefly on some questions based on this chapter like a tutorial or a quiz. Now, the first thing before we start is that the function of packages, I want to reemphasize is basically, it should protect the device from the external environment, it should enable electrical conductivity through the leads or the pins or the solder balls that the package will have, heat radiation, removal of heat to protect the die and finally to improve handling assembly, and therefore, packaging is a very important aspects for active devices.

Now, what I am going to basically do is, put some of the acronyms and see if you are able to name these packages. So, this will give you a complete comprehensive understanding of what the terminologies today in the industry are. So, a CBGA, this has come up on the screen right now, a CBGA would mean what? CBGA means, a Ceramic Ball Grid Array, so you can see the answer coming up at the bottom left of your screen, a CBGA means, a Ceramic Ball Grid Array.

Then, we have CDBGA, it is known as Cavity Down Ball Grid Array. Now, you should be able to, in fact, draw the cross section of each of these packages as we move along in this particular course. Because we need to understand cross section of packages, we need to be able to draw down the cross section of packages to really understand the first level interconnect and the second level interconnect and the type of materials that are used.

The third one that we are going to see is CerDIP; CerDIP means, Ceramic Dual In line Package, then we have CPGA which is known as a Ceramic Pin Grid Array, then we have PBGA which is known as a Plastic Ball Grid Array, then we have TBGA, it is the package, it is known as Tape Ball Grid Array; is ZIP, Zig Zag In line Package. So, this gives you an opportunity to go to the web or text book that I have mention and see, what these packages, because they these are packages that are produced by various companies. If you go and look at the data sheet, you will be able to understand what kind of pitches they have, what kind of materials they have used, and what are the chip mounting choices interconnects that are being used in this packages.

Then, we have CSP; CSP denotes chip size or chip scale package, DCA is known as direct chip attach, then, we have COB, COB is known as Chip On Board, we have use we have seen what COB configuration looks like, CLCC is known as Ceramic Leadless Chip Carrier, CERQUAD is known as Ceramic Quad Flat Pack, FC-PGA this is Flip Chip Pin Grid Array system or package, FCOB is known as Flip Chip On Board; that means, you are using a flip chip on board, which is similar to a - I mean - this is different from a chip on board, where in chip on board you will have face up configuration.

The next one is FPQFP, this means, Fine Pitch Quad Flat Pack, the next acronym that you should know is CQJB, which is Ceramic Quad Flat Pack j bend leads that come out from the package. You have now FPBGA which is Fine Pitch Ball Grid Array. Then you have EQFP or EPQFP which is known as Enhanced Plastic Quad Flat Pack, the term

enhanced is use for using better materials to remove heat from the QFP. DFN stands for Dual Flat No lead package, QFN stands for Quad Flat No lead package, QIL stands for Quad In line Package, LFBGA stands for Low Profile Fine Pitch Ball Grid Array, then you have SCM Single Chip Module.

LGA stands for Land Grid Array, MCP stands for Multi Chip Packaging, SOJ stands for Small Outline J leader package, WLP stands for Wafer Level Package, UFP-BGA is Ultrafine Pitch Ball Grid Array, HSOP stands for Heat-Sinked Small Outline Package; that means, it is a SOP which contains a material that is used for heat sinking purpose, MLF stands for Micro Lead Frame Package, FC-CSP is Flip Chip Chip size package or chip scale package, LBGA stands for Low Profile Ball Grid Array, low profile is small thickness.

Then, you have OLGA Organic Land Grid Array package, which is seen in Intel processors, EBGA stands for Enhanced Ball Grid Array, again enhanced means, using better thermal materials, SSOP stands for Shrink Small Outline Package, SQFPH stands for Shrink Quad Flat with Heat spreader, PSvfBGA Package Stackable very fine pitch Ball Grid Array.

So, you must able to understand what package stackable means; that means, it contains a stacked die configuration, SIMM stands for Single In line Memory Module, HPFC-BGA stands for High Performance Flip Chip Ball Grid Array, T squared BGA is another package that is available today, it is known as Turbo Thermal Ball Grid Array which means, quickly removing heat from the system or from the package. TEPBGA stands for Thermally Enhanced Plastic Ball Grid Array, and then you have HSBGA which stands for Heat Spreader or Heat Slug Ball Grid Array.

So, it may mean the same for different package acronyms, but this can be used by different companies. Then you have VfBGA which stands for Very Fine Pitch Ball Grid Array, MCM-D stands for multichip module deposited thin film, JEDEC is institution which looks a package Joint Electronic Devices Engineering Council.

LCCC stands for leadless ceramic chip carrier, MELF stands for Metal Electrode Face Leadless SMD device, PLCCH stands for Plastic Leaded Chip Carrier with Heat spreader, SOG stands for small outline IC with gull wing leads, TCP stands for Tape Carrier Package, VTSOP stands for Very Thin Small Outline Package, micro BGA is

also known as CSP. So, that completes the type of packages that you will see in the market, or when you are going to use advanced designs you will be using these packages.

And there are much more acronyms that you need to get a custom to, and this is only a glimpse. So, we will continue with some more quiz and some more information in the next session.