An Introduction to Electronics Systems Packaging

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Module No. #03

Lecture No. # 13

Advanced packages (continued)

Thermal mismatch in packages

Current trends in packaging

In this lecture, we will continue with the packages of the previous class. We have seen the types of packages. So, we will take a quick review of what we have seen.

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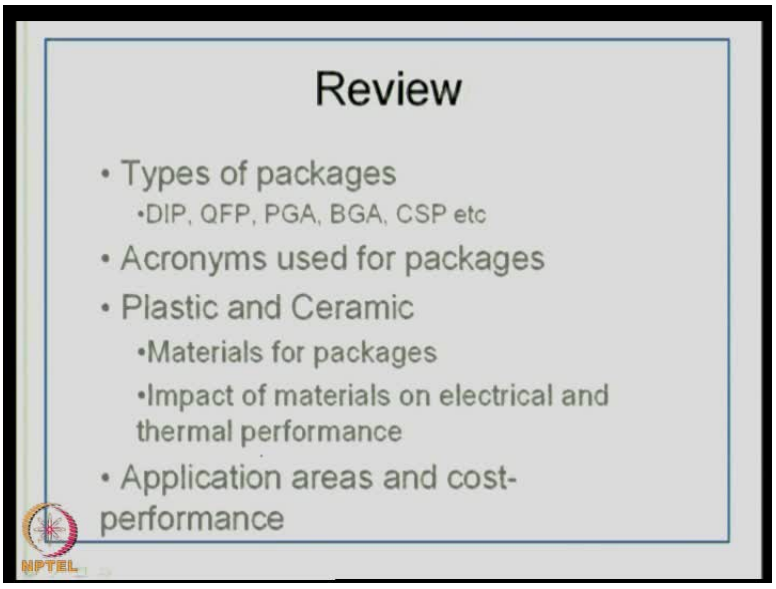

If you recollect, we have seen the types of packages. In terms of illustration, I have shown you all the packages. In terms of life samples here, I have shown you each of

these packages: DIP- Dual Inline Package, QFP- Quad Flat Pack, Pin Grid Array- PGA, Ball Grid Array- BGA, Chip Size package or chips Scale package etc. We have seen all of these packages and we have spent some time on looking at the various acronyms used for these packages because in day to day use, you will come across various acronyms used. Sometimes, different acronyms for similar kind of packages and there could be slight variations on the nature of the package, format the type of lead frame structure available, in the materials that are being used in these packages. They could belong to the same class or the same family of packages. So, you must be well aware of the various acronyms that are being used in this context. We have also seen that basically there are two classifications in terms of materials or from the material stand point, it could be a plastic package or it could be a ceramic package.

So, choice of materials is very important. A designer of a particular package needs to carefully look into the material properties that are being chosen for manufacturing a particular type of package. As you know, these packages are produced in millions and therefore the accurate value in terms of electrical performance and thermal performance need to be studied at length because you will appreciate that there is a large impact of these materials on electrical and thermal performance. We have seen a host of examples for this particular statement.

Now, the packages can be used for different application areas like as I said before, you could use a plastic package for a different application and a ceramic package for another application, although the functionalities in terms of electrical function could be the same. It could be a microcontroller package in a QFP format, but in consumer electronics, we could probably go with the plastic, whereas for a automobile application we could going for a ceramic package. So, application area and cost versus performance are the key drivers for the package selections and also basically for the package manufacturing.

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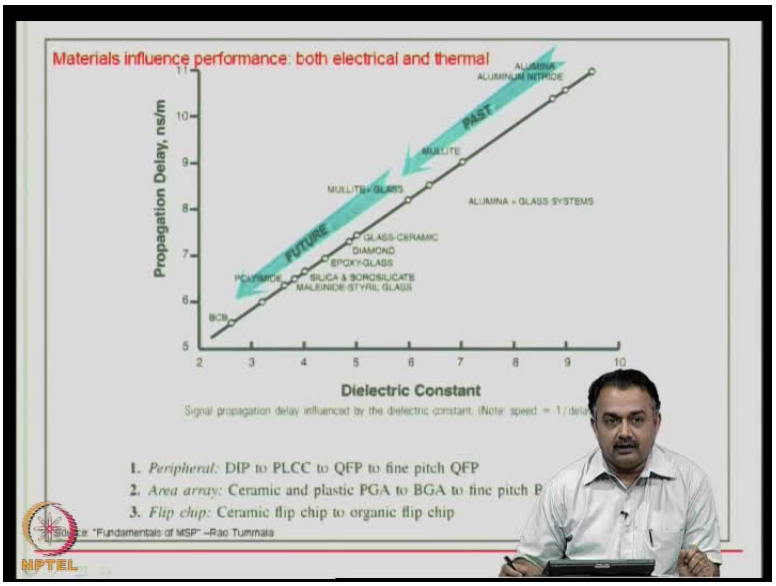

So, we will now go ahead with the other topics in packages. So, I want to emphasize here that materials influence performance; both electrical and thermal if you look at this particular graph which is basically indicating dielectric constant property versus the propagation delay. As you know, the propagation delay is a very important factor in looking at the electrical performance of a particular package because, if you choose a particular dielectric material, then the propagation delay is going to be dependent on the dielectric constant of the material.

So, this graph will show you that on the extreme end, we have the ceramic substrates, which have higher dielectric constant and these were used in the past. So, in terms of thermal performance, probably they will be at the receiving end, but in terms of electrical performance, there could be some shortcomings in terms of the properties. Again the dielectric constant is not the only deciding factor, but it is a key factor in selecting the substrate or the package material.

So, as you move along, in today's technologies and today's manufacturing, we have seen a lot of composites are being used. For example, the glass ceramic materials, then we have the epoxy glass whose dielectric constant varies in terms of added fillers - between 3.5 to 4.2. So, we are using a lot of epoxy glass substrate and silica is being used; borosilicate. Then polyimides have been used for high performance applications. In terms of dielectric constant, it may be superior, but if you look at other properties, for

example, moisture absorption it could have higher moisture absorption. Therefore, it could decrease the electrical performance, but at the same time, it is a future material and also it is a current material. It could be a future material and another material that is being used today in the semiconductor manufacturing is BCB.

BCB is Benzo Cyclo butane, whose dielectric constant is close to 2. Therefore, you can expect better electrical performance. Electrical parasitics could be very less, if you are thinking of using it as a very thin dielectric in manufacturing. Here, dielectric materials choices could relate to substrate, thin dielectric layers used in the buildup of these package substrates and it also could mean encapsulation. So, these are the areas, where dielectric materials could be used.

So, we have seen peripheral array packages, area array packages and bare die called a flip chip or a C4 interconnect. If you look at all of these classifications, we are moving towards organic substrates and organic packages. Firstly, because it is cost effective and secondly, we are able to synthesize organics materials with better dielectric materials to achieve better electrical performance compared to the expensive ceramic materials.

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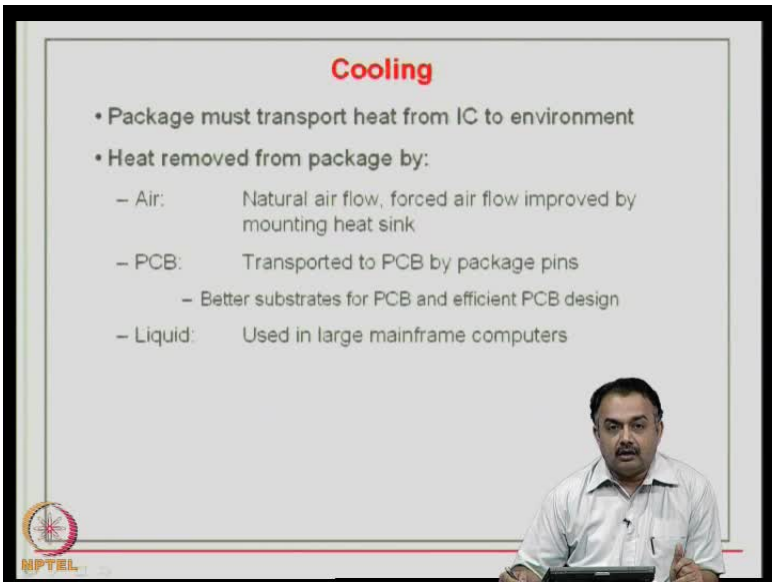

Another important aspect, when you look at packages would be the cooling phenomenon. So, when a die is packaged and connected to the external world by means of lead frame structure or a solder ball arrangement in a area array format. Whatever be the case, the package must transport heat from the core die to the environment. So, heat

from the IC to the environment should be faster, quicker and effectively removed because, if you can look at the previous class, what we have discussed is that when heat emanates from a die, when you power up a particular circuit. There is silicon die and if there is a heat buildup, there can be die crack because of heat accumulation and there can be fatigue on the interconnect structures. So, it is a combination of silicon die and if you are using an organic substrate to place the silicon die, then there is going to be problem in terms of warpage due to continuous thermal cycling at the organic substrate. Therefore, this heat has to be quickly removed effectively.

Now, heat can be removed from the package by air. You have seen in desktop computers that there is a fan. You are removing the heat by forced airflow- by mounting a fan. There is also a methodology of using a heat sink. So, these are the two common methods that you will see, where either you can depend on natural air flow, but in some cases, if the quantum of heat that is dissipated from the active device is large, then you will have to look at forced air flow. That can be done by mounting a heat sink or using a forced cooling by a fan or a similar device.

Now, the printed circuit board or the PCB, on which the components are mounted and on which the packages are mounted, will also have to behave as a heat sink. Therefore, the package pins, the leads or the solder balls in the case of a BGA or a CSP will have to transport this heat to the PCB, so that the heat at the die stage is quickly moving through the package substrate, through the package pins and then to the PCB, on which the host of components are assembled or mounted. Therefore, you must look at printed wiring board not just as a rigid substrate or a flex substrate that is used from assembling your components. It should also be considered as substrate that can take care of cooling, removing heat. Therefore, PCB design today, involves a lot of thinking by the designer, engineer to place your components in such a way that your PCB is not affected. PCB effectively acts as a good heat sink. There are other methods of designing a PCB, where from the package pins; you can remove heat through copper layers and that can act as a heat sink, embedded in one of the layers of the printed wiring board. You could also use liquid. Big companies like IBM, have employed liquid cooling in main frame computers or high end servers etc, where it is expected to have lot of heat generated from the various active devices. Therefore, you should be able to remove the heat quickly from the high-end servers.

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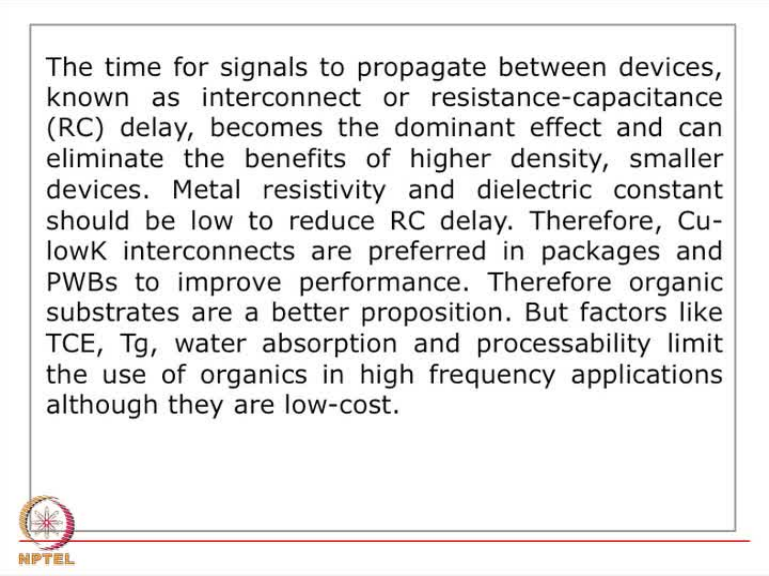

Now, there is also another methodology, where you are going to protect the die and the interconnects. Remember, this is a bare silicon die and you have the first level interconnects. At the back of the mind, you must always think about packaging as a means of protecting the die, protecting the first level interconnect. You are having the package in a format that is now available for the second level interconnects on printed wiring board. I think this big picture should always be there during this discussion

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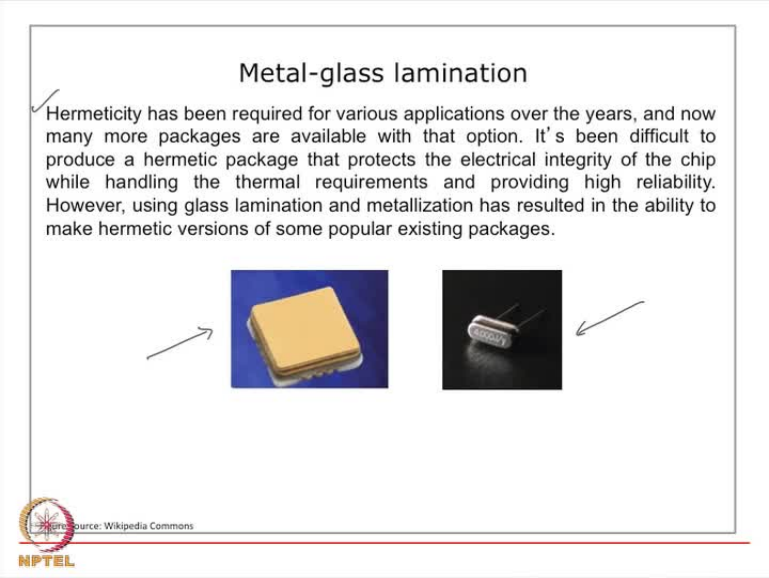

Now, what is metal glass lamination or in other terms hermetic ceiling? I am going to

introduce a term called hermetic ceiling or hermeticity and that is used for some types of packages. This technology has been there for few years now. Hermetic ceiling means- air type ceiling and that means the die and the first level interconnect are completely sealed. In the case of plastic packaging, for example, it is possible that the plastic material can absorb moisture. Therefore, your die and the first level interconnects could be exposed to some kind of a moisture. In hermetic ceiling this is not allowed, the die and the first level interconnects are completely sealed, checked for air type ceiling after the process is over. It is definitely expensive compared to the normal plastic encapsulation or a ceramic encapsulation.

Now, it is difficult to produce a hermetic package because of the cost involved and the test involved. It protects the electrical integrity of the chip, in terms of thermal requirements and in terms of providing a high reliability for the package. In certain application areas like space, avionics etc; this is definitely a requirement. They use hermetic sealed packages in specific demand for certain circuits. Therefore, the picture that you see here is a typical example of hermetically sealed packages. They are popular, but the volumes may be much less.

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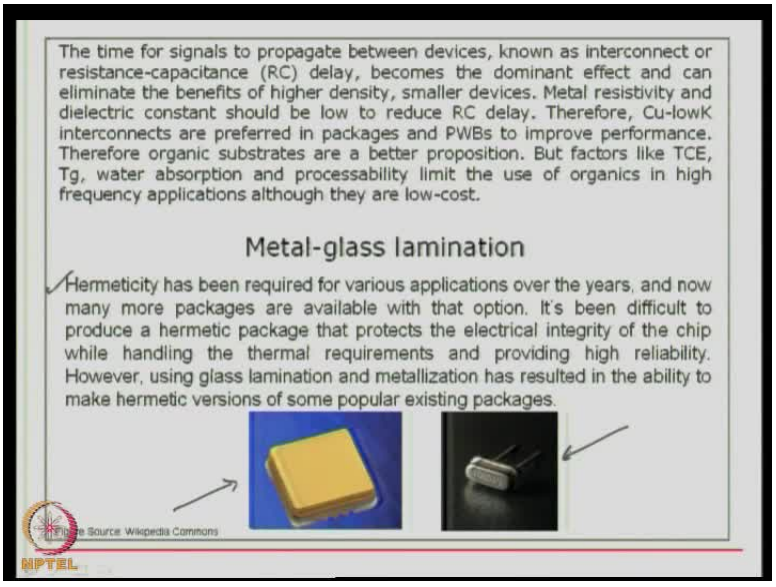

Now, another important aspect that I would like to discuss at this point of time is that the time for signals to propagate between pins, devices or active processes. For example, known as interconnect or RC delay, most of you are aware of this term Resistance

Capacitance delay. It is a very important effect that takes a dominant nature, when you power up the circuit. It can eliminate the benefits of higher density, smaller devices. Therefore, metal resistivity and dielectric constant should be low to reduce RC delay. So, this becomes a very important factor in selecting the dielectric constant for packages. This is also important in the second level interconnect stage. Therefore, if you look at printed wiring board, you would also like to choose copper-lowK combination of interconnects. It means copper material and then the low dielectric constant materials are used in-between interconnects have to be very low. Dielectric constant has to be very low. So, this is preferred in packages and printed wiring boards to improve the performance; electrical performance. So, these can be achieved with organic substrates. Therefore, organic microelectronic packages are a better proposition today, not just because in terms of cost, but other factors like the low dielectric constant, low moisture absorption or water absorption, process ability and then factors like TCE- Thermal Coefficient of Expansion and the glass transition temperature - Tg are all important properties that a designer has to look at, when you decide on PCB substrate and also packages that are going to be used for your applications.

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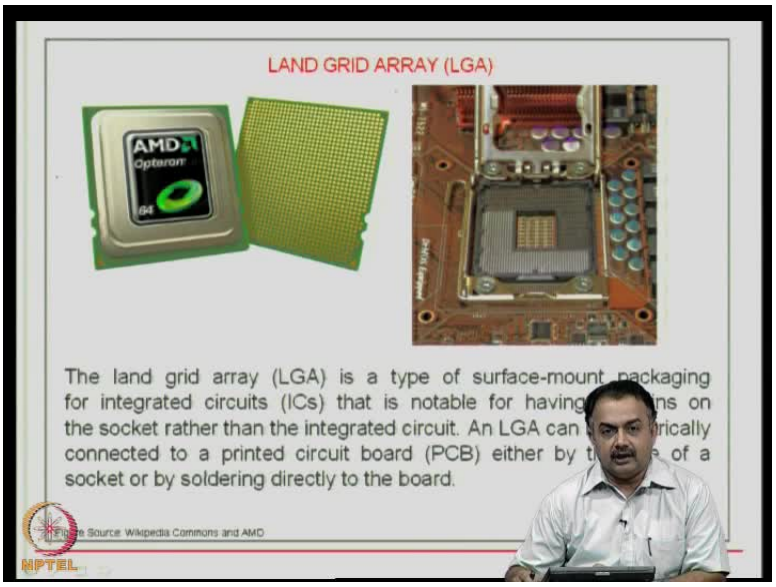

I am going to introduce another package, just like your pin grid array. Here is what is called a Land Grid Array - LGA. So, companies like AMD and Intel are now bringing microprocessors in the format called LGA- land grid array. So, what is a land grid array? It is very analogous to your pin grid array, but let us look at the definition and the

structure of a land grid array. Land grid array is a type of a surface mount package. So, the first information that you get is- it is a surface mount package, it is not a through hole package. It is used for making microprocessors integrated circuits that have high pin count greater than let us say 700 pins or I/Os. It is notable for having the pins on the socket rather than at the package substrate. so, that is the basic difference that you get.

If you look at this particular picture (Refer Slide Time: 19:20). This is the top of the package and this is the bottom side of the processor. Now, if you look at this particular picture here, there is a socket mounted on the printed wiring board or the motherboard, as you call it in a desktop application. So, we can see here; there is a socket that has got the pins. So, compared to other pin grid array, for example, where you have the pins on the device. Here, you have the pins on the socket. In this particular arrangement here, you can see are gold pads- gold flat lands. Now, this will register correctly into the socket and like a clip, it will get attached to the pins on the socket. You can use this lock assembly; mechanical assembly. So, you can see that it is a huge assembly here and after the IC has been placed in the socket, you can close the lid and then make sure that there is complete perfect registration to the I/Os of the pin and the processor.

So, you can imagine that a printed wiring board contains this socket that is mounted. Then it is electrically connected to the land grid array package by using a socket, but the datasheet also says that you can solder it directly onto the printed wiring board. As you know this is a very expensive package, it could be possible that you have to repair and rework on this active device because of failures that could be expected. Therefore, it is easy to use a socket, do repair and rework or change the processor rather than soldering it directly onto the board because as you know once you do a direct soldering on the board, it is going to be very difficult to repair and rework as you have to remove all the 700 plus pins. You know to remove the socket carefully without damaging the processor is very expensive. So, this is a land grid array. You can compare it with the PGA. So, today's processors are coming in LGA format. PGA is no more a common methodology for mounting microprocessors on motherboards.

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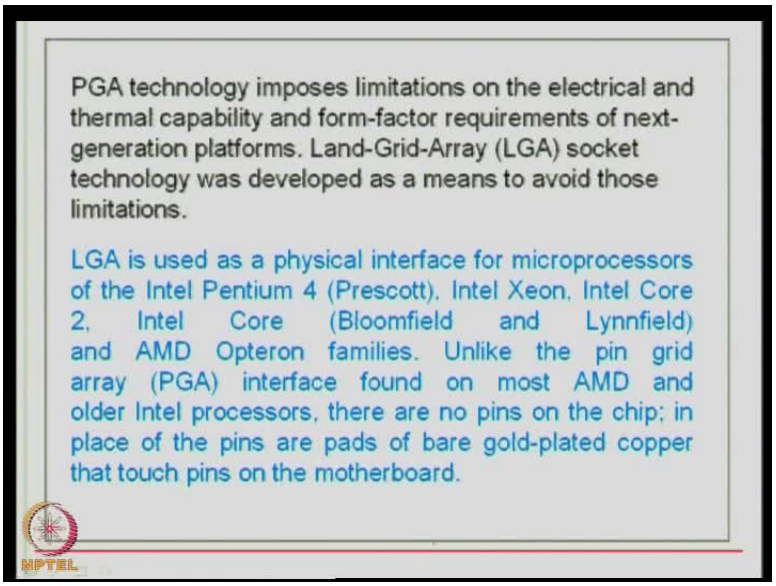

Now, PGA technology imposes some limitations on the electrical and thermal capability and also the form factor requirements of next generation platforms because of large size, there is huge mechanical area that is required. As you know, if you look at this picture (Refer Slide Time: 22:46), there is a large keep-off distances. You can see here, where you cannot really do any routing or any other assembly. Therefore, in terms of space requirements on the board there are also some limitations, but it is a key device and therefore that particular aspect could be ignored.

LGA socket technology was developed to avoid all the problems that were encountered with PGA. Especially, in terms of larger pad area, contact area and so on. So, LGA is used as a physical interface for microprocessors of the Intel Pentium 4 family, Intel Xeon, Intel core duo processor, AMD Opteron families of microprocessors and so on. Now, unlike the PGA interface found on most AMD and older Intel processors, there are no pins. The material that is used for the LAN's are gold plated and so this is a major requirement. All the contacts have to be gold plated because of the excellent resistance, contact resistance and the wear and tear is very low in the case of gold compared to other metal alloys. Therefore, gold in very small thickness on top of the copper is an important requirement.

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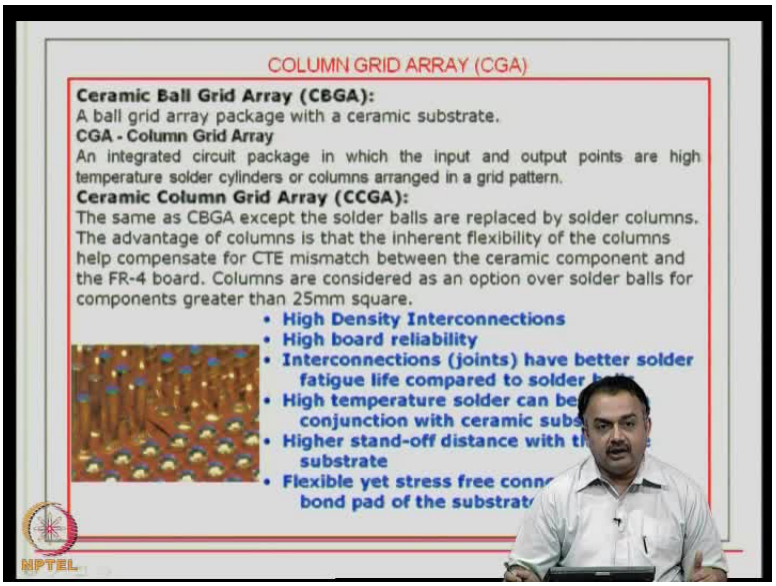

The other package that we will get introduced to is known as a column grid array. Now, a CBGA is known as a Ceramic Ball Grid Array, which is basically a ball grid array with a ceramic substrate. so, the reason why I introduced this particular acronym is- this is CBGA and now we are getting introduce to an acronym called CCGA- Ceramic Column Grid Array because column grid array mostly comes with the ceramic substrate packaging. So, a ceramic ball grid array is basically a ball grid array - BGA package with the ceramic substrate and so that is very clear. Now, we will look at defining, what is a column grid array? It is basically an IC package in which the I/O pins are high temperature solder cylinders. So, basically, we are going to see solider cylinders. if you look at this picture here and if you look at the bottom of the picture, this is basically solder balls. These are columns; solder columns and these are arranged in a grid pattern like your ball grid array.

So, a ceramic column grid array is the same as a CBGA, except that the balls are replaced by solder columns. The advantage of using columns is that it could be used in cases or in applications, where you need help to compensate for the CTE mismatch between the substrate and the ceramic component. So, because, you are using high temperature solder and the length of the column is definitely larger than the solder ball height, you get a relief over the CTE mismatch. We normally get concerned with in a organic package attached to a silicon die like in a BGA. Typically, these are used for very large packages and there is no point in using these for a very small die having a few

columns. So, typically, it used for application areas like military and so on. So, this particular property can be well utilized.

What are the features of a column grid array? You get high density interconnections, high board reliability, the interconnections have better solder fatigue life compared to a solder balls, which is expected because of the length of the column. You can use high temperature solder in conjunction with the ceramic substrate because there is good compatibility and the thermal performance. The application areas could be increased to higher temperatures if required. There is a higher standoff distance with the base substrate and this is also very important property.

If you can imagine, there is a substrate and BGA solder ball. There is a very small gap between the die and the printed wiring board substrate, but in the case of column grid array, you can expect a large gap between the silicon die and the ceramic substrate that you are using. It could be a printed wiring board or it could be a ceramic substrate in terms of a wiring similar to a PWB. Therefore, this high stand of distance could be an excellent factor in thermal management because it can take care of the heat dissipating to the environment through the solder columns. It is flexible, yet stress free connection with the bond pad of the substrate. So, you will see that CGA is not much around in terms of popularity, but if you are looking at specific applications with thermal management as a key factor, then you can go in for a column grid array.

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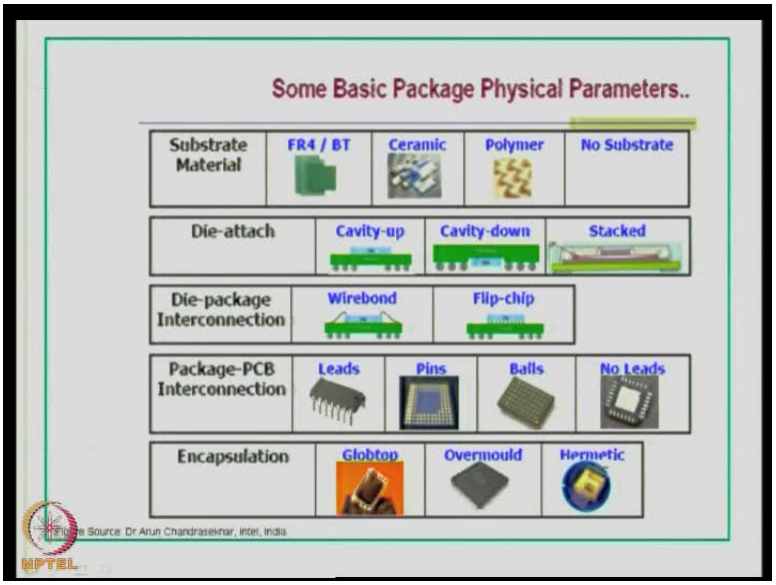

Now, we will look at some basic physical parameters of the packages. This is like a summary of what we have seen so far. I have introduced you to various substrate materials. We have seen, what an FR4. This is basically an organic substrate. FR4 is basically a flame retardant class four material. You know, what a ceramic substrate is. Polymer could be used for specific properties like low dielectric constant and so on. If you are very particular, polymers of different types could be used as a substrate material in the package buildup. You could have no substrate and so is this possible? Can you have a package with no substrate? When you say no substrate, there is no platform for the die to sit on. If you look at the literature, some packages have been made with no substrate; in the sense that there is a die, which is immersed in an organic resin and then cured. The interconnects in terms of lead leads come out from the organic resin.

So, specifically they do not use a substrate, but this is very rare. So, we are going to depend either on organic substrate or a ceramic substrate or specific polymer material. Now, the second point that you have to look in terms of components of the package is- what is a type of die attach? Is the cavity up or is the cavity down to house the bare die? So, this particular configuration is very typical of a BGA. This could also be a BGA, but here, you can see that the cavity is down and the die is closer to the solder balls, than away from the solder balls in the case of a cavity up configuration. So, this is very difficult to manufacture, in the sense that you need to create a cavity in the substrate. You could also have stacked configuration and that is one die over the other interconnected to a common substrate. We will look at the die to package interconnection and very common today is the wirebond and another more popular choice today is the flip chip. So, the particular cross section that you see here (Refer Slide Time: 32:00) is a wirebond BGA. This is a C4 or a flip chip, BGA and what you are seeing is basically a cross- section.

Then comes the package to PCB interconnection. What are the choices available? We have leads that could be used like your dip packages or QFP's .Then you have pins like your pin grid array, solder balls in the form of… In the case of BGA or a CSP, you could have solder balls and you could have no leads. Typically, you will see this in quad flat no lead packages or QFP packages. Here, you can see that the electrical interconnects are typically flushed with the package surface. So, you cannot really see leads protruding out or interconnects protruding out of the surface of the package area. The next one that you

are going to look at in the package is- how do you protect it? What is the encapsulation that is normally used? So, you can use a glop top, if you recollect what I have said before, you can use glop top in a chip on board configuration. Overmould is very common in all packages, whether it is a DIP package or a QFP and one that we have seen today is a hermetic ceiling, where you use a metal glass lamination. So, if you can breakup or if you can look at the cross-section of the package, you will see all of these. The first is a substrate material, then what is a die attach? Third is the die to package interconnection. Fourth is the package to PCB interconnection and fifth one is the encapsulation.

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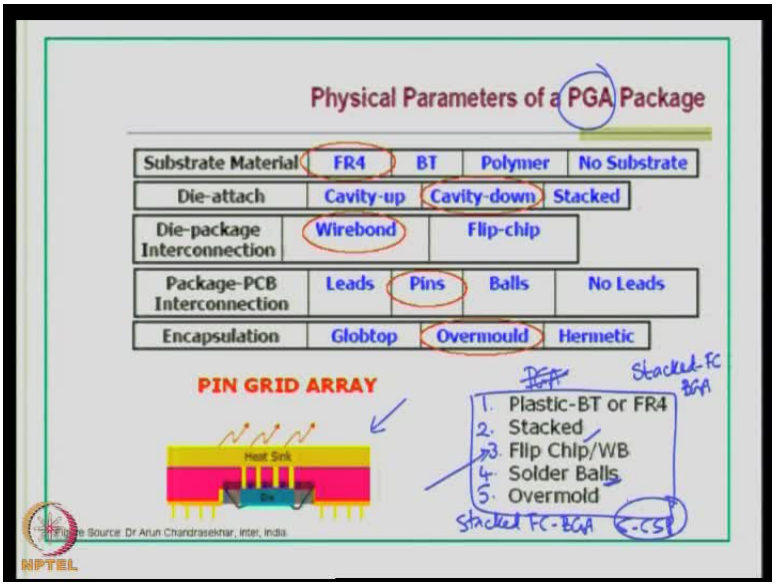

If I give you a kind of quiz, for example, if I look at this particular chart and I have marked certain identities in red. It is assumed that there is a substrate material in which we have used an FR4. The die attach is a cavity down configuration, wirebond is the die to package interconnection. In this particular package, we have used pins to connect to the PCB. Overmold is used and if I ask you to identify this package, you should be able to come up with the answer that this is a PGA. So, you can easily identify these five parameters. So, this is the cross-section of a pin grid array with a cavity down. Similarly, if you look at this particular clue, here we have it as a quiz. So, if I ask you to identify from this given information that is there is a substrate material, which is plastic and then there is a stacked die attach configuration. The third one is flip chip or wirebond could be used. For example, let us assume it is flip chip. The fourth one is package to PCB

interconnection and that is solder balls. The fifth one is an overmold and you must be able to identify, what package it is.

For example, given this configuration, it could be a stacked configuration and that means there are two dies or more, stacked one on top of the other. You can see tense in a Solder Ball and therefore it could be a BGA. If you are using a flip chip, it could be a flip chip and so it could be a stacked flip chip, ball grid array. If you actually know the dimensions, it could also be a stacked chip size package. You must now be able to identify packages from such information given.

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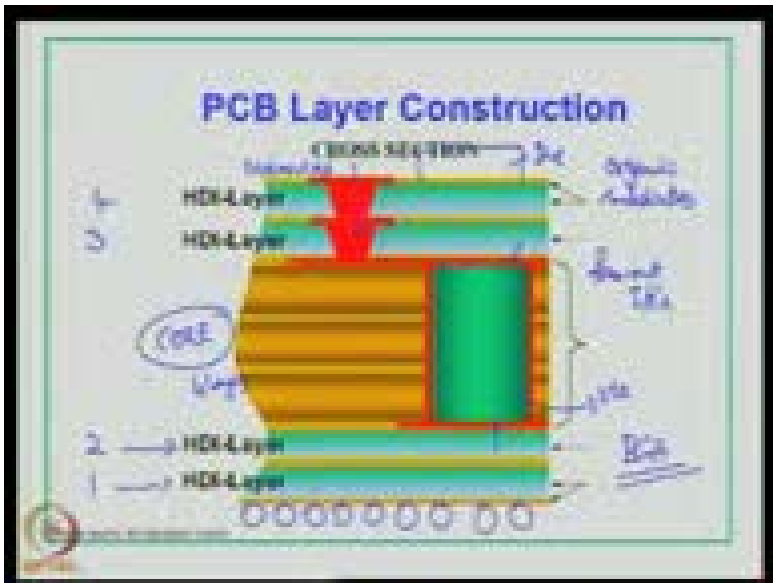

We have been talking about printed circuit board or organic substrate, which resembles a printed circuit board in these packages. In a BGA package or a CSP, for example, you must know these organic substrates are used, which support the die have very high density interconnect structures. So, I want to pull out some of the slides, which we discussed in the technology to give you some idea about what a cross-section of organic substrate will look like. It is similar to a PCB configuration, but here basically, in a package substrate, you will look at basically, fan out of the IOs from the die to this particular package and then finally, you might end up with solder balls. If this is the cross section of package, you might have a die here (Refer Slide Time: 37:35) and this is the configuration of the package. So, if you look at a cross-section, you will see multilayer and this could be layer 1, layer 2, layer 3, layer 4 and so on. You have a core

and this core will have 1,2,3,4 layers. So, typically, it could be a 8 layer board or 8 layer substrate. You have a via here, which is fairly large and which interconnects from this layer to this by metallization using copper. Here, you will see, all the additional built up layers are connected by using microvias and these are vias, which are very small. I think I have introduced, what a via and a microvia is. These dimensions are very small of the order of 125 microns or less. Therefore, you can expect in a BGA, this kind of a cross section and buildup.

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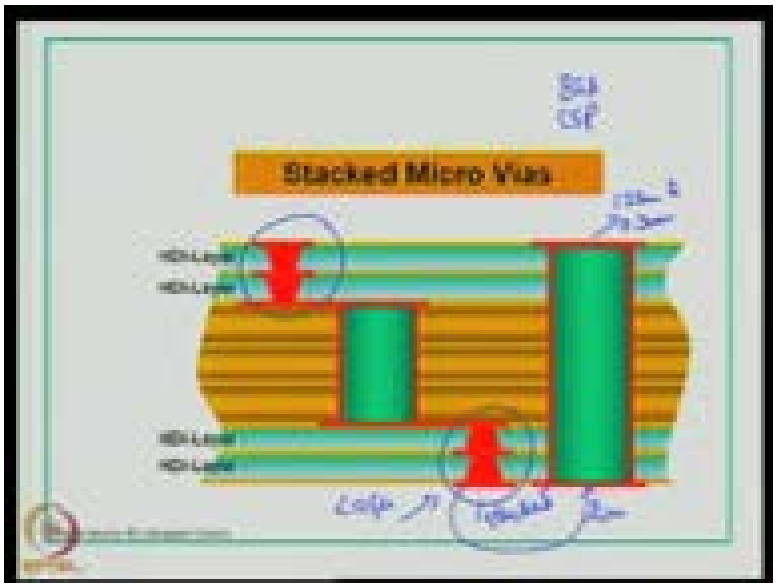

This is an example of how the micro vias are staggered. So, this is a plated through hole or printed through hole and this is a via. This is also a via and you can see here the vias are staggered. Here, also we can see that the vias are staggered. So, in the earlier example this could be a stacked via configuration, whereas here it is a staggered via configuration. So, here again we can see this is stacked one on top of the other, which actually resembles something like this, (Refer Slide Time: 39:18) but the dimensions are very small. In this case, it is less than 125 micron, whereas this could be anywhere from 1.27 mm on the lower side to 0.3 mm mechanical drilling. So, this is again an example of a stacked micro via configuration, you can expect these kind of configurations in a BGA or a CSP.

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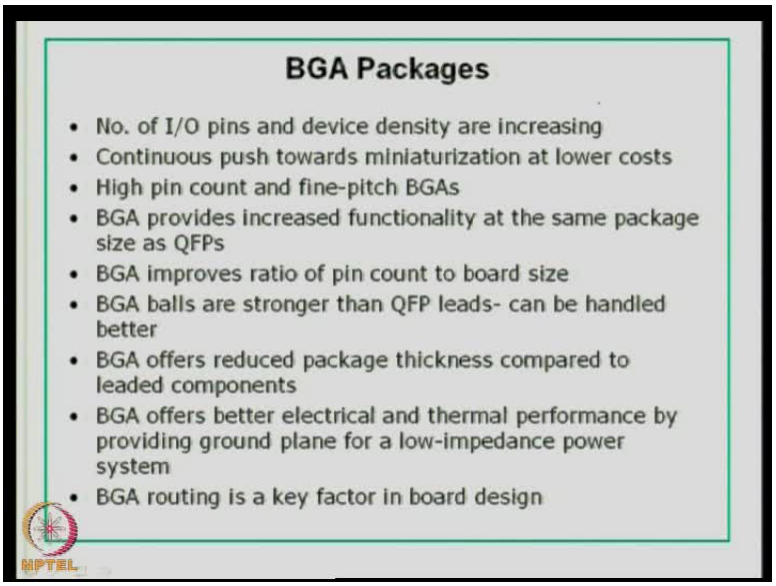

So, a BGA package, today is a work cross of the industry. We will finally look at the summary of BGA packages. In a BGA package, the number of I/O pins and device density are increasing. Today, you can get BGA packages of the order of 1100 pins or more. So, how to handle them? There is continuous push towards miniaturization at lower cost by using organic substrates. High pin count and fine pitch BGA's are the order of the day. So, it does not mean that you can have a high pin count, but large pitch. It has to be fine pitch. When I say fine pitch, we are talking about 0.55 mm BGA's. Below 0.55 mm, it is classified as a CSP. BGA provides increased functionality at the same package size as QFP's because of these two factors fine pitch and multilayer buildup. BGA improves ratio of pin count to board size because of fine pitch. This is not possible with QFP's. BGA solder balls or interconnects are stronger than the QFP leads and therefore it could be handled in a better way, in terms of assembly and testing.

BGA offers reduced package thickness compared to leaded components, which is a fact BGA offers better electrical and thermal performance by providing a ground plane because if you look at the previous slide, if this is the CSP or a BGA configuration, you can assign a ground plane in one of the inner layers here. Therefore, if your die is sitting on top of the layer you can have your ground interconnections routed properly for much better electrical performance. So, BGA design is a very important step and BGA routing is key factor in board designs. So, we are going to discuss when we look at compute rated design for printed wiring boards. We will look at BGA routing in a much detail

fashion.

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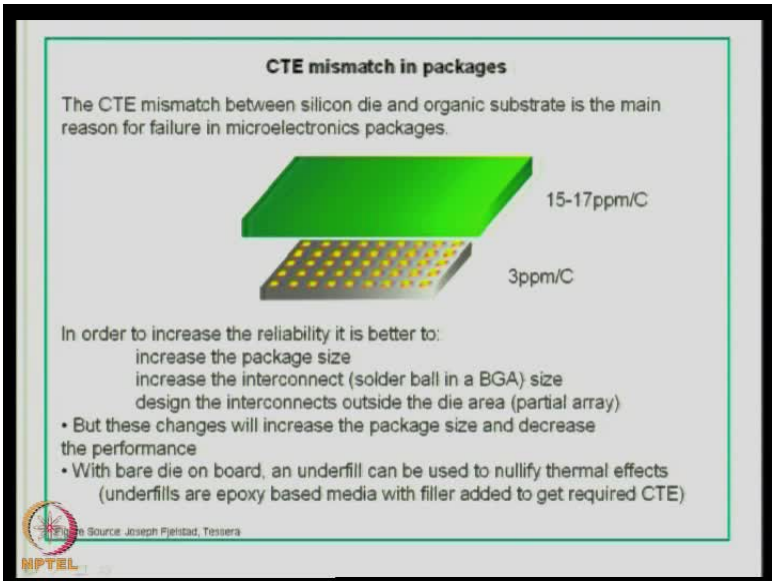

Now, the next aspect in packages is CTE mismatch and that is coefficient of thermal expansion. So, as you know, when you power up a device there is… and when you use a package, which uses an organic substrate, there is going to be a thermal mismatch between the silicon die and the organic substrate. One of the reasons or failure in micro electron packages is the CTE mismatch. Now, if you look at the slide; this is a typical example, we have seen in numerous cases like this. There is a silicon die here, this is the organic package and it is a very common thing now. You will see in low cost packages and you can see that the CTE values are 3 ppm per degree centigrade for a silicon die. For the organic packages, it varies between 13 to 17 ppm per degree centigrade. When you power up, there is going to be mismatch.

We have also seen that in such cases, the reliability is going to shrink down. So, how do you increase the reliability? It is better to increase the package size, but that does not justify because we are always looking at lowering the package volume and size. If this is going to be a problem, you have to increase the package size, increase the interconnect or a solder ball diameter or size in a BGA and design the outer interconnects outside the die area. It means, if you have the arrangement of the solder balls, this is the die and do not place the solder balls at the back of the package, underneath the die area. So that it impedes in the thermal performance dissipation of heat. So, this is a key factor. These

changes will increase the package size and decrease the performance with bare die on the board. You can use a underfill and as I said, it is basically a material that is used in between the die and the substrate to nullify the thermal effects. The CTE mismatch can produce and typically underfills are epoxy based media with different fillers added to change the CTE. So, typically you can use materials, which have a CTE in between the die and the substrate.

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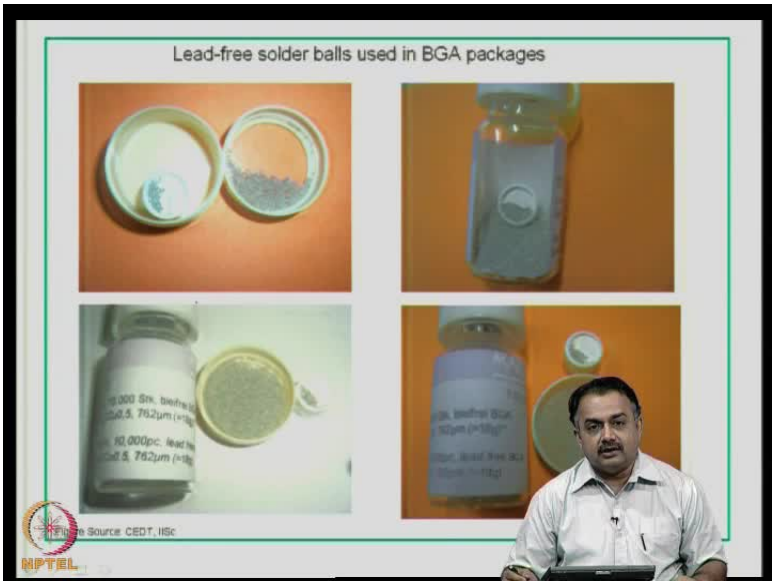

Now, the BGA packages or CSP packages will use interconnects based on solder balls. Here, I have shown some photographs of solder balls that are available in the market today because, when you use BGA packages, sometimes you want to reconstruct the BGA arrangement. If there is a problem with repeated failures because of repeated thermal cycling, there is a failure in the BGA package. You want to remove the BGA package, mount another one or repair the existing BGA because of a poor solder interconnect.

So, you can see this is BGA solder balls. Typically, the diameter of this is about 762 microns close to about 0.8. So, you can use this for a 0.8 pitch BGA. If you are working on a prototype, you must be able to prepare and rework a BGA package. BGA solder ball is now available in lead free. Earlier, we were using a lot of lead based solder balls, but today lead free materials are available in the market. As you are aware of legislation, we are now going to use only lead free materials.

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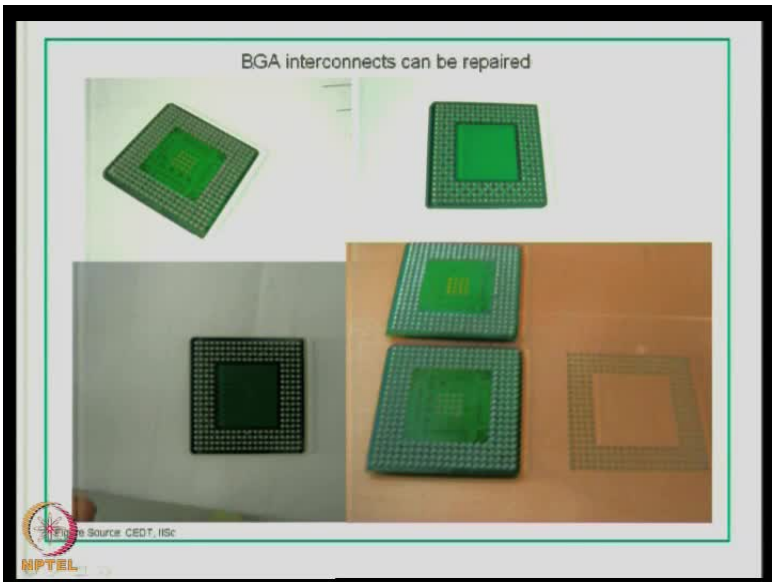

Now, BGA interconnects can be repaired. If you look at a through hole component for example, you have a dip package, it is very easy to disorder and put another component in its place through the through hole. Solder it back on the other side, but this is a surface mount device, surface mount component assembly. We are going to deal with it much later. To remove the curiosity, I have included two slides here to say that although BGA is expensive, it can be repaired today. So, we are going to discuss SMD and BGA assembly in much detail, but at this particular slide, this has been done at CEDT. Here at the Indian institute of science, we have made the slides to impress you, how a BGA interconnect can be repaired. So, if you at this picture here (Refer Slide Time: 47:52) and this picture here, there is a stencil of the solder ball arrangement of a BGA. So, we can print a solder paste through this stencil on to this particular BGA package, where the older solder balls have been removed. Now, once the print has been done, they go through a reflow process in an oven at specified temperatures pertaining to the melting point of the solder material. As you can see here, these materials have reflowed and nice solder balls have been formed at the respective designated spots with the correct pitch. So, you can remove the interconnects of the BGA, when you repair and replace with new solder balls, but this is a method, where we have used a solder paste as the starting material to realize the solder balls.

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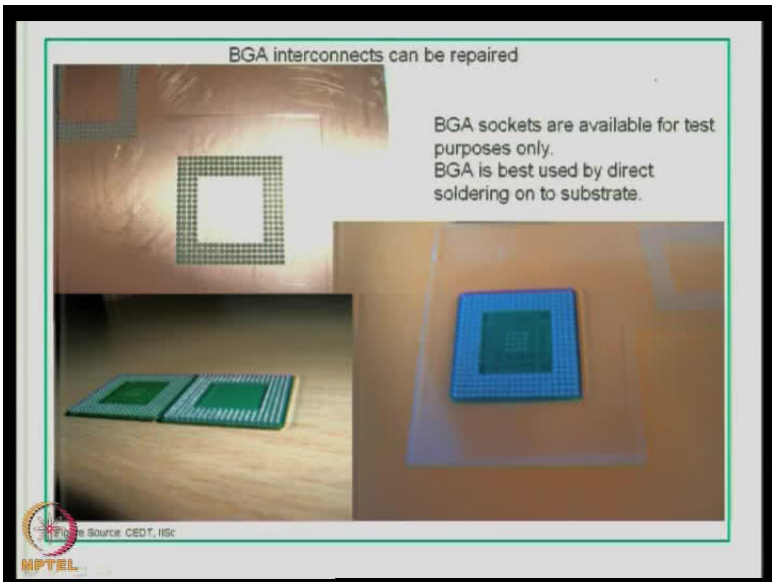

If you look at this particular slide here, we have used another stencil pertaining to the arrangement of the BGA. The distances are well measured here. We have used solder balls itself. I have shown you the previous picture of a solder ball, these have been placed on these holes that have been drilled on a thin laminate structure or a thin polyester sheet like here. You can see here, which is used for alignment. Once the solder balls have been placed, they undergo a reflow process. During the reflow process, the solder ball melts and gets attached to the pads on the substrate designated for these solder balls. So, the grid is established beautifully and you can see there is no solder bridging at all.

So, this is a BGA interconnect directly done on to a organic substrate or even a ceramic substrate. Now, you could ask me a question, why cannot we use a BGA sockets, as we are using for a DIP package or a QFP package. BGA sockets are available in the market, but these are used for test purposes and for prototyping. For actual volume manufacturing, we normally do not use a BGA socket because it is heavy; it occupies more space on the board. Although, repair and rework could be easy, but today the technology of assembling a BGA device on a board is well established. Yield is close to 99 percent or more. If you know the right technique of repairing and rework, you still can make perfect BGA interconnections.

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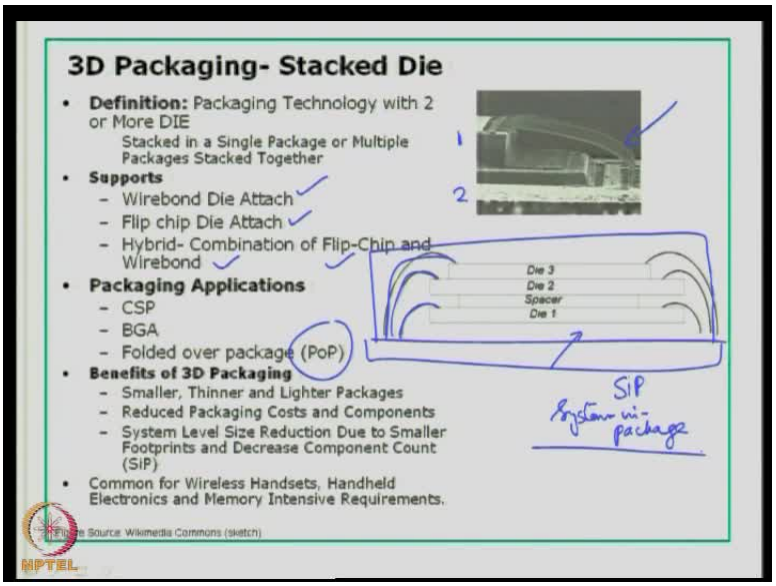

Now, what next after BGA? We are now looking in current global scenario, 3D packaging or stacked die configurations in packages. What is the definition of this packaging technology with two or more die stacked one on top of the other? It is 3D packaging. So, you can stack it in a single package or multiple packages or it can be stacked together. So, this is 3D packaging or stacked die. The aim is to save space and the aim is also used to bring two or more die and build it as a custom built package for a particular functionality, when all the three packages or two packages are working in unison. So, if you look at this definition, I think you are clear about stacked die configuration, then what is the support in terms of first level interconnect? It could be a wirebond attachment, it could be a flip chip die attachment, it could be a hybrid combination of both flip chip and wirebond. If you look at this picture here, you could have this wirebonds coming over here onto the base die coming from a second die. You can have die 1 and die 2. The die 1 is sitting on top of die 2 and interconnected to the base die. Both the die or two or three dies can have a common substrate onto which the connections… For example, if you look at this sketch here, you can have die 1, die 2 and die 3 and you could have a common substrate here. The wirebonds are drawn to the common substrate and then you could have a package done for this. So, this is really a custom built packaging.

Now, the application areas are you could make a CSP and out of it, you could make a multi stack BGA out of it. A new technology called package on package- PoP. It is now

available, where you could mount already built two packages; one on top of the other and establish a connection. These are used to save space with high level of vertical integration. The electrical density is very high, the thermal performance have been tested and the benefits of 3D packaging. It is smaller, thinner and lighter because we are using bare die. We are not using multiple packages and mostly reduces packaging, cost and components because all assembly is done on a common substrate system level. Size reduction is due to smaller foot print and decreased component count. So, typically these kind of packages are known as SIP system in package. SIP is generally not available off the shelf, you have to custom build a SIP package and the application areas for these are the wireless handsets, handheld electronics and memory intensive requirement.

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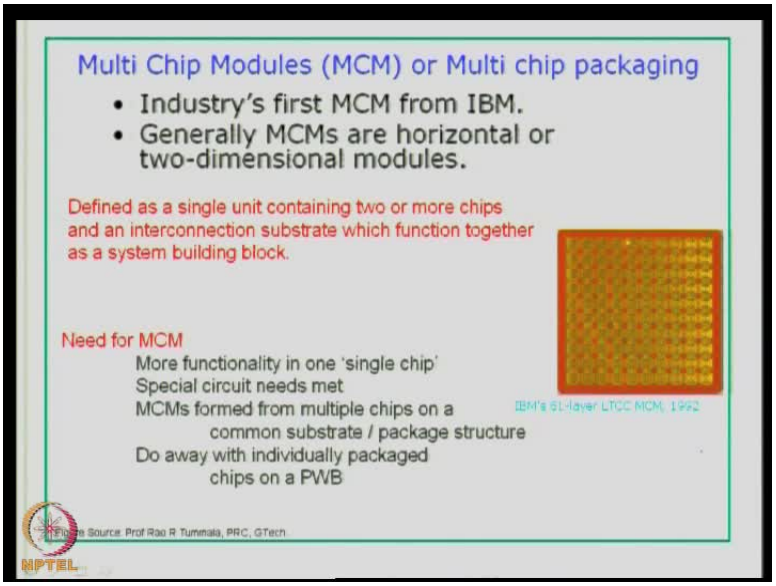

You can use 3D stacking or multiple die stacking for creating system in package configurations. Now, we will move into multi chip modules- MCM. So far, we have discussed single chip modules. Now, we will move into Multi Chip Packaging- MCP or its also known as Multi Chip Modules- MCM. As the name indicates, a single unit of multi chip module will contain two or more dies. These dies will be interconnected on a common substrate and this will function as a system by itself. So, this is a very important system building block of a major system.

So, it could be a subsystem, but it contains all functional units integrated together. So, multi chip module is basically going to integrate a lot of devices together. It is going to

reduce the space and it is going to increase the component density or the pin density of a subsystem. So, Industry's first multi chip module came from IBM. Generally, MCM's are horizontal or two dimensional modules and that means look at this picture here (Refer Slide Time: 56:08), this is a photograph of IBM, 61 layer low temperature co-fired ceramic substrate, multi chip module manufactured way back in 1992. You can imagine 61 layers built on the top layer. You can see a host of IC's, number of IC's stacked together and interconnected. So, it is a 2 dimensional module and so what is a need for an MCM? You build more functionality in one single chip, if you can call it as a single block special circuit. Requirements are met by using this because of certain functional requirements, multi chip modules from multi chips are on a common substrate. Therefore, you can choose a substrate that has a very good property and that suits the various functionalities that are embedded in the module. You can do away with individually packaged chips on a printed wiring board.

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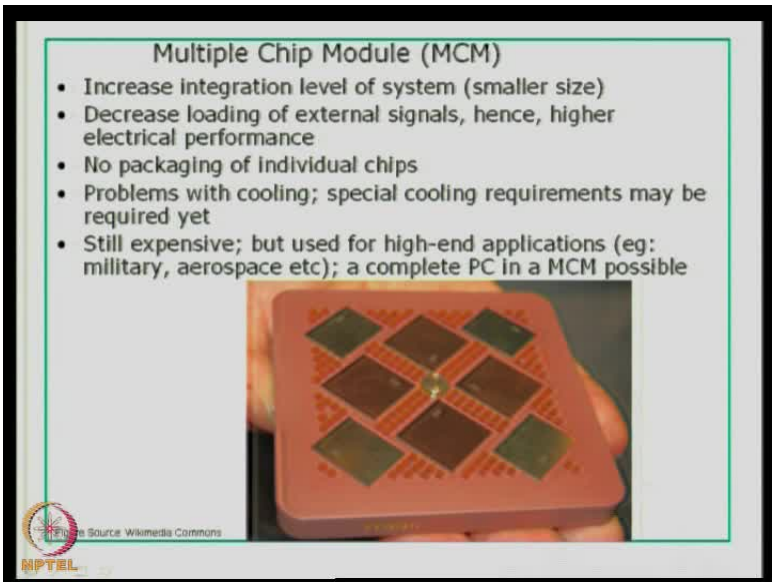

So, you can look at this picture here. This is an example of multi chip module and again some of the salient features of multi chip module are - there is no packaging of individual chips, problems with cooling is a big deficiency, but special cooling requirements may be required and that can be built, including liquid based cooling. There is definitely an increased integration in the system and that is how you reduce the size, yet it decreases the loading of external signals and hence higher electrical performance. It is expensive compared to a printed wiring board. It is expensive because of the

substrate. It is a ceramic substrate that is expensive, but it is used for high-end applications like military, aerospace, avionics etc. Therefore, it is bound to be expensive; for example, if you can build a complete PC in an MCM, then that is great. You can use a single substrate to build complete PCB with all the inbuilt functionalities of a PC. Although it is expensive, multi chip modules are required for various applications today. So, I will stop here and we will continue with the further aspects of multi chip module in the next class.