An Introduction to Electronics Systems Packaging
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Lecture No # 12
Commonly used packages and advanced packages
Materials in packages

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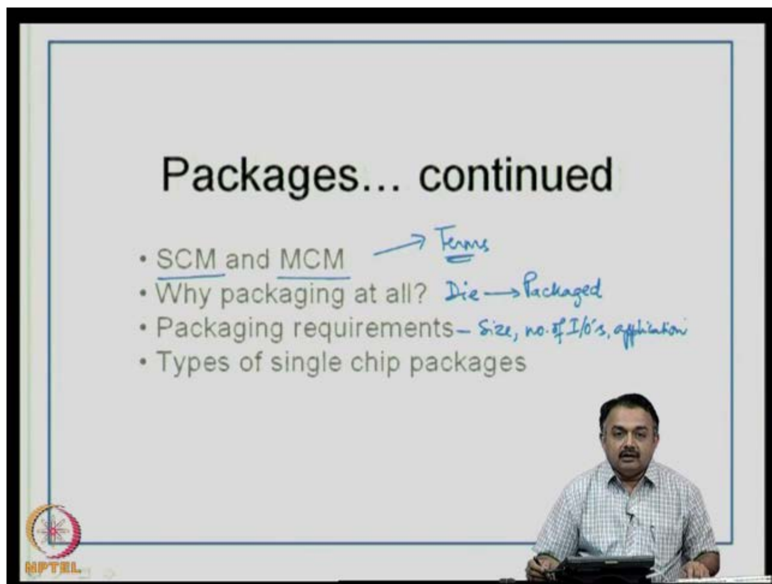

Welcome back to this module on packages. As you would recollect we are looking at various packages, the format, size with relation to application; and what package evolution has been over the years, starting from DIP packages to the chip size or chip scale packages of today. So, if you look at the, a quick review that we can have before we proceed, we have seen in the last class all about the definitions concerning single chip modules and multi chip modules.

So, SCM stands for single chip module or single chip package or single chip packaging, multi chip module MCM or MCP multi chip packaging. So, you must be aware of these various terms or acronyms that are being used today in the packaging world. We have also seen briefly, why packaging at all; which means that we get a die, and the die is packaged. We have seen some reasons as to why a die should be packaged, what happens if a die is not packaged, in terms of electrical or thermal and environmental issues. So, we have given valid reasons for packaging a die, so that it can be handled, it can be tested and finally, the die can be reliable during its application.

The third point that we have seen in the last class was, what are the packaging requirements? One of the important thing is, one has to look at the size of the die, the number of IOS, the size, the number of I/O's that is input, output pins that is there according to the design of the die; and then finally, again the application. So, accordingly you can have different materials that can be used to package a die. So, it can be a plastic package, it can be a ceramic package and therefore, the cost and economic factors also play a part, when you do the packaging of these tested known good dies. And we have also seen briefly the types of single chip packages. So, we will continue with this same momentum, and we will try to see a various acronyms, various terms, various packages that are now available for you to be used according to the application requirement.

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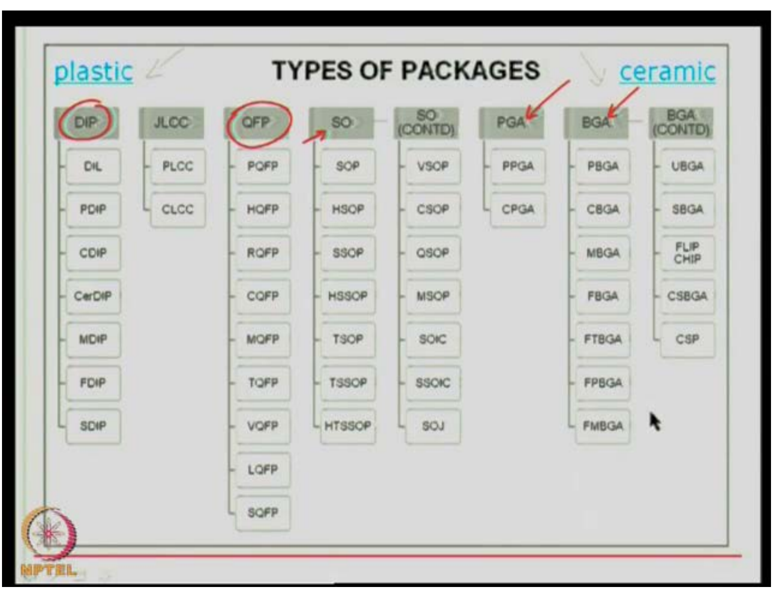

This particular slide is very exhaustive in the sense that it lists the complete set of packages in different formats in different classifications. So, at the top I have written that basically packages can be made out of plastic or it can be ceramic. The first classification is known as Dual In Line Package that is DIP or DIP package, we have seen that format of the packages in the previous classes; then comes to JLCC - J-Band Leaded Chip Carriers; Quad Flat Pack that means, when you say Quad Flat Pack, the package consists of a quad row of pins arranged mostly symmetrically, so that it occupies the entire periphery of the package.

Then we have small outline package; then we have if you recollect the graph that indicated the growth of packages over the period of time during the last 40 years; Pin Grid Array was one of the major (( )) for packages especially, in terms of the microprocessor industry; it was Intel, AMD and other semi conductor companies, which manufactured microprocessors for desktop and computing applications quickly changed over to pin grid arrays, because it afforded large number of I/O's, and very reliable pin connections to the mother board. From the pin grid array, we now have the ball grid array, where the pins are replaced by (( )).

So, we will now look at, if we look at the ball grid array here, we can see the number of packages that are available under the general heading of ball grid arrays. So, you have PBGA, which means, it is a Plastic Ball Grid Array; CBGA means, it is a Ceramic Ball Grid Array; MBGA is a Metal Ball Grid Array. Then we have like that various classifications, including flip chip; if it is flip chip or a C 4 connection chip it is used in a BGA, then the package is known as flip chip ball grid array. If it is a CSP, which again comes in a BGA format, then it can be called as CSBGA Chip Size or Chip Scale BGA.

So we will, for the next few minutes, we will see the entire set of acronyms, and see what these terms meant; what kind of superior qualities in each of these categories that we are having witnessing. So, similarly in small outline packages, you can see SOP means Small Outline Package; SSOP mean Shrink Small Outline Package, Thin Small Outline Package and Very Small Outline Package. So, all these terminologies, which can be sometimes, trademark of companies, but in practice they have become very common names of usage for marketing.

So, they have a lot of difference in terms of the length of the lead or the type of the lead or the material used in the lead and so on, including the profile thickness; when I say profile, the height of the package. So, accordingly these classifications have been made. So, in the simple DIP package for example, again you can see you have Plastic Dual In Line Package, Ceramic Dual In Line Package, the same thing has been termed in some circles as CerDIP, which means Ceramic Dip Package and so on. So, SDIP means Shrink Dual In Line Package and so on. So, this particular slide will give you a complete list of the various packages that you can choose from. So, we can now try to go into each of these classifications, and see what they mean. What I have tried to give alongside each of

these lists of packages is along some picture of these packages, so that you get an idea of how they look like; and compared to the current packages, how these can be compared.

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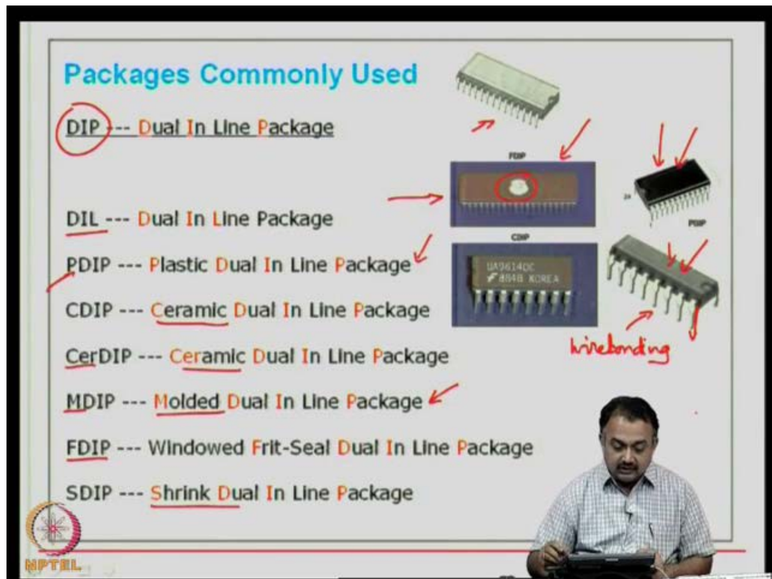

So, we will take the most preliminary or most early package called Dual In Line Package, you can see that DIL means Dual In Line, the same term DIP also means Dual In Line Package. So, when you add a P here, it becomes a Plastic Dual In Line Package, what does a plastic dual in line package mean? For example, all these you see here, which have a plastic casing or a plastic moulding, which basically is an epoxy material, I told you before, which uses in epoxy resin; and the volume of epoxy material to be used in each of these cases are well defined, because you cannot simply add more package volume.

So, the thickness is specified, the material is specified, and then these are well cleared at certain temperatures; so that it protects the inner bonds, typically a wire bond that is used in these packages. So, CDIP means Ceramic Dual In Line Package, CerDIP also indicates ceramic package, then MDIP means Molded. So, basically these are all molded packages. So, Molded Dual In Line Package and the Plastic Dual In Line Package would almost mean the same; only the terms are different. A Plastic Dual In Line Package will also have an epoxy mold. So, it depends on the marketing terms or they understanding that various companies make use it. So, we should come across these terminologies, you

must be able to understand the cross section, and the materials that are used in these packages.

As you can see that these packages have a very long lead length, so it basically is built on a lead frame, and we have also looked at what is a lead frame material. And then from the lead frame, if you rip open this package inside you will see a die has been wire bonded. So, typically you can expect a wire bonding to be done from the inner die to the lead frames right. So, FDIP means windowed Frit Seal Dual In Line Package. So, here you can see an FDIP package for example, in this picture. So, you can see at the centre, there is a glass window, and which is made out of frit glass, a toughened glass, and it is transparent, typically these are used for E prompt devices, where would you like to expose, if you want to erase a program, you can subject this package to UV light, and then the program can be erased.

So, typically for E prompts, FDIP packages with a frit seal or a glass window is typically used. Shrink Dual In Line Package or SDIP would mean that the package is typically going to have a shorter lead length and the total thickness of the package is considerably reduced. So, that depends on the wire bond length, the loop length in the wire bond and then the length of the lead frame and so on. So, this is their first major classification that you are looking at.

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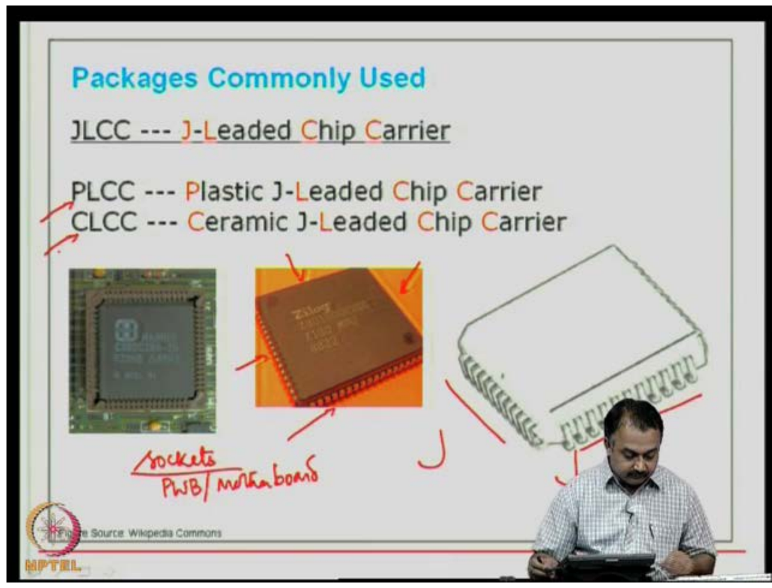

Then comes the next section, which I mentioned earlier known as J- Leaded Chip Carriers, so as you can see in this picture, these are quad, because you can see the connections are the IOS are of the four sides of the package. And typically, you can see that the leads are in the form of a J-band. So, as you can see the entire row of lead shear or J-band inside, so which means the body outline of these packages are considerably smaller compared to your Quad Flat Packs. So, this picture shows here a Plastic J-Leaded Chip Carrier, and these chip carriers can be accommodated in sockets. So, when we use these, you will have sockets that are mounted on your printed wiring board or your mother board, and these can fit into the sockets, and the advantage of using sockets is that you can remove these packages that will for repair and rework. So in this, you have two classifications; one is a Plastic and the other is a Ceramic J-Leaded Chip Carrier.

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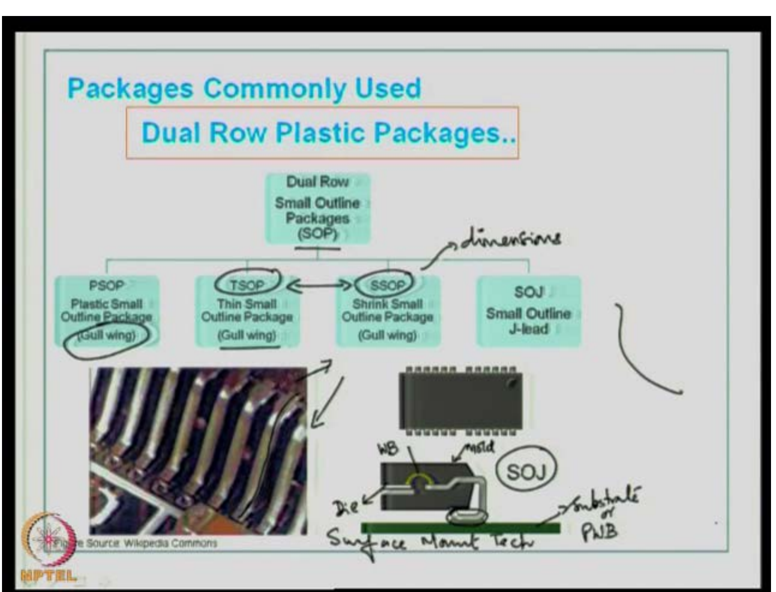

The next set of packages that we would be interested is the Small Outline Packages known as SOP. In this, you have different classifications again; one is the PSOP - Plastic Small Outline Package, then you have a thin small outline package, then we have SSOP Shrink Small Outline Package, and SOJ Small Outline J-Leaded. So, all of them are not the same; as the term indicates, and as the expansion of these terms indicate, there are differences in the construction, differences in the material and differences in the lead length, and the type of the lead attachment that you are expected to give with the printed wiring board.

So, first is the PSOP, and you have can look at the word here called the Gull wing. And this picture will indicate what a gull wing lead will look like. So, if you can look, so this is the body of the package outline, and you can see that the leads are coming out in the form of a gull wing. So, you can see that there is a large gap between the edge of the lead frame I/O point and the plastic body. So, this obviously, will occupy a lot of space on the board, but these packages are available with low pictures today, so that you can improve upon the density of the package. So, this is the typical example of a plastic small outline package. The difference between a DIP package and the small outline package is that the thickness is considerably reduced, which means that the package material is reduced which obviously, in terms of electrical performance is much superior.

Then we have the next classification: Thin Small Outline Package, so which again indicates that the package is very thin. It is in the form of a small outline package. So, compared to a PSOP, a PSOP will have a low profile. And this is again gull wing. Then you have a Shrink Small Outline Package. So, you have to really look at the data sheet in order to exactly look at, what is the basic differences between a Thin Small Outline Package and a Shrink Small Outline Package in terms of the dimensions or the thickness specific to the manufacturer? So that these terms are correct, they are accepted by the industry and therefore, different companies will bring out packages either in a PSOP, TSOP or SSOP, but the industry guidelines will rule the classification of these under PSOP or SSOP.

Then we have this small outline J-lead. So, you can see this picture here, this is the Small Outline J-Leaded device, this is the package body, and you can see here, this is the wire bond, and you can see the die here that is inside the package epoxy mold. And then the lead frame is actually J-band towards the inside after package. So, the landing point of the device is this area, and this this is typically your substrate or printed wiring board. So, the assembly of this device will come under the classification of surface mount, if you can recollect the difference between surface mount and through hole packages. So, these packages come under the classification of surface mount devices. So, the technology for assembling these compared to a DIP packages, your DIP packages will require a through hole to be inserted into the printed wiring board.

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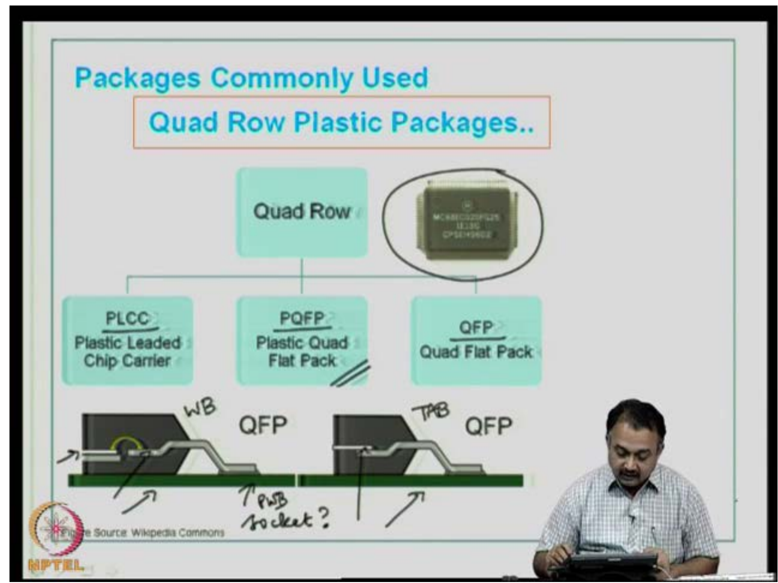

So, this is a major difference in terms of assembly. Now now we look at the next classification, which is known as Quad Packages or Quad Row Packages or Quad Row Flat Packs. So under this, you have again different categories; one is known as a Plastic Leaded Chip Carrier, the other is Plastic Quad Flat Pack, which is very common today PQFPs, and then you have simply a QFP. Now here you can also have a ceramic material that can be used, but the most economic material or package in QFPs is a Plastic Quad Flat Pack.

Now you can see here, this is the typical cross section that you can think of in a QFP, and this is the picture of a typical QFP. If you can focus on these samples here, we have seen number of times that this is a QFP, this is the top, and this is the bottom side of the QFP, and you can see that the I/O's are arranged in a quad fashion around the peripheral of DIP package body outline. So if you look at the inside of a QFP as expected, you will have the die at the centre; then you will have a wire bond, which connects the bond pad of the die side, and then to the lead frame. And then this is the shape of the lead frame. And this is the printed wiring board side. Now this can have a socket or may not have a socket that depends on the density of the board and your requirement.

So this one here typically, is another mode of QFP assembly. So, if this is wire bonding can obviously, you can expect that this is a TAB based QFP. As you can see, there are no wires here, and typically this is the site of lead bonding. So, you can have different

combinations of first level interconnect, and then the package type. So, in this case, we are looking at a wire bonded QFP or a TAB based QFP.

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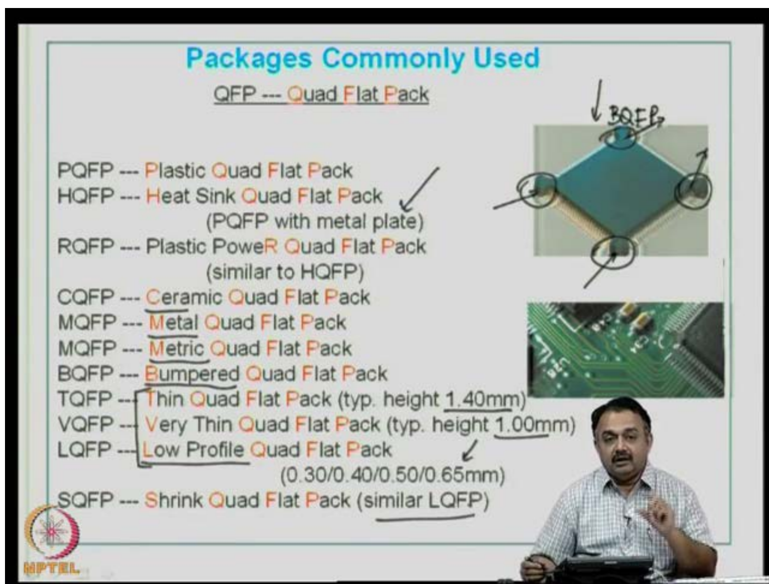

Now, under the QFP, there are various names, various packages that are available in the market today. PQFP is a Plastic Quad Flat Pack, HQFP means Heat Sink Based Quad Flat Pack that means, it is basically a PQFP, but it is got a metal plate, which acts as a heat sink, and this is typically used to remove the heat quickly from the surface of the die. So, if there are QFPs that are designed, and which can produce heat during the power up, during the working of the device of the system; then based on your design, you have to embed a heat sink. Now typically a heat sink material can be aluminium or a simply a other materials that that have very high thermal conductivity, and which should be very thin, low weight, because we do not want package packages to be very heavy.

And you have to look at compatibility of the plastic package along with the metal material to provide a reliable package or a device. Then you have RQFP, which in industry terms is known as Plastic Power Quad Flat Pack, which is similar to HQFP in the sense that it is used for power applications and therefore, is expected to have a good heat sink. Then you have Ceramic Quad Flat Pack, Metal Quad Flat Pack, metric based on some standards metrics standard. Then you have Bumpered QFP. So here you see this is the picture of a BQFP, as you can see that the corners have bumps or it is bumpered; compared to other packages, which do not have this type of a plastic material protruding

outside from the package outline. So, these are meant for different and specific purpose during assembly especially, during a process called wave soldering for example, which most of you are not aware at this stage that is a particular method of attachment or attachment soldering material to the device on a printed wiring board.

There can be chances of the two adjacent pins of the corners getting shorted due to the wave drag that happens in the wave soldering process. So, you introduce a plastic material, which will not drag the soldering material and therefore, crossing a bridge between two adjacent pins; and this will help in providing a high assembly yield. So, you can avoid bridging, and the contacts at the edges be the much perfect compared to a QFP, which does not have a bumpered edge.

Then you have a Thin Quad Flat Pack, in this case the dimensions typically the height is 1.4 mm; very thin means 1 mm height, Very Thin Quad Flat Pack; and then you have a low profile. So, all these are specific to the height requirements that an industry can produce these packages. So, typically you can see low profile can be 0.65 to 0.4 and 0.3. And then you have Shrink Quad Flat Pack, which is similar to low profile QFPs. So, this were the terms typically 3 or 4 of them in this particular list could mean the same, but if you see packages coming with each of these, you must be able to gauge or guess, what it really means in terms of material and the profile.

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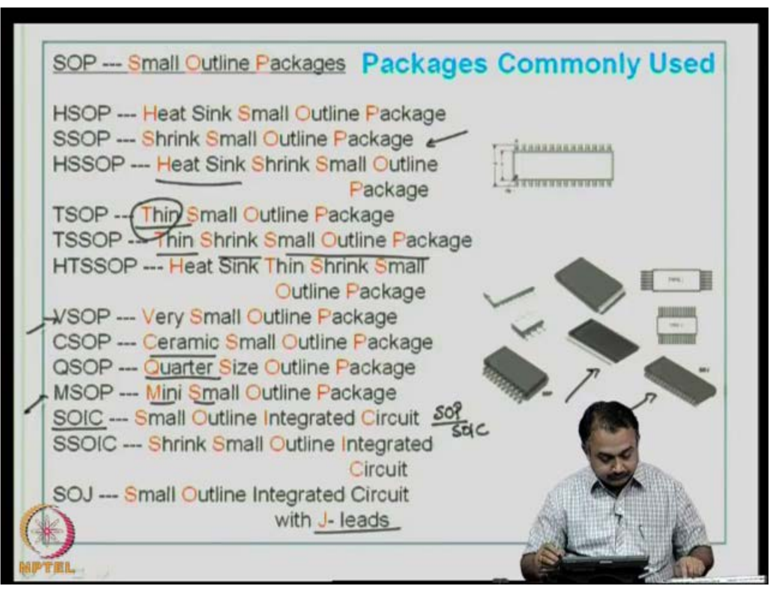

Then you have this Small Outline Packages. As you can see these pictures compared to your DIP packages or QFP, these are very, very thin. These are mostly plastic packages, and then these can be Dual In Line mostly, but with very thin lead frame structures. So, HSOP would mean Heat Shrink Small Outline Package, SSOP Shrink Small Outline Package again indicating the thickness, then you have HSSOP Heat Sink Shrink Small Outline Package Thin Small Outline Package. So, we need to look at the data sheet from the company to really understand how thin it is; what type of heat shrink materials being used, and then you say thin and shrink and small outline. So, definitely this must be high density package.

Then you have HTSSOP, which includes all of the characteristics that we have seen here, Heat Shrink Based Thin Shrink Small Outline Package, Very Small Outline Package; then you have ceramic packages in SOPs; quarter size, which is a very old package terminology; quarter is basically the coin, US quarter dollar, so Quarter Size Outline Package, Mini Small Outline Package. So in fact, VSOP and MSOP may mean the same, but they can come with different terminologies from different manufacturers. Small Outline Integrated Circuit; and SOP and SOIC would mean the same. Then you have SSOIC and SOJ with J-leads.

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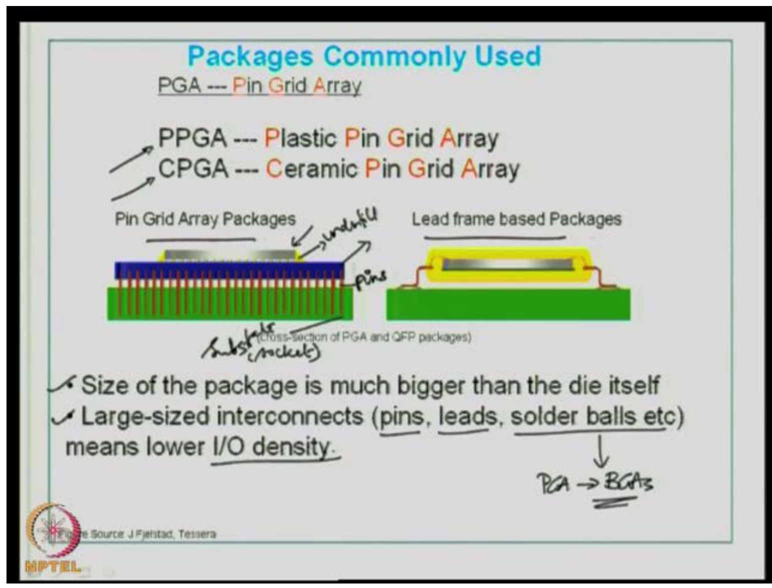

Then comes to Pin Grid Array Packages, which provide a packages with very large pin prompt and a very large die size. And usually these were very heavy as you can see from

this picture having, I have shown this Intel processor, this is basically a very large, very heavy, this contains a metal heat shrink on top; and there is ceramic package; and on the other side, you will see a metrics of gold plated pins, which are fairly long enough that can go into a PGA socket typically, of a mother board for a desktop, now computer that was used earlier. Today we do not really get PGAs for micro processors in the desktop computing, and these are replaced by the very new technology, which we will see shortly.

So, basically we have plastic pin grid array, which means the substrate and the plastic encapsulation is very specific. So, there can be a variance of the plastic that can be used. Then you have ceramic material, ceramic pin grid array. So, this is the cross section of the pin grid array package, where you have the die. Then we have the substrate of the package, these are the pins of the pin grid array, and this is the organic substrate of the printed wiring board or the socket that can be used to mount your PGA.

So, and you can see that this can also use a under fill material. If you consider the top die as a flip chip kind of a material. And this is a cross section of a typical lead frame package. So, alongside you are able to compare here, what is the cross section of a pin grid array package, and what is the cross section of a heat frame package. So, you must be able to quickly picturize cross sections of packages, as we go along. This will help you to identify the method of construction and the advantages in each using each of these packages.

In the pin grid array, the size of the package is much bigger than the die itself. You are going to use more packaging material to take care of fan out of the I/O's, and also a thermal part removing large amount of heat from the surface of the die. And the interconnect sizes are very large. So basically, these are pins, which are large; and it could be leads also or solder balls in terms of when you consider PGA migration to BGAs. So, basically it is low dense, but again these are specific to certain applications, where we are not worried about the I/O density; we are worried about the reliability of the interconnects, and the stability or reliability of the package along self life.

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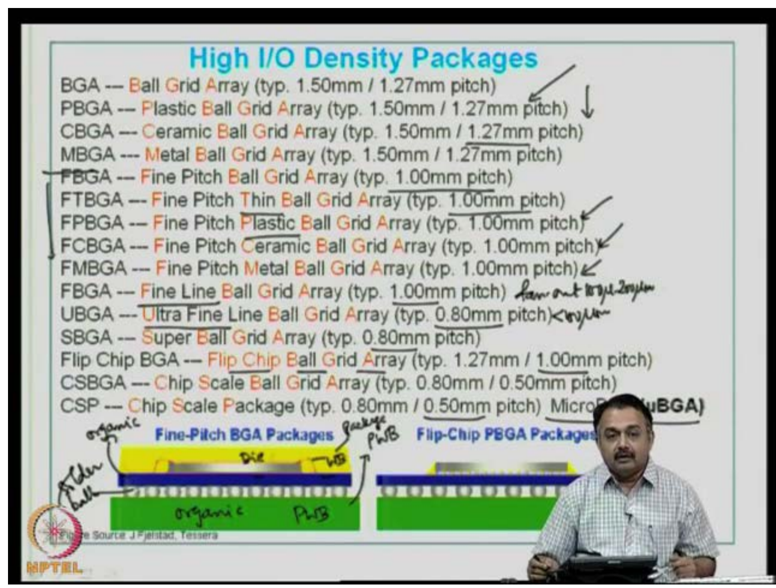

Then came the BGAs they called it as high density packages or high I/O packages, because if we compare PGA and BGA, the construction is almost similar, instead of a pin; as you can see again, if you can focus to this sample; this is a PGA, and if you look at the BGA here, the topologies almost similar, instead of pins, you have the solder balls. I also want to show you here this particular bottle, which contains solder balls. This is a typical solder spheres that are available today in the market of various dimensions starting from 0.3 mm to 1 mm; and these are used for repairing these kinds of packages during the continuous use of these if you want to repair and rework. We are not using sockets for BGAs therefore, we should be able to replace the solder spheres or the solder balls with the appropriate dimensions of these solder spheres.

Now let us look at what are the various packages available in the high density packages or advanced packages. BGA means Ball Grid Array typical pitch is about 1.5 mm to 1.27 mm to start with, then BGAs were introduced. Then we have PGA, which is called Plastic Ball Grid Array. Today a Plastic Ball Grid Arrays are available from 1.27 mm downwards. Ceramic Ball Grid Array similar dimensions; Metal Ball Grid Array, which means it uses a metal inter processor in the package construction to remove the heat.

Then you have fine pitch. So, when you say fine pitch, it is slightly different from here Plastic Ball Grid Array or the Ceramic Ball Grid Array in the sense that the pitch is reduced from 1.27 mm to 1 mm and below. Fine Pitch Thin Ball Grid Array, so again 1

mm pitch downwards fine pitch plastic. So, it is very specific here that this is the fine pitch, but it uses the plastic and here it uses a fine pitch, and the ceramic ball grid array. Then we have a fine pitch metal ball grid array. So, from here these classifications talk about fine pitch.

Then we have fine line ball grid array. So, what do you mean by fine line? So, basically if you look at this picture; here this is again a cross section of a Fine Pitch Ball Grid Array Package. Here you have the printed wiring board, then what you see here is a solder ball, which provides the interconnect to the printed wiring board, this is an organic substrate. Then you have the die here, this is the package mold, then you can see here this is a typical wire bond let us say, and then you have in between the die and this blue area that you see here un adhesive, which attaches the die. And this is basically again an organic substrate.

This organic substrate is typically about 4 to 8 layers of construction. So, what basically does? As I mentioned before, the I/O's of the die are fanned out through this entire 4 layer or 6 layer or 8 layer substrate to terminate in a solder ball. So, in this particular construction, the fine lines are used; the conductor lines that are used to fan out. These lines are very small. Typically it can use about 100 micron to 200 micron of conductor rises to fan out the I/O's from the die to the Ball Grid Arrays. So, that is why it is classified as a Fine Line Ball Grid Array. Then you have Ultra Fine Line; pitch is again reduced; in this case, the line width can still be reduced to less than 100 micron, if the construction is possible.

Then you have a Super Ball Grid Array; again typically the pitch is 0.8 mm length; it depends on what the company calls as super, but we have seen that Super Ball Grid Array would really attack the thermal problem, thermal management of the die much effectively compared to large pitch devices. Then this is a very common terminology that is FCBGA Flip Chip Ball Grid Array; and pitches are 1 mm downwards, then you have CSBGA, which is Chip Size Package Construction, Chip Size Ball Grid Array; and Chip Scale Package CSP, this is also known as micro BGA. In fact, micro BGA is a terminology introduced by the company Thesara. Thesara is a well known manufacturer of a CSPs and BGAs globally. And you can see Chip Size Package has a pitch of 0.5 mm and below. So, for a package to be classified as a CSP, the pitch was to be 0.5 mm, and we will see later, what exactly was CSP means in terms of package area to die area.

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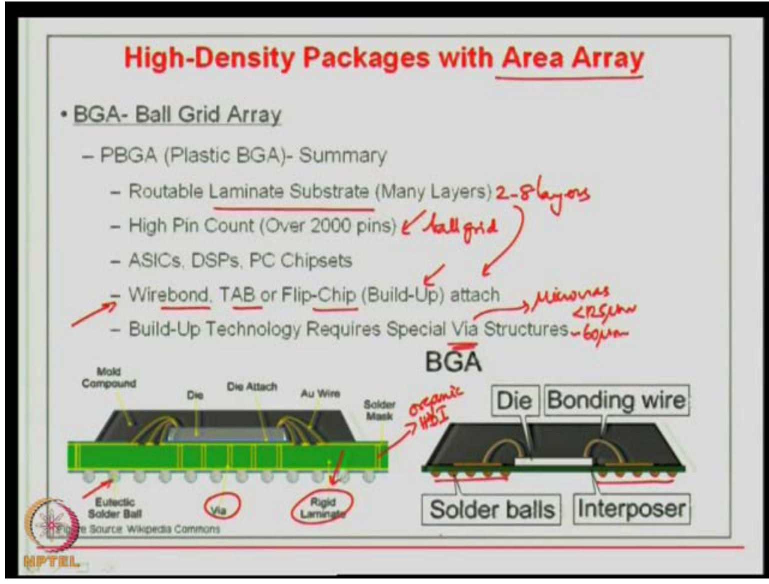

So, these are High-Density Packages with Area Array. So, we have seen compact of DIP package, BGA is a area array package, a CSP is also a area array package. So, the summary is that plastic BGAs are available; you require a laminate substrate to do the routing. It can be between 2 to 8 layers typically not more than that. Then it has got high pin count. Today is SPGAs can have pin count over 1700 pins, such will balls solder balls. So, here typically it is a ball grid.

So, assembling such a high pin count device on to our organic substrate is going to be a major challenge. But as I said earlier because of the controlled collapse in self alignment basically due to the surface tension provided by the solder balls, you actually get very high yield or throughput per process. The areas of applications for BGAs are typically then you look at CSPs and DSPs that is Digital Signal Processors, chip sets of PC's and the inside construction could be a Wirebond Tab or a Flip Chip. And when you use a flip chip you have to use a build up technology by having a high density interconnect substrate. And the Build-Up technology requires special via structures; the via have to be micro via's and typically, less than 125 micron in dia. Today people are manufacturing micro via's for BGA's of the order of 16 microns.

So, you can imagine the amount of real estate saving, the amount of density that is introduced, high density that is introduced in the design and the construction. So, if you look at the cross section of a BGA, you can imagine that there is a die, there is a

wirebond, and then the termination is with the BGA solder ball. And this is another picture of a cross section of a BGA, where the focus here is see here is the organic substrate, which is high density interconnect structure. So, you can see there are via's, and this is the solder ball, and this is the rigid laminate structure, organic structure.

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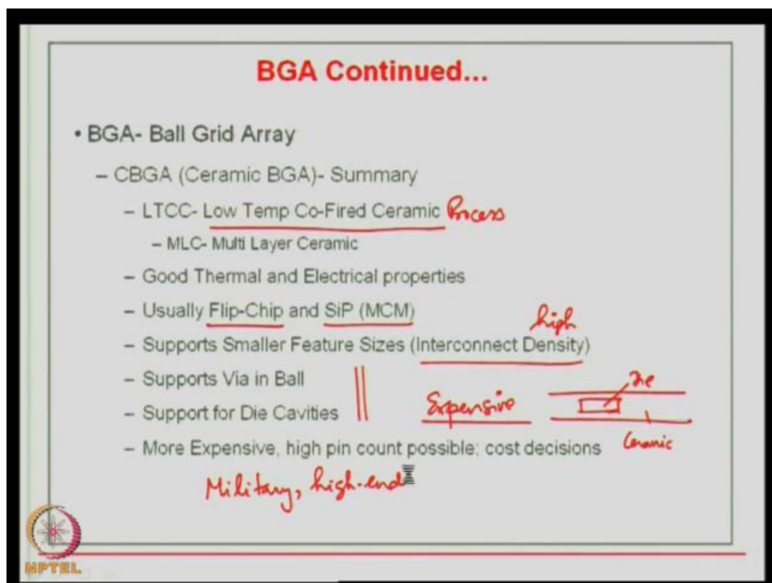

You can also have ceramic BGAs; you can also have multi layer ceramic, that can house these BGA's. The reason for using ceramic ball grid arrays is that the applications compared to a plastic ball grid array are different, which means the, you are going to look at better thermal properties, you are expecting more heat to be generated during the application of the device or the power up during the power up of the device and therefore, you require a better support in terms of removal of heat from the substrate. Therefore, you would rather going for a ceramic substrate, which has got better thermal and electrical properties, which can protect the die; and which can reduce the parasitics, because of the different dielectric constant that you have in the ceramics compared to a plastic substrates.

Then typically usually in ceramics, it can be a Flip-Chip BGA or it can be a Multi Chip Module, it supports small feature sizes that means, the interconnect density is very high. The manufacturing technologies of a CBGA and the plastic BGA are different, because you are going to use a process called Low Temperature Co-Fired Ceramic Process, we will see that in the next lecture, which is quite different from the PWB and seek and shell

build up technology that is very popular today. And again this is expensive compared to your organic substrates and your plastic BGA; the ceramic BGA's are expensive. It it supports other feature like via in ball and our die cavities that means, if you take a ceramic substrate, it is possible that you can embed your die in one of the lowers after ceramic substrate, and then build your interconnects around it, but these are going to be very expensive.

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So, typically if you look at the application areas, this will be use for military and other high end applications, where cost is not a factor, but where the formats becomes a major concentration and choice. There is also another classification called Tape Ball Grid Array or if you know about tape automated bonding. Here the, these are basically a chip size package, very low profile; that means, thickness is very small; smaller pin count and low density cavity down.

So, basically you can expect the features to be available on the tape, and then you have the bonding taking place between the die; the Ball Grid Array typically comes in a tape format, and then typically a Tape Ball Grid Array is not very common nowadays; most people use Plastic Ball Grid Arrays, and for high end applications, we use a Ceramic Ball Grid Array. So, the interconnects can come in a 1 or a 2 layer tape, and it is easy to build the grid, ball grid around this, including the interconnection to the die.

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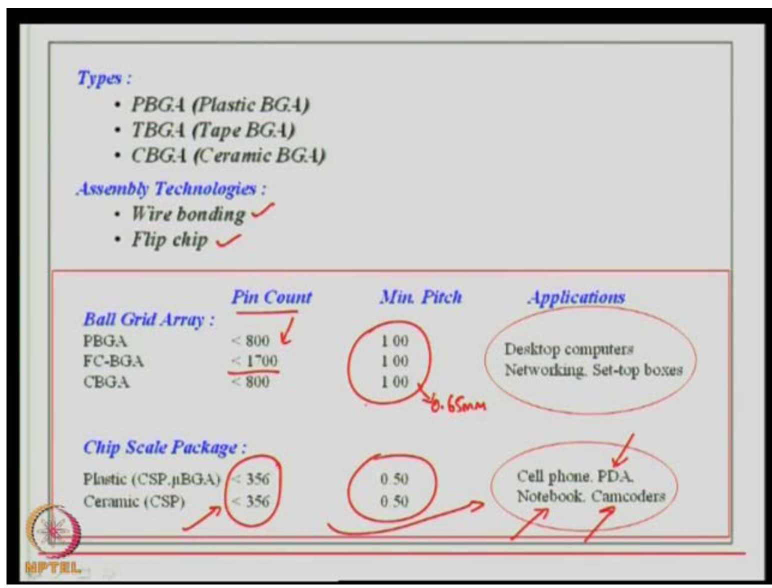

So, as a summary, we will see that there are 3 types; Plastic Ball Grid Array, Tape Ball Grid Array and Ceramic Ball Grid Array. Technologies can be wire bonding or flip chip. And then these at a glance will give you the application areas for example, BGA's you can see in desktop computers, networking set top boxes and so on typically for communication device. Then you look at CSP - Chip Size Package, these are used for hand help products like a cell phone, personal digital assistance, these are all hand held devices; notebook computers, camcoders and so on.

So, what are the pictures that you can expect in a CSP? As I said earlier, it has to be 0.5 and less. And then in Ball Grid Array typically starts with 1 mm and it today you have seen Ball Grid Arrays go down up to 0.65 or 0.5; if it is 0.5, then it is a CSP typically, up to 0.65 mm technologies are available and therefore, you should look at this CSP, you do not expect a very high pin count, very mid range pin counts so around 350 or so, because the die size is very small, the package wiring is also very small. And these are meant for typically handled applications, where the size of the product itself is small. Then you have a Plastic Ball Grid Arrays, you can expect larger pin counts here. Flip chip BGA will provide a very large I/O density, ceramics mid around 800.

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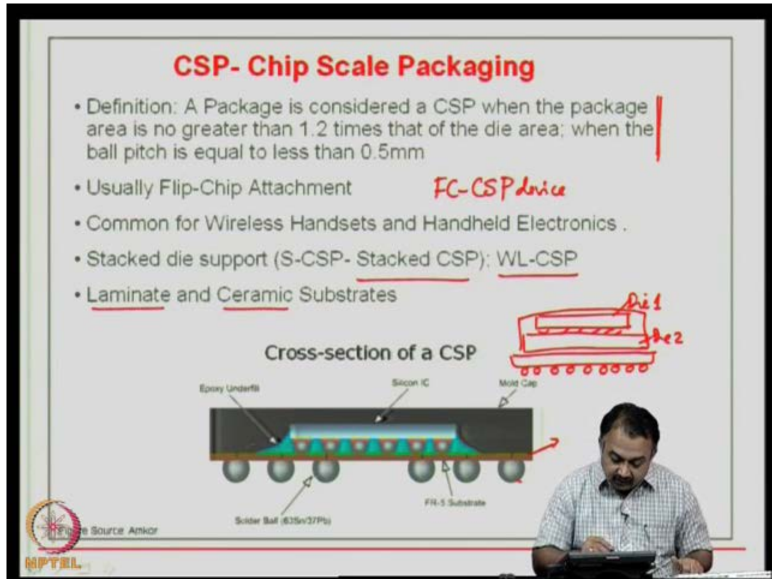

So, what is a CSP compared to a BGA? The first thing that we have seen is the pitch equal to 0.5 mm or less than 0.5 mm for it to be classified. If you look at the definition, the package is considered as CSP, when the package area is no greater than 1.2 times that of the die area. So, this is the very important thing to be considered or classifying a BGA as a CSP. The package area is just about 20 percent that of the die area. Then if this is not met, and including the ball pitch equal to or less than 0.5 mm, then you can considered it as a CSP.

You know, CSP normally, it is a flip chip attachment. So, you can call it as a flip chip CSP device, because only this kind of a construction will give you a very high pin count. It is very common for handle the applications wireless handsets and so on. It is possible to have a stacked die support; therefore, you can call it as a stacked CSP. And if the CSP is manufactured at the wafer level; you now know, what is a conventional packaging and wafer level packaging, I have explained it before; therefore, you can have a wafer level package also. You can have a laminate substrate as well as a ceramic substrate. So, typically, what do you mean by stacked CSP? Typically you can have die 1. So, this die 1 can sit or can be attached to another die - die 2; and finally, this can have a package built around it, and this sits on a substrate, organic substrate with the Ball Grid Array. So, the entire unit or a system should have package area not greater than 20 percent of the die area.

So, you can imagine you can have 3-D stacking, multiple die stacking; and at the same time it will give you large number of values; these are custom built. So here, this picture here will give you an idea of what is CSP S? Almost similar to a BGA, where you have the die, die bonding done, and then these are the bumps of the flip chip, getting attached to the substrate here, then these are the solder balls, and then you have the epoxy under fill this green area that you see here, and this black area is the top epoxy mold, which protects the device. So, typically this package area should be much less compared to a BGA.

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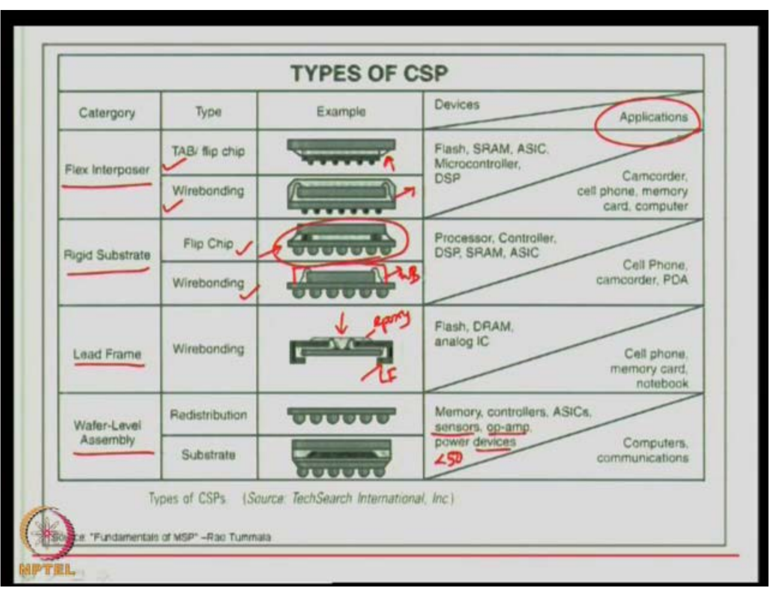

So, the types of CSP based on the applications and based on the materials, and the type of construction, you can have different types of CSP. The first thing is a tab or a flip chip CSP, where you gives a flex interposer between the die and the I/O's or the bumps that is basically for providing better reliability during the operation of the die in terms of heat, the die and the substrate together can undergo changes during thermal cycling or expansion and contraction of the entire set of materials, the silicon die, the organic substrate.

So, in avoid to in order to avoid die crack, and war page of the substrate, you rather use a flex interposer. So, in this you can have two types; TAB/ flip chip and wire bonding, and these are the application areas, and you can see the construction here, this is typically a TAB material, the TAB type of construction, and this is a wire bonding construction, and

these are packaged protected with a epoxy mold. And you can see that in some cases, you can have the cavity down, and in some cases it is face up, face down configurations are possible. Then you can use a rigid substrate, if you use a rigid substrate, you can have a flip chip or a wire bonding options, typically used for DSP's, SRAM, ASICS and so on.

I think by now you are very familiar with these kind of a cross section, where you have the die, the bump, the solder ball, the under fill and so on, very popular type of construction. Here it is a wire bond. So the, because the size is small, the wire bond, number of wire bonds will actually, be very small, the I/O's are expected to be around 200 to 300, it can be even less. And the packages also done on this type of a construction. You can also have a lead frame based CSP, where you do wire bonding as you can see here in this picture, there is a wire bonding, and there is a lead frame here, and then the wire bonds are protected with the epoxy material or the mold; these are used for analog ICs, DRAMs and so on.

Then you have wafer level assembly, where you do the redistribution of the signal layers of the wafer level at the organic substrate, and these are very small in size, these require expensive bumping process to be done at the wafer level, and the number of players in these particular activity are very low currently, and the application areas for very small devices with very, very small number of I/O's, sometimes the number of I O's can be less than 50. Therefore, the typical application areas can be sensor, operation amplifiers, power devices, memory devices, micro controllers and so on. And you can see the various application areas for CSP.

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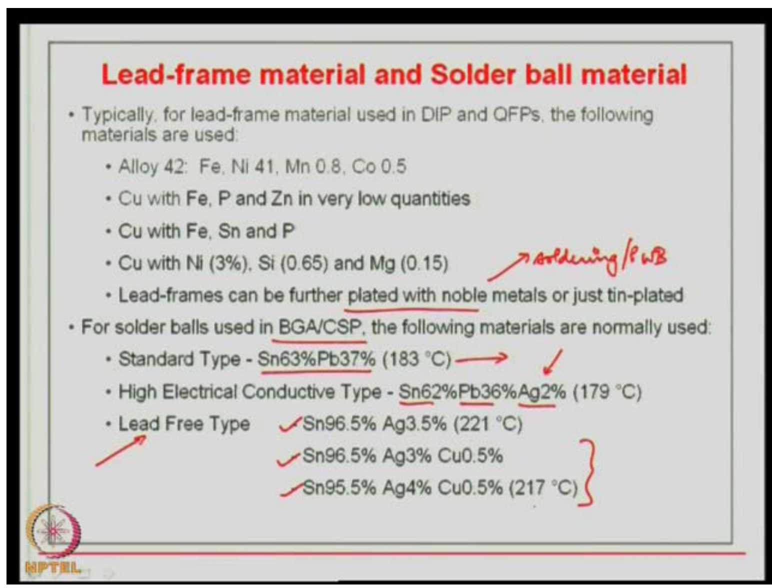

Now, what is the lead frame material? So, we have actually covered the entire section of packages from a d DIP or Dip Package to a CSP. Now what is the Lead Frame Material or the Solder Ball Material that is being used? Typically for lead frame material used in DIP and QFP packages, the following materials are used. The most common is alloy 42, which contains apart from iron, nickel 41 percent, manganese and cobalt in very small percentages, copper leads with iron, phosphorous and zinc in very low quantities, copper with iron tin phosphorous in very low quantities, copper with nickel silicon and magnesium; and these alloys can be further plated with tin or other noble metals like coal or palladium and so on or platinum and so on to provide better connectivity contact, so that your electrical performance for these package to devices are better.

And these plated materials should accept the solder, so because the next step is soldering these devices on to your printed wiring board. So, that part has to be taken care. If you are using solder balls that are used in BGAs and CSPs, the following materials are normally used, the standard type so far has been tin lead with eutectic composition of 63 percent tin, and 37 percent lead, and the melting point of this particular alloy is 183, which is, which has been so far a very common standard. But with the advent of legislation or the introduction of legislation on lead usage, lead frame materials are being used.

But we have to compromise to some extent on the higher temperatures that we have going to face with higher energy utilization for assembling these devices on to the substrates therefore, a very proper choice is to be made, if you are going to work with lead free materials. So, we will talk more about lead free at much later stage, the high electrical conductive type material is tin, lead and silver; silver is introduced in improve the electrical conductivity and the melting point is around 179.

And more important lead free, many industries are switching over to lead free. So, when I talk about lead based, it is already extent in most industries. But for academic purpose, we need to know that we have been missing tin lead; when we have been missing tin lead silver material to reduce the melting point further. So, lead free can be tin silver, which melts at 221, when you have tin silver copper and tin silver copper with different percentages basically to improve the metallurgical bond, and to improve the properties of the solder attachment.

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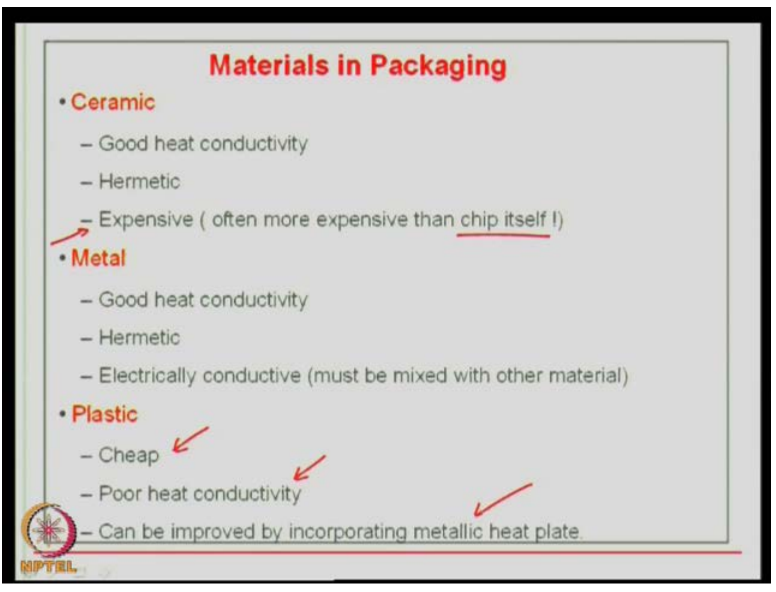

So therefore, you can see now that materials in packaging are very important. The choice of a plastic package or a ceramic package is again based on what you are expecting in terms of application; therefore, all applications need not have a ceramic choice, and all applications need not be plastic. So, you have to carefully look at the circuit that you are working with, if it is a power or if it is a communication circuit, if it is a analog circuit,

what kind of simulations you have done, what kind of heat requirements are there in terms of material choice.

So, ceramic if you are using, it should have good thermal conductivity, it should be possible to hermatically seal the packages with ceramic; it is expensive compared to plastic packages. It is often more expensive than a chip itself therefore, you must be wondering, why do we need a ceramic package, but I so said in certain areas like military and space and other avionics and so on; the reliability is more important, because of high performance therefore, people going for ceramic. Metal packages, good heat conductivity, hermetic sealing, electrical conductivity. So, therefore, it must be mixed with other material.

Plastic, it it is very cheap poor thermal conductivity, but you can add fillers and improve the conductivity, thermal conductivity; and you can also have metallic heat plates to improve the thermal conductivity, because your applications, where you have to work in millions of systems, and cost is a factor, you will have to going for plastic packages. So today, we have seen all the packages; and we have looked at various cross sections of packages; and we also looked at the progress from DIP to CSP, and the requirements in terms of pitch materials and so on. We will continue this chapter in the next class.

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