An Introduction to Electronics Systems Packaging

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Module No. # 03

Lecture No. # 11

Why packaging? & Single chip packages or modules (SCM)

We will begin this module with the review of the topics that we have done so far. Today, we are going to talk about a new topic, which is called packages in general. We will look at various formats of packages and try to understand what benefits you get by using different formats of packages, what applications you can use for each of these. So, the selection of packages in your future design and applications requires you to understand the various cross-sections of packages and inside of packages. So that you can utilize to the maximum benefit of the electrical characteristics that are embedded in this packages.

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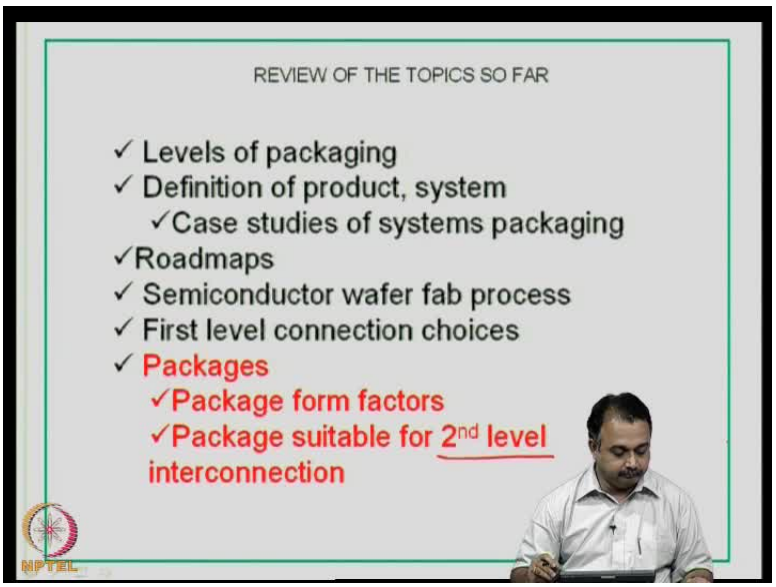

So, we will begin with the review. The topics that we have done so far are; what we have seen? Levels of packaging: We have seen first, second and third level of packaging and understood the critical areas in each of these levels of packaging. Secondly, we saw, what is the definition of a product and a system. We have defined what packaging is and we have seen at least four different case studies of systems packaging. We have looked at roadmaps; initially, we looked at the semiconductor roadmap. We also had a brief glimpse about the packaging and assembly roadmap. I need not emphasize that roadmaps are very critical in understanding the growth of the packaging industry. I hope, by now you are aware of the usefulness of various roadmaps.

I have to remind you that even industries have roadmaps. Even industries that manufacture packages have certain roadmaps and they work according to those timelines. Then we saw, what semiconductor wafer fab is and how the process in this particular industry has grown over the decades. We also have seen flowchart of the front end and back end process. We have seen the criticality of various process steps in defining a particular technology and therefore the growth in the semiconductor industry.

We have seen the first level connection choices. What are those connection choices? Wire bond, tab and flip chip. So, we have seen exhaustively and extensively, what a wire bond means, what are the materials used in the wire bond and how the process is established. Then, we have seen tab- tape automated bonding and the areas of application for tab. The methodology of connection in tab, especially the inner lead bond and outer lead bond, you are familiar with that now. We looked at C4 and that is the flip chip process, which is currently very popular. We are going to see, how flip chip methodology of inter connection or chip connection choice is utilized in fabricating or bringing out these packages.

Today, we are going to look at packages in general. We will look at package form factors. We will look at the suitability of packages for second level interconnection. I hope, by now, you are aware of what is a second level interconnection? The second level interconnection means- your package is now connected to a printed wiring board; the printed wiring board is a system level printed wiring board because a printed wiring board by itself can perform system functions. It is highly integrated and high density board. You can pack as many components as you would like because the technology growth in this second level is enormous. We have to fully utilize those technologies. So

that the package you are using becomes an added advantage by itself; in terms of density in these second level interconnect system. So, we will now look at it.

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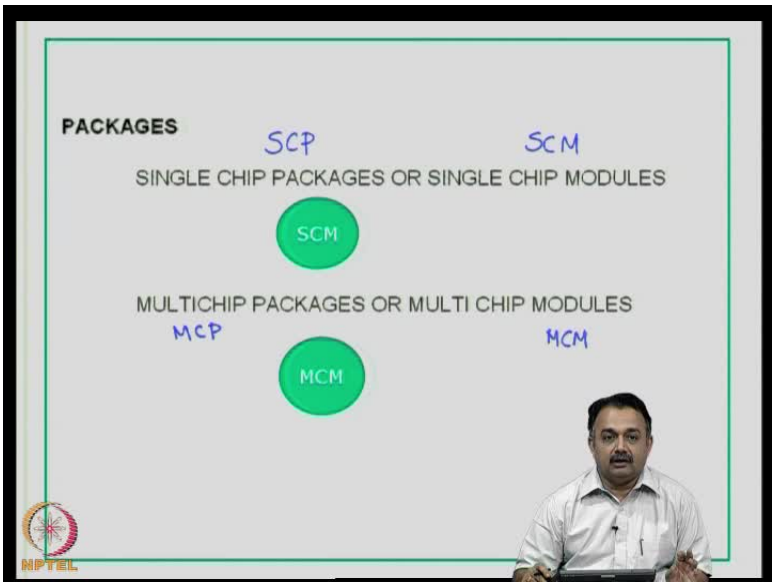

The Packages - what do you mean by packages? Broadly, we can define packages as single chip package or another term used today is single chip modules. You call it as SCM and sometimes this acronym called SCP is used. So, whenever you look at this acronym in the packaging context, you can identify the mask single chip packages or single chip modules.

Now, you have the other end and that is multichip packages or multichip modules. So, you might also hear the term called multichip packaging, which basically describes the process sequences in building a multichip package. So, the criteria performing a single chip module and a multichip module are completely different. So, what you are trying to understand through this chapter is that, as the name indicates, a single chip package will contain one chip or one die interconnected in a suitable format and then packaged. Package means, it is protected from the external environment. Other external factors like temperature, humidity, dust, electrical, thermal effects and so on. Then as a name indicates; multichip modules or multichip package- it means that that package will have two or more die interconnected on the same substrate. So, the first hand definition for single chip package and multichip module or multichip package, basically gives you an indicator that how many dies are present in the package form.

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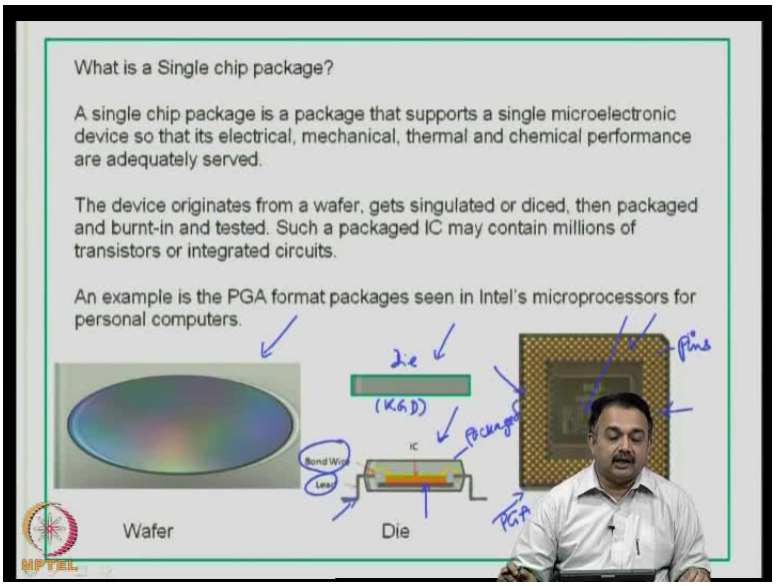

So, we will try to define further on what is a single chip package. A single chip package is a package that supports 1 micro electronic device. So, electrical, mechanical, thermal and chemical performance are adequately served. So, it is not enough if we take a base platform like a substrate. It can be an organic substrate, a ceramic substrate or some other substrate that is suited for that application. Then, you have to look at how to fan out the IO's from that single die suitably, such that the designed electrical characteristics are not diminished. It has better mechanical, thermal properties and chemical performance; in terms of its interaction of the materials with the environment is not changed and it is served adequately.

So, the device originates from a wafer. So, the starting point, as you can see in this picture is the wafer. We started with the wafer, after the wafer is totally tested and the process completed. We are now singulating the dies from the wafer. So, you get a known good die and this is the die in which you can perform the required electrical test and then call it as a known good die or KGD. It is packaged and after the packaging is done, it is burnt using several standards based on the material that you are using. It is tested and then qualified for sending it to the market So, such a packaged die or IC may contain millions of transistors or integrated circuits. So, basically, if can look at the microprocessor application, the die is singulated. Then it is packaged and then we are going to look at what format or form this particular microprocessor die is going to be available in the market. Whether, it is going to be in the form of a lead, a pin, a solder

ball. Normally, if it is microprocessors, it is going to be packaged. For other prototyping applications, this packaging sometimes may not be done. So, it can be directly mounted on to your second level systems, which is the printed wiring board. So, that is known as a bare die and the conditions for using a bare die and a package die depends on the application that you are going to work with. Normally, it prefers to have a well-packaged IC for high end applications. Now, as you can see from the wafer, the die is singulated and then it goes into the process that we talked about wire bonding, tab, flip chip. In this particular picture, (Refer Slide Time: 10:37) what you are seeing here is a wire bond and these are the lead frames. You can see the bare die at the center resting on a substrate. At this particular point, we are going to do a die bonding and that is how it is resting on that particular base of the lead frame material.

You can see, the wire bonds are the first level interconnection and it is attached to the lead frame. It is packaged or encapsulated. So, you have to choose a suitable encapsulant and mold the material to get a well-defined thickness of the plastic material. As per quality, you can check the thickness, the length of the lead frames and so on for sending it to the market. So, wafer to single die, single die to a package die. You can see here, (Refer Slide Time: 11:51) this is how a single chip package or a single chip module will look like. Here, you can see at the center; there is the encapsulant material. If you rip this particular package, you will see the bare die inside. So, here the die is protected and along the periphery, you can see the interconnections of the IO's brought out from the die. So, typically, this is a package that you would have used and this is known as a quad flat pack for example, QFP because it is a quad interconnection. The IO's are at the periphery and at the four sides of the die.

So, because of this, you are able to increase the number of IO's. It can be in the form of this particular format. This is different from the QFP and this is known as a pin grid array or PGA. So, for example, Intel microprocessors recently have been in the format of pin grid array or PGA. So, here you can see the interconnections are in the form of pins. These are the pins, which will get attached to your system level printed wiring board. So, various companies like Intel also bring out there microprocessors in a PGA format. Some of them will bring out in a ball grid array format. Some others in a QFP format and that depends on the number of IO's and the pitch. I hope, you remember what a pitch is. Pitch is going to be a very crucial decisive factor in determining and building your format for

the IC packages because you are going to make it. The industries are going to make it in millions and so they have to consider the cost of the materials, the number of IO's and the pitch to decide on what kind of package they can finally bring out for that particular design.

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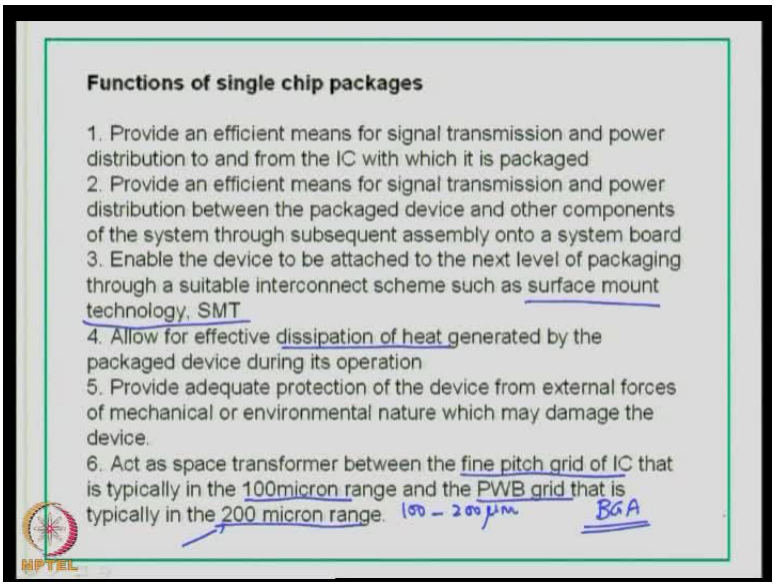

So, what are the functions of a single chip package? Firstly, it provides an efficient means for signal transmission, power distribution to and from the IC. You are going to take the IO's and then you are packaging it later. We have seen this particular statement in the definitions for packaging, if you recollect. So, whenever you look at the package, we are not really worried at the number of IO's. The IO's and the package format will finally be converted into some methodology for efficient means of signal transmission without loss in signal, which means the signal propagation delay should be very low.

You would have calculated something from your circuit design regarding the signal propagation delay, but when we use the package, it should not be lowered to the great extent. A great is the one that will contribute to some extent in the delay or loss, but we have to make sure that the tolerance levels are minimum. Power distribution is very important for the working of the IC and that dependence on the power, you have calculated for running the IC without a package. With the package, you have to basically do some testing, before these packages are send to the market. These packages will have to provide an efficient means for signal transmission and power distribution between the

package device and the other components that you are going to mount on the system level printed wiring board because an IC is not going to perform by itself. The performance is related to the other subsystems. It can mean a number of capacitors, resistors, inductors, electromechanical devices and other integrated circuits or active devices that you are mounting on that system level board. On that particular device, you are going to interconnect these various active devices and passive devices to perform a particular system function. It can be an analog function, a digital or mixed signal, high bandwidth and so on.

So, it can be a high power application circuits. So, depending on the type of application, your IC has to perform efficiently in this mixed environment. Thirdly, the packages unable the device to be attached to the next level of the packaging through a suitable interconnect scheme, such as surface mount technology, which I talked in detail. You now know, what is a through hole technology component and a surface mount technology component. Today, the surface mount technology is growing leaps and bounds. Most packages are being available in the surface mount technology format. The package should allow for efficient and effective dissipation of heat, when the package is powered up. So, when the package is powered up through the circuit that you have designed, there will be heat generated from the active device. How are you going to take care of it? Partly, the package material has to take care of it to dissipate the heat from the silicon die through the package material to the environment. That happens through the system level printed wiring board. If you are an efficient designer of the printed wiring board, you will take care of heat in different ways through the solar joint, through some kind of a heat sink or a copper plane that you have generated in the printed wiring board to remove the heat quickly. Other methods can be by using an external heat sink on top of the device to efficiently remove the heat. So, this is a very important point that you have to take care of in deciding what package you want to use.

So, I would put this as a very important point of discussion. The fifth point is - the package should provide adequate protection of the device in concern, basically, the silicon device from external forces of mechanical or environmental nature, which may damage the device. So, obviously, when you look at any package, depending upon the size, the package volume also increases. Therefore, the package volume and the package material will have to take care of temperature changes, moisture changes in the particular

area of operation of the device, then dust and finally, other electrical or other mechanical interruptions like vibration or shock and so on.

Finally, the device should act as a space transformer between the fine pitch grid of IC. Please note this point very carefully because we are talking about two levels of pitch here at the IC end. Typically, for example, it could be 100 micron pitch. At the system level printed wiring board end, it could be around 200 micron range pitch. So, we are talking about this pace transformation from 100 to two 200 microns. So, your substrate is going to handle this space transformation between the device and the board. How do you take care of this? Because you cannot handle fine pitch at the system level currently, because of the limitations in technologies and the assembly limitations. You are going to establish that in your package by having a suitable fan out and this is typical of your ball grid array, which you are going to see later. How efficiently the substrate takes care of space transformation between two types of pitches, one is a fine pitch and one is a fairly larger pitch, which you can probably handle. This is the type of pitch that you will utilize for mounting your substrates on the printed wiring board.

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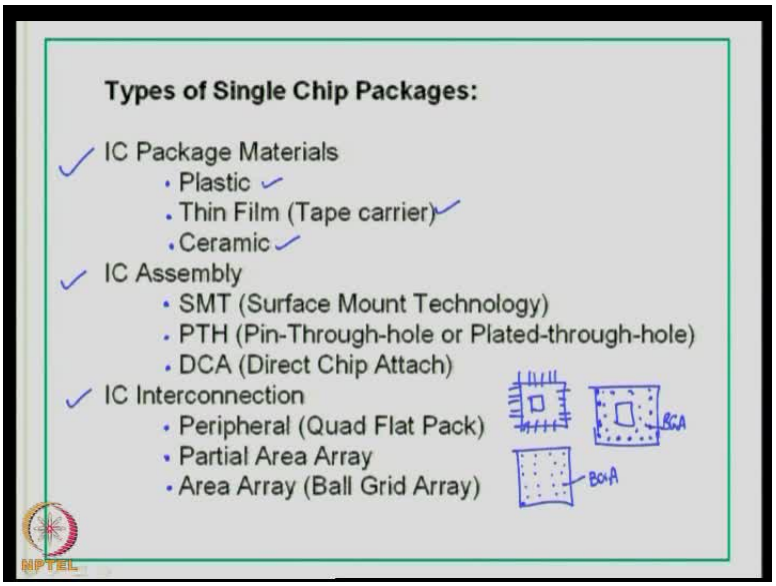

What are the types of single chip packages that are available? They can be classified based on package materials. First thing- it can be a plastic package, the second thing- it can be a thin film or a tape carrier and thirdly- it can be a ceramic material that can be used to package the material, which means in the first case, you are going to use a plastic

substrate. In this case, you are going to have the IO's in thin film note or a tape, example: polyimide and thirdly it can be a ceramic substrate that can be used for packaging your device. The other classification is based on IC assembly type. So, it can be a surface mount device. It can be through a hole device or it can be a direct chip attach.

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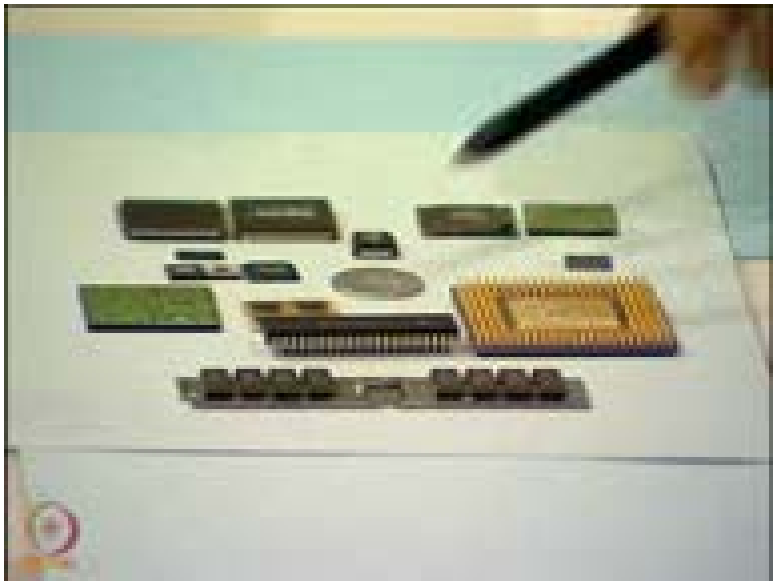

I want you to turn your attention to these particular samples that are given, where I will try to show you in this classification. For example, this is a plastic package and then this is a ceramic package. It means the substrates for each of these are different. If you look at this particular device; this is a quad flat pack and is of surface mount technology. We have this one; this is a dual in line pack, which is a plated through high technology because they have long leads, which go into the holes of the printed wiring board. If you look at direct chip attach, for example, this is a bare die, which can be considered as a flip chip and can be directly attached your printed wiring board. So, the pitch here is going to be a very small compared to the pitch here. So, the assembly techniques also define the types of single chip packages.

Finally, the classification is based on IC interconnections. It can be quad flat pack, it can be partial area array or it can be a complete area array package. So, you know what is a quad flat pack which means the die is here and the leads are taken from the four sides. There are different types in a quad flat pack. If it is a partial area array, that means the die is here and you are going to utilize partly at the back side of the die or the package by

using solder balls and this is a BGA connection. A complete area array would mean the entire area under the die is utilized for creating solder balls and this is also a BGA. So, that depends on the size of the die, the pitch and amount of heat that is dissipated. So, these are the basic types of single chip packages that you will encounter.

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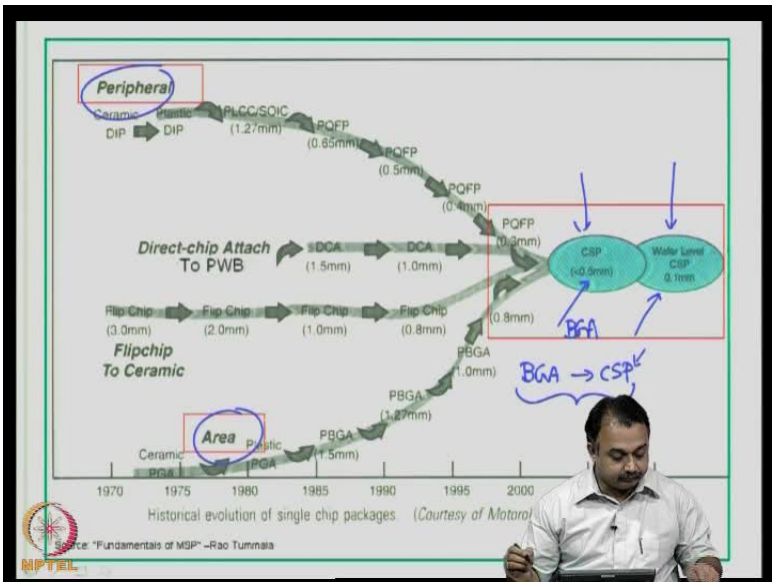

If you look at this figure, on one side you see peripheral packages and the other side you see area array packages in the peripheral packages. We have moved from DIP to plastic dip packages, then we have seen the growth of a PLCC is Plastic Leader Chip Carrier small outline intergrated circuits. This number that is written here denotes the pitch of the component, 1.27 mm is the pitch of the package and we move to a smaller pitch 0.65 mm for PQFP, which is Plastic Quad Flat Pack. We have worked with 0.55 mm plastic quad flat pack, 0.44 mm PQFP, 0.33 mm PQFP, which means we have seen that the pitch has reduced continuously over a period of time. So, we are at 2010 and in 2011, we have seen the growth. Lower pitches means growth or high density packages are being utilized or produced by the industry.

We have area array packages on the other side. Pin grid array packages are used for intel microprocessors. Other companies, which have utilized PGA's initially, were ceramic because the number of IO's was very large. It has gone in to plastic PGA, then have moved to ball grid array. PGA is similar to BGA and the only thing in BGA's is solder balls replace the pins. So, in BGA, for example, initially during 1980, we have worked

with 1.55 mm pitch ball grid arrays, then 1.27 mm became good standard plastic ball grid array and then1 mm and 0.8 mm. Today, we are working 0.65 ball grid arrays and what next? If you look at the other extremities; direct chip attached to printed wiring board. Typically, you can call it as a flip chip or a chip on board technology, which I have briefly mentioned in the earlier class. So, DCA - Direct Chip Attach with the pitch of 1.55 mm,1 mm and now what next? Flip chip to ceramic 3 mm, 2 mm, 1 mm, 0.8 mm and what next? So, all of these technologies that we have seen has very high growth rate in terms of lowering of pitch culminated in a very new technology called chip size package or chip scale package. It can also be known as wafer level CSP. Now, if you look at the pitch here, CSP is classified, if the pitch is 0.5 mm or below. Otherwise, you can call it as a plastic ball grid array or a ceramic ball grid array or a PQFP with a 0.3. We have seen that and if you look at CSP, the definition or the qualification for a BGA package to be called as a CSP. The pitch should be 0.5 mm or lower.

Today, there are new technologies called wafer level chip size packaging, which has got pitch as low as 100 microns and that is 0.1 mm. As you know, the CSP methodology and wafer level CSP methodology; it is a lightly different and I will briefly explain about conventional CSP and wafer level CSP shortly.

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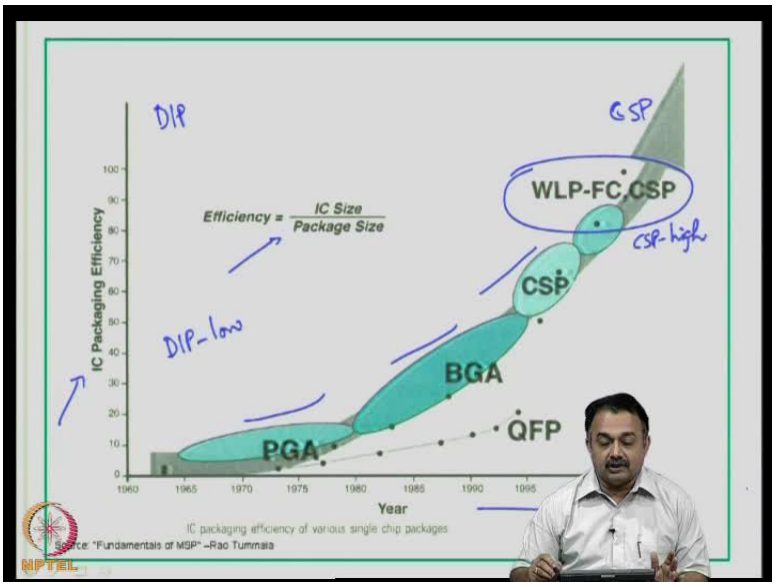

The basic difference between BGA and CSP here is that the package volume is much less in a CSP compared to a BGA. So, today, we are in the era of CSP's. If you look at

these particular slides, which talks about packaging efficiency on one side and then the timeline, this is slightly outdated figure, but nevertheless it holds very good because we need to know how the evolution has taken place in terms of efficiency. So, if you look at efficiency of package, a package efficiency is - IC size by package size. Obviously, in a dip package, the package size is very large compared to the IC size and that is why in a dip package the efficiency is low.

So, the efficiency increased slowly through PGA, BGA and CSP. Finally, at a CSP wafer level package, the efficiency is very high. So, if you have the different ends, DIP on one side and CSP on the other side. You can very clearly say that CSP has a very high packaging efficiency because the package volume is much less in comparison to the die size in the CSP and comeback to a dip package or a QFP.

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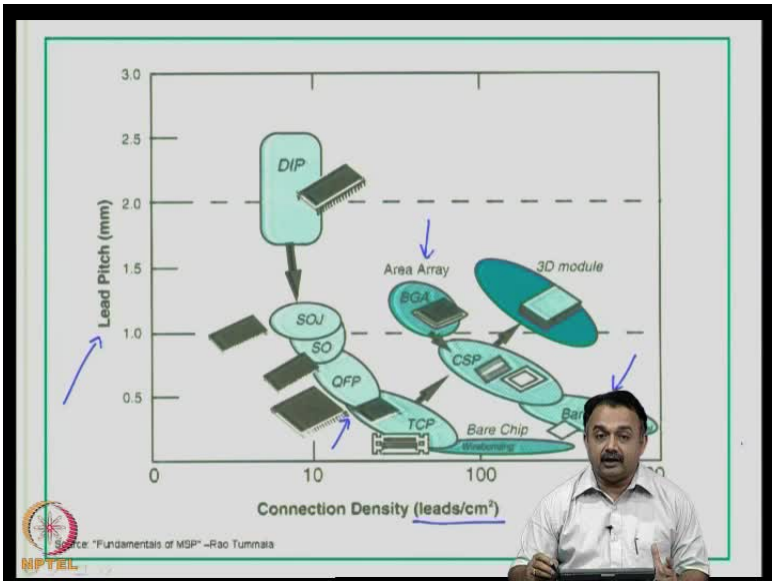

This particular graph or elastration will talk to you about connection density that is the number of pins, number of IO's per package. So, if you look at the graph in terms of lead pitch that is the distance between two edges and pins in a package. The midpoint of the pin 1 to the midpoint of the pin edges in pin 2. It is lead pitch to connection density that is number of leads per centimeters quad, when you actually mount them or design them to be mounted on to a system level printed wiring board.

So you have dip package which obviously the lead pitch is very large therefore, the connection density is obviously lower compare to a ball grid array where the lead pitch

You can work as low as 0.5 mm and therefore the connection density, when you use a number of area array packages replacing DIP packages or a QFP package will give an increase in the connection density. When use a bare chip, obviously a 3D module is formed. You can expect a multifold increase in the connection density.

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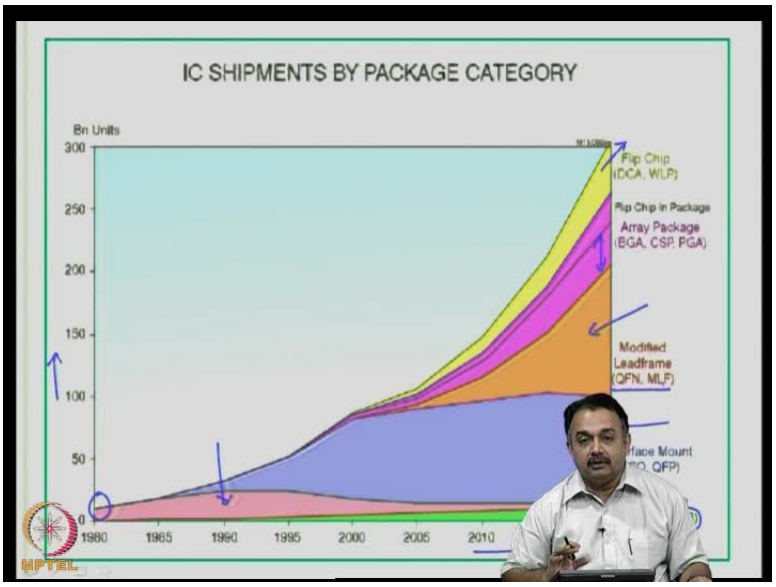

The best example is a CSP, which will have a better connection density compared to a even area array package or a QFP package, if you look at the volumes of packages that have been produced globally. This picture will give you a very nice idea because this is very current, if you look at the various colors that represent the various packages. On the left side, you see the volume in production in terms of billions of units. Here is the timeline going up to 20, you will see that compared to 1980, today, we are working at large volume of surface mount in our circuit design and that means the surface mount technology packages are coming out in large numbers in the market.

You can see that through holes, the presented by these colors is totally diminished compare to 1980. You can see very few numbers are coming into the market in the next five years. In the next ten years, you will probably see hardly any through hole components in the market because all of them would have been converted into surface mount format because the methodology of mounting and assembling surface mount devices are well known. The yields are very high and a throughput is very high. Therefore, people are opting for converting from through hole to surface mount.

You can absolutely see large growth of flip chip, which is not at all there in the 1980s to 1990. Then we talked about area array packages, which have a very high growth rate. compared to the last two decades, BGA and CSP, a pin grid array, bare die and that is your chip on board process is also catching up. As u know, if I am asking you to specify the application areas for chip on board, typically it will be for handheld applications and then modified lead frame packages like quad flat. No lead or micro lead frame packages are also increasing in terms of manufacturing numbers. So, you can look at this graph, the first thing that strikes you here is surface mount technology; it is very a popular area array. Technologies are becoming popular and will continue for a long time. Bare dies utilize like flip chip or chip on board will continue to be used in prototyping and small volume category.

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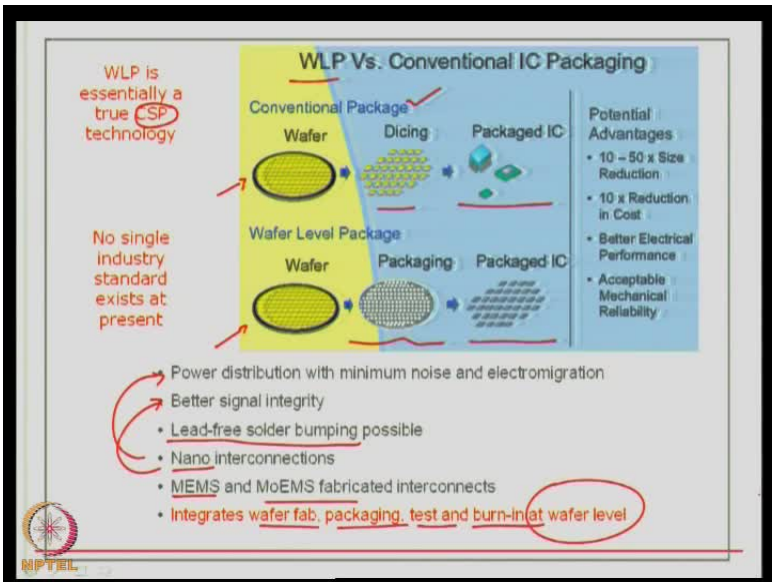

So, this is what I meant, what a wafer level package is and what is a conventional IC package. In one of the classes, you have seen the video or some other illustrations that the wafer manufacturing, it is singulated and then it is packaged. So, this is a conventional method of packaging a die. You create a wafer, you die it, each die is tested and then it is packaged. That is how you get the different formats like a dip or a QFP, but a wafer level package is lightly different. The wafer is done, the packaging is done at the wafer level and that means you are not singulating the die. Here, you are doing the packaging process on the wafer itself for each and everyone of the qualified die and then you are singulating it.

So, the singulation process is done after the individual IC's are packaged when it is at the wafer. So, what are the advantages? You can do away with a lot of budgeting and they can be 10 to 50 times the size reduction because you are doing it on wafer, you will tend to add much less package material, when it is on the wafer. The manufacturing technologies for these are getting well established. There is no single industry standard today that access for wafer level packaging because there are very few players in the global market for manufacturing wafer level packages. So, we need talk about wafer level package. Essentially, you are going to create a CSP package; Chip Size Package and that is the best thing that you can generate from a wafer level packaging. You are not talking about low density packages.

So, the advantages of using a wafer level package will be power distribution with minimum noise and the electromigration because the interconnect lengths are very low, better signal integrity, that is better electrical performance. Free solder bumping is possible and you can do this bumping process in the wafer itself. You can use lead free material and the interconnections are nano. As I mentioned earlier, it adds to better performance and these are ideal. Chip size packages are very ideal for MEMS application and MoEMS applications because this is not truly well understood today, as it is the monopoly of a very few industries. It integrates wafer fab packaging test and burn it in all the wafer level.

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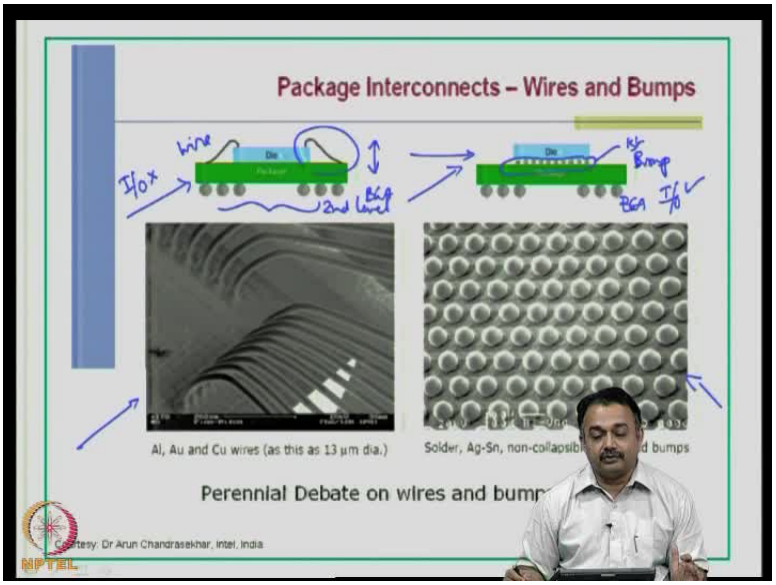

So, I hope you get the very clear picture about what a conventional IC packaging is and what a wafer level package. To produce a wafer level CSP, there are two types of interconnects. You are familiar with that one is the wires and the other is the bump. You can see the die here and then you can see the first level interconnect done by wires. In this case, you can see the die here and the first level interconnect is done by a few solder bumps. You can see the micrograph of the wires in this particular picture. We can see the row of wires that are attached by ball bonding. On the right side, you can see solder balls that are typically present in a ball grid array package or a CSP package.

So, now the question that many people debate is which is better and whether you need to use wires or bumps? So, wires have been there for a long time, right from the dip package to QFP. As the size diminishes, using a wire bonding becomes a problem because of the height factor in the profile of the package. If it is going to be small, then you can look at utilizing solder bump technologies, which are much suited for low profile packages small outline packages and CSPs.

There are also many other issues, in terms of electrical characteristics and thermal issues. Obviously, the package on the left is depicted as a BGA. Here, you can see the second level interconnect is a BGA. Here also, it is a BGA, but here the first level interconnect is a bump and here the first level interconnect is a wire. So, this is the basic difference between these two. We are not going to consider a wire and a lead frame because typically that is low dense. These two options that I have presented here in this slide are typically high dense packages because it is ball grid array, which enables you to work at low pitch, but the first level interconnect here are varied. One is a wire and the other is a solder bump.

So, the wires will obviously give you peripheral attachment. You cannot do an area array attachment. Whereas in the bump, you can do a complete area array attachment. Obviously, the number of IOs here can be larger compared to the number of IOs that you can generate here. So, like this you can find out various benefits in terms of a bare die in a solder bump format with the BGA compared to a wire with the BGA. So, again it depends on the number of IOs.

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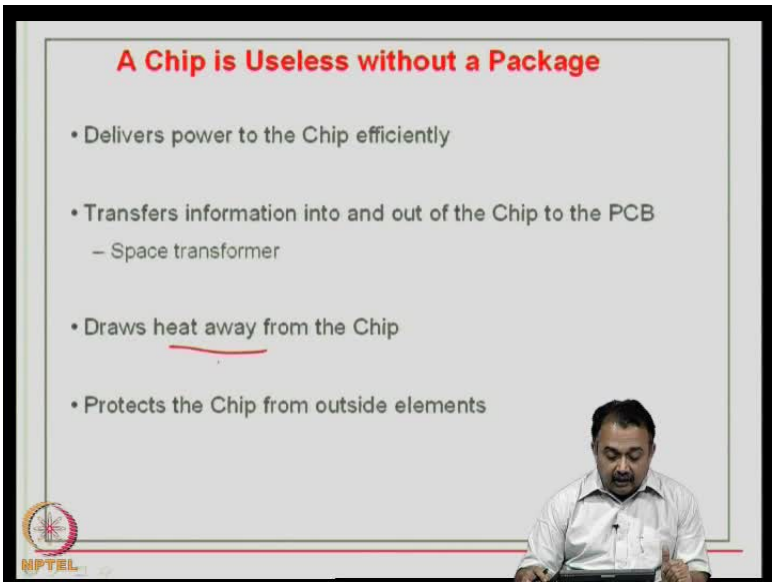

Now, is it really required to use a package? A chip is useless without a package. As many people would like to affirm because it gives you a well defined methodology for system functions like power delivery to the chip efficiently through a much larger pitch and the interconnect device dimensions.

You can utilize space transformer from the die to the package like a BGA or QFP or bend lead frame and so on. So, it transfers information in and outer the chip to the system level printed wiring board. The printed circuit board draws heat away from the chip. So, the package plays a very important role in removing some element of the heat away from the chip. So that the die does not crack, when it is powered up and if there is no sufficient cooling, it produces the chip from outside elements.

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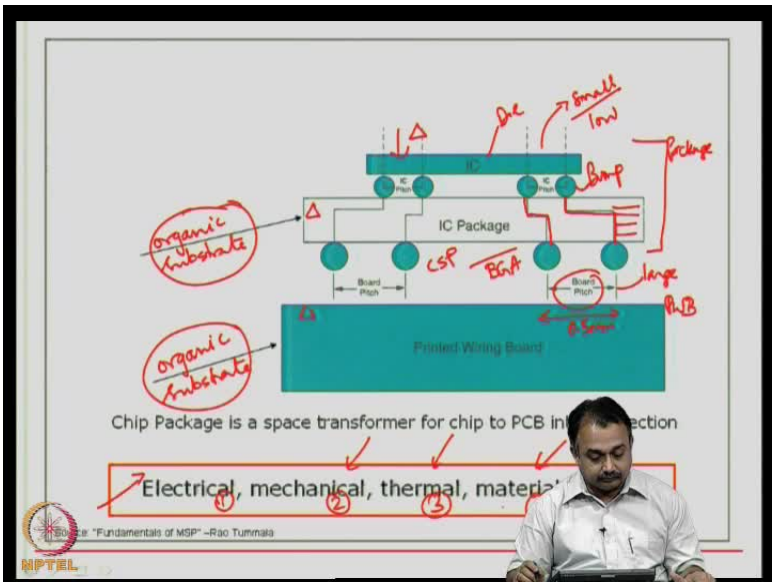

This is another slide that talks to you about the same point. That is chip packages is the space transformer for chip to PCB interconnection. Now, if you look at the arrow here; this is typically… For example, an organic substrate that you can think for system level printed wiring board, then you again have an organic substrate that could be used as a substrate material in the package. So, this part of it is known as the package. This is your PWB and this is the space transformation that you are talking about. Here, this is the die and this is the bump that comes out from the die. So, you can see this pitch is very small - a low pitch die. Then the IOs from the bump or space transformed through the multilayers of the IC package. So, you can imagine that this package is a multilevel organic substrate, multilayered organic substrate. Through that your pitch has become large. So, you are able to fan out the low pitch at the die end to a larger pitch at the back of the package and that is typically a ball grid array package. It can be a CSP package and these are advanced packages. You are able to handle this kind of a pitch. Let us say this is 0.55 mm or 0.33 mm and you are now able to handle this size of pitch. When you look at it, technology is available to mount this particular device on to the printed wiring board and established a second level interconnects.

Now, when you look at such a system, where you have a die and then you have an organic substrate for the die housing and then a printed wiring board. If you power up the circuit; this kind of a circuit, for example, electrons start flowing from the die through the solder bump, through the multilayer substrate to the BGA solder balls and what

happens is the host of electrical, mechanical, thermal and material issues get changed. They may not realize it at first. When you power up the circuits, there is going to be a lot of electrical issues that come up because we do not know what is the track width length. We do not know what is a dielectric constant of the organic substrate that you are using and we also do not know what is the environment in which the package is going to be mounted. What is the neighbor on the system level printed wiring board, which will interfere in the electrical performance of this particular die.

So, there can be issues like cross talk impedance issues and other electrical parasitic takes that you have to take care of, which will become visible. If you try to test these kind of electrical issues, then we have mechanical issues. If you do not take care of thermal management, then typically your die can crack. This is a very important area, where heat can play a major role. Your die can crack your package and can get warped. Your board surface and the solder joints can get affected due to thermal issues or the thermo mechanical readability becomes a question.

Mechanical issues like, if you look at vibration or mechanical shock just by dropping, then there can be shock and that can be transformed to the solder bump or the solder joints of the PWB, which can result in a failure; electrical failure. Then materials issues, when you design the particular package for which a particular organic substrate is used. If you are going to use dielectric materials, which are going to be conduced for the application and then you are saved. Otherwise, properties for these materials like dielectric constant, moisture absorption, the thermal core efficient of expansion and another important thing called as the glass transition temperature of the organic substrate, which we are going to see in detail, when we come to PWB technologies. They are going to play a major role in defining the system. If I call this as a system, all these four points: electrical, mechanical, thermal and material issues are going to play a major role

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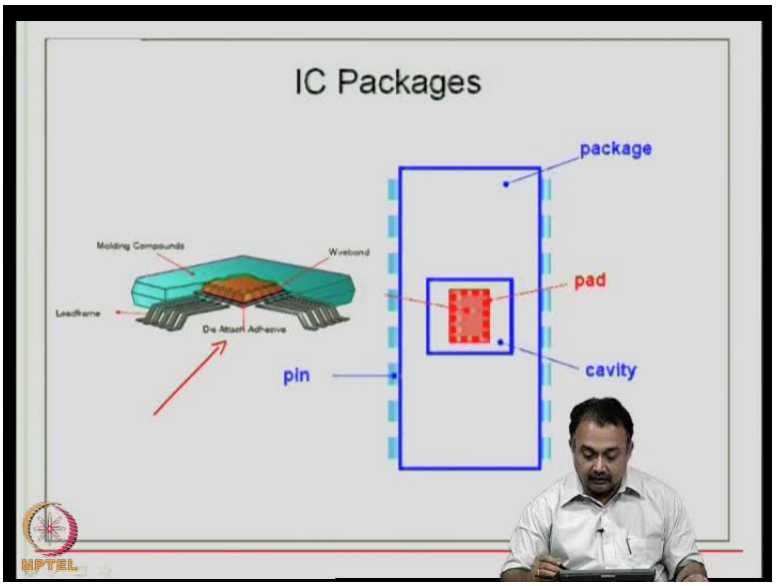

So, how does an IC package look like? When you open up a package and see, it shows a package that is typically removed from the epoxy material and a cross section. You can see the molding compound on top the lead frame. The lead frame is here and there is a die attached to the center on a suitable substrate, which is attached by a die attach adhesive. You can see the wire bond and then the periphery of the lead frame. So, this is typically inside of an IC and this gives you a top view of the IC package. This is how the dip package is. For example, these are the IO points that you are going to utilize to interconnect to your printed wiring board. This is the package material and this is the IO pad or the bond pad of the die. This is the cavity and so there are different formats for a dip package, which we will see shortly.

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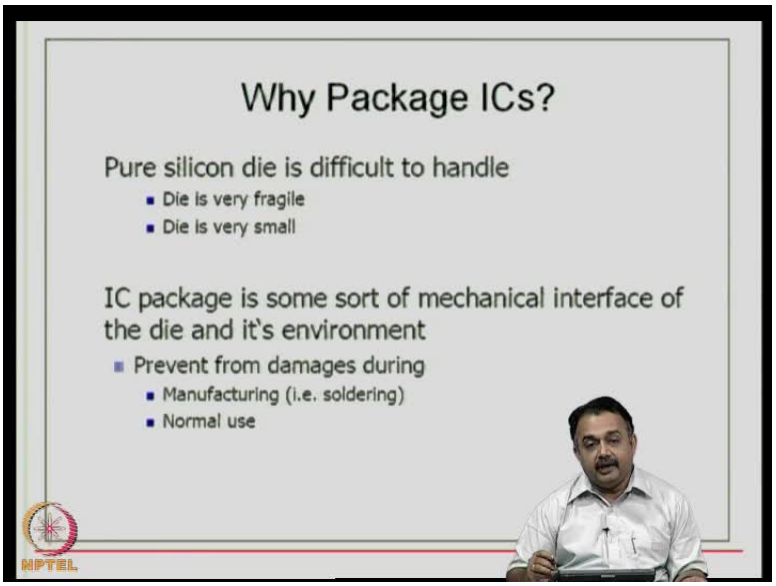

So, why package ICs? Because pure silicon is actually difficult to handle as the die is very fragile. It can be sensitive to the environment and to your touch. There are lot of organic materials in your hand. The assembly becomes difficult and so it is a procedural problem. The die is very small and it is diminishing, as we have seen in various system applications. Today, in huge microprocessors, the die can be very large, but still they are very sensitive. IC package is some sort of a mechanical interface of the die and the environment. So, it prevents from damage during manufacturing, especially soldering, where lot of heat will be involved. Your first level interconnect cannot be disturbed or spoilt during the soldering process, which involves high temperatures and also normal day today use, after the device has been manufactured.

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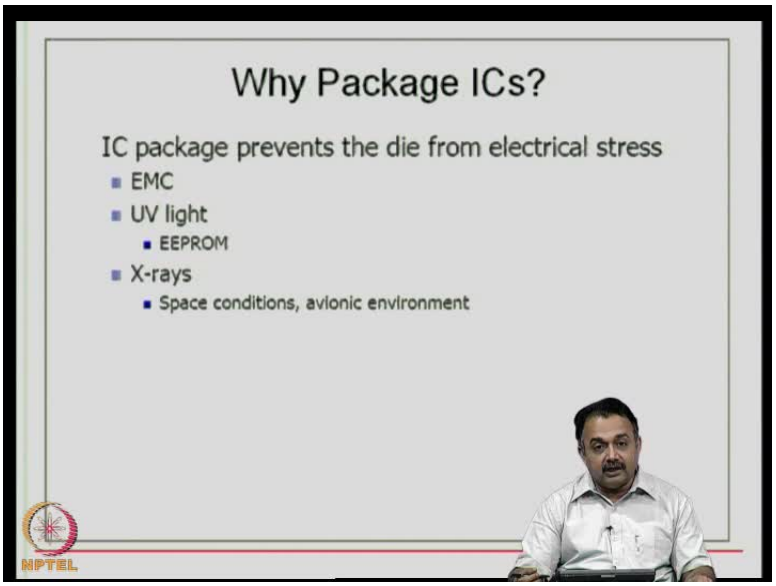

You also prevent the die from electrical stress like electromagnetic compatibility or EMI- Electro Magnetic Interference from the system level printed wiring board because you are going to use various other devices. For example, expose it to UV light by either doing a programming like EEPROM. During the operation, if there is any expose to UV light, then you can have electrical stress that can creep into the system and spoil your first level interconnects. Then X-rays like space conditions and avionic environment. These are the area, where you can expect damage to the die and that is why it needs to be protected.

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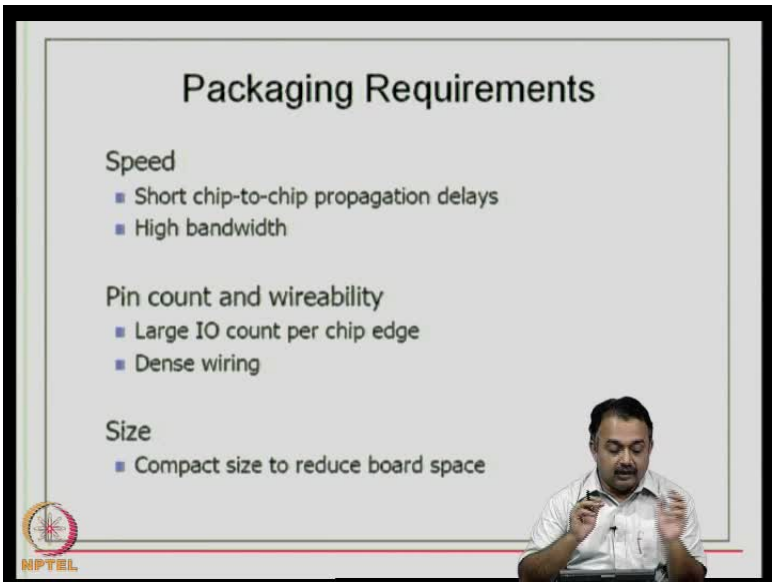

So, the packaging requirement is speed and it is a major issue, which means chip to chip propagation delays should be shorter. The same holds good, when you talk about interconnect at the second level printed wiring board. Obviously, this is a major consideration, when you look at the VLSI design. The interconnect links are very small then high bandwidth pin count and wireability is a major requirement. All IC manufacturers look at increasing the number of IO's per chip, there by increasing the wiring density. You need to reduce the size of the device because today, the product size is also reducing and space in between the board also gets reduced.

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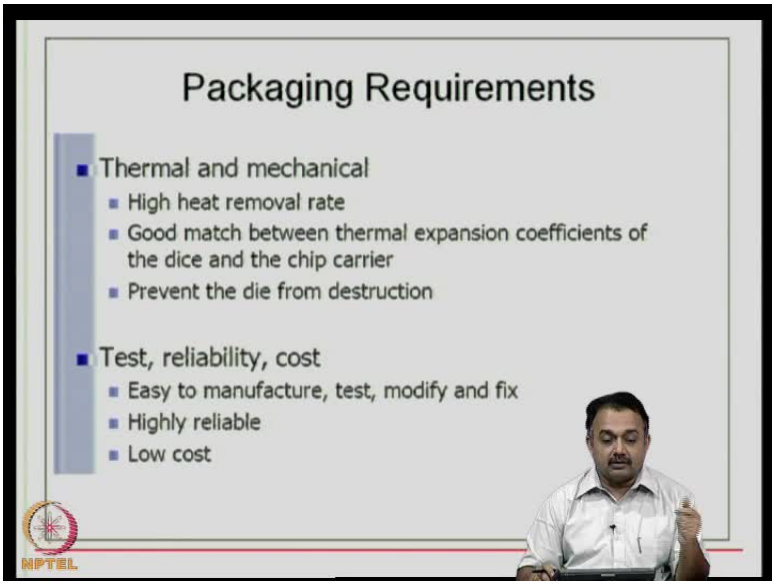

I have repeated this time and again. One of the important packaging requirements today is that the thermal and mechanical stress needs to be reduced on the device. So, you should have a high heat removal rate. Good match between the thermal coefficients of expansion of the die and the chip carrier. So, the chip is the silicon and the chip carrier can be a plastic. They have different TCE's and that is the thermal coefficients of expansion. Therefore, how do you take care of thermal mismatch, when you are using these materials, but at the same time, for such a device, you need to use a plastic because it is economic and prevent the die from destruction during such thermal flare ups that can happen during the powering up of the circuit.

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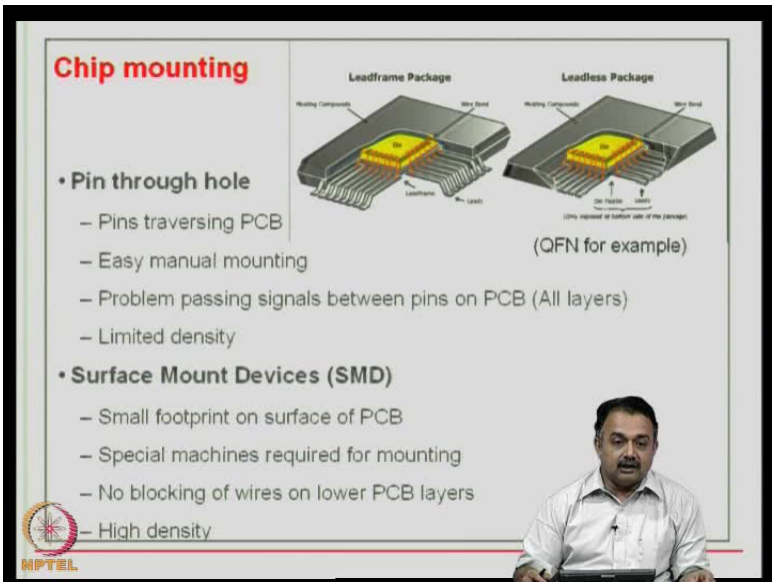

Then you talked about electrical test, you must be able to test the device of the package easily, after it is packaged. Then you should be highly reliable and of course, low cost. So, chip mounting can be… As we have seen earlier, pin through hole means your package should have pins that should traverse through the PCB and easy manual mounting, when we use a pin through hole format. Instead of depending on automated equipments, you must be able to mount these devices like your dip package here. You can use this dip package and mount it on a printed wiring board for the holes.

It has been manufactured and you can use your bare hand to simply insert the device into the system level printed wiring board. Obviously, there is a Problem in passing signals between pins on PCB's. When you have pins, you cannot utilize the area on the other side of the printed wiring board. Therefore, you are using the real estate and you are loosing in terms of connection, density or the pin density. It is very difficult to pass the number of lines between two such pins and there is a restriction on the number of routing pins. Therefore, the density is reduced and then you can opt for surface mount device because it has got a small footprint and it utilizes only the surfaces of the PCB rather than going through the PCB. So, typically this kind of package; the QFP or your BGA or your CSP will be utilizing surface mount technology. Even your pin grid array here, (Refer Slide Time: 54:57) utilizes pin through hole technology like your dip package.

Therefore, for this you requires special machines. For mounting, the assembly technology becomes different, but there is no blocking of wires on the other PCB layers because the pins do not block. There are no pins and the surface mount technology means the pins do not come to the other side. Therefore, you get more area on the other side of the printed wiring board to route your tracks. Therefore, this kind of a format for chip mounting will result in high density.

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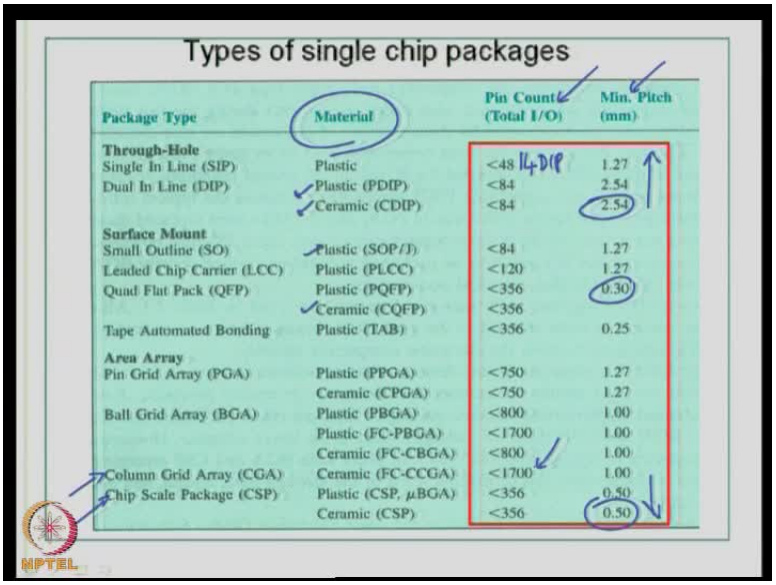

So, the types of single chip packages can now be classified as: through hole packages, which is single in line package, dual in line package and they can be plastic. So, these are the materials that you can think for these package types. So, through hole it can be a plastic package or it can be a ceramic package and then you have surface mount technology, where you have different types and again the types of material that are used is either plastic or ceramic.

You have small outline package Leaded Chip Carrier - LCC, quad flat pack and tape automated bonding; tab package, which is again in surface mount methodology. The other classification is area array package in which you get pin grid array and ball grid array here you can have plastic pin grid array plastic ball grid array ceramic pin grid array and ceramic ball grid array and then you have another variety called column grid array.

This is a particular methodology or package format, which has got a limited circulation. You do not see this in high volumes, typically used in boards, which are highly dense in terms of requiring thermo mechanical reliability standards to be very high like in military applications and so on. Then you have a finally, the chip size package in which you can have plastic chip size package as well as ceramic chip size package.

So, the other two columns here will indicate to you the typical pin count or the total IO that you can probably see the availability in the market today. This also gives minimum pitch. So, you can see minimum pitch starting from 2.45 mm to something like 0.5mm and lower than 0.5 today, in terms of QFP; 0.3 and so on. 0.3 is also available in BGA and CSP formats today. So, you can see the range in minimum pitch. As you go through this table and also you can see the high pin count. Typically, look at even less than 48. Many of you would have seen 14 pin dip or today you can see FPGA components coming in BGA format, which has got over 1700 solder balls, which represent the total IO's that need to be connected on to a printed wiring board.

So, I will stop here. In this particular class, what we have seen basically is the definition for single chip module. We are going to see what a multichip module is in the next class. We are trying to see how ACM or ACP can be classified based on assembly technology, based on materials and so on. We have ended up looking at the important things like formats available and pin counts. How relevant pitch is that IO pitch in deciding the package format for various type that we are seeing in the market today. Thank you.