An Introduction to Electronics Systems Packaging

Prof. G. V. Mahesh

Department of Electronics Systems Engineering

Indian Institute of Science, Bangalore

Module No. # 02

Lecture No. # 10

Wire bonding, TAB and flip-chip – 2

-Tutorials

Welcome back to this module. Actually, we are in the last segment of the second module, where we are discussing semiconductor overview, fabrication overview.

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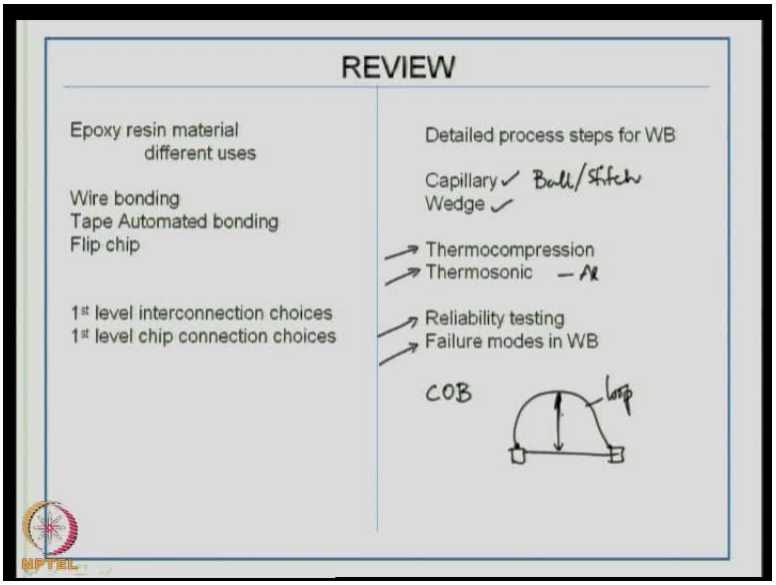

We saw the front-end and back-end processes. We saw the chip interconnection choices, that is, the first level interconnection choices. In the last class, we talked about epoxy resin material. We also looked at the different uses or applications for this epoxy resin material in the packaging industry. We dealt some time on wire bonding, tape automated bonding and that is TAB, flip chip, which also known as C4. So, we also spent a lot of time on understanding, what is a first level interconnection choice. You can also call it as

a first level chip connection choices. So, basically, there are three chip connection choices, which is wire bonding, tape automated bonding and flip chip. We also saw in the last class about the detailed process steps for wire bonding. In that we spent some time on two basic tools used in wire bonding: one is known as capillary tool or capillary method to wire a die bond pad from the die onto a substrate and the second one is wedge bonding. So, basically, two tools are used: one is a capillary and that creates a… as you recollect a ball bond and a stitch bond on the other side of the ball bond. Then wedge tool creates a wedge bond. Two methods of creating wire bonding or two types of equipments that are available for wire bonding would be- thermocompression wire bonding and thermosonic wire bonding. If you can recollect, thermocompression would require the use of appropriate temperatures, pressure to enable the wire bond to happen at a quicker time and with a very good metallurgical bond.

In addition, thermosonic bond will use some form of ultrasonic energy vibrations to reduce the temperatures. So, materials like aluminum and if you want to use it as a wire bond material, then you would prefer to go in for a thermosonic bonding. So, it depends on what type of equipment you want and what material you would require for that particular application. As I said before, wire bonding can be done even on applications like chip on board, which is mounting a die onto an organic substrate. Then wire bonding from the bond pad on the die to the bond pad on the substrate. So, chip on board is in fact, establishing a connection at the second level substrate, which is a printed wiring board. So, we will see much of it later.

We also talked about the failure modes and the testing methods. Once you establish a wire bond, it is always necessary to look at the reliability of the wire bond that has been established. One should basically have some idea about what kinds of failure can happen in the wire bond. This is the essential part because you are creating a loop between this substrate (Refer Slide Time: 04:37) and this is the loop height. If you can recollect, this is the loop. So, you need to find out, how this loop behaves during thermal cycling.

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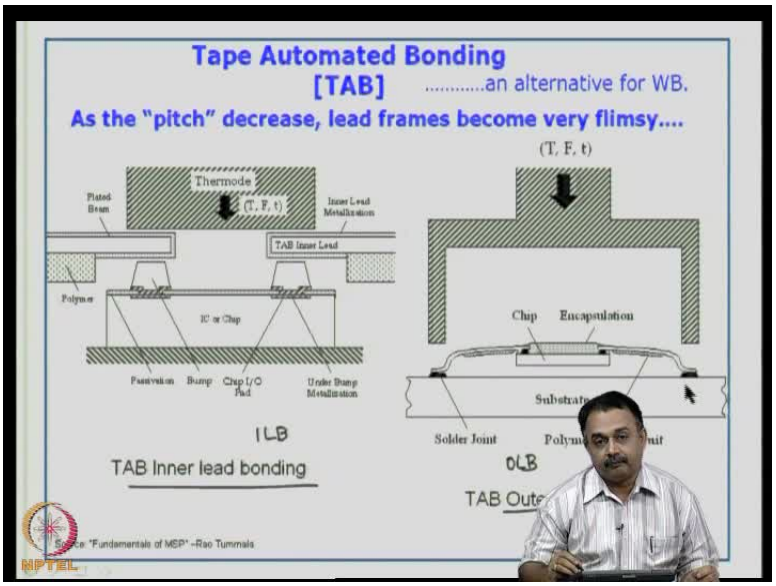

Today, we are going to talk about some details about Tape Automated Bonding methods like what we have seen for wire bonding. So, tape automated bonding is an alternative for wire bonding. As the pitch decreases, lead frames become very flimsy. Basically, you require some method to hold the lead frames. In this case, we are using a polyimide tape. I think I have shown you a picture in the last class about a polyimide tape, which houses these lead frames. You are going to introduce the die onto the lead frame center and then establish thermocompression bonding, which is now called as tape automated bonding. So, the name tape comes from polyimide tape, which is custom built for a particular design and for a particular number of IO's in a particular design. So, in a particular design you will have 48 lead frames or 60 lead frames or sometimes even very less about 16 lead frames and that depends on the design.

So, in tape automated bonding, you will encounter two types of bonding: one is known as the inner lead bonding, the other is the outer lead bonding, that is, ILB and OLB. What is inner lead bonding? So, if you look at this picture (Refer Slide Time: 06:33) here, there is there is the IC or the chip ready to be bonded. There is a frame on which the IC is mounted using or probably introduced… You can see here; this is the polymer tape, the ends are shown. Remember that this is a cross section, what we are seeing is a

cross section of the inner lead bonding methodology. So, you have the polyimide tape, which houses the plated beam structure or the lead frame on both sides. Then these are the bond pads at the die level. So, if you look at the cross section here, we are seeing similar bond pads or the bump structures. Now, these are slowly introduced from the bottom to the area, where it has to be bonded at the lead frame site. Now, from the top a thermode, a hot plate kind of a material is introduced slowly. So that the lead frame and the bond pad are touching each other at a particular pressure, temperature and time. depending upon the material that you have used in the lead frame. This creates a thermocompression bonding at this site and that is how the bond is established here. So, this represents the inner lead and this is the inner lead in the polyimide tape. So, the other materials in this cross section that you see here is this bump of the die and it has got some kind of a under bump metallization also known as UBM. This is Chip IO pad and these are the bumps. There is some passivation done to protect it against the environment.

Now, what is outer lead bonding? If you look at the next picture alongside, now, the inner lead bonds have been completed. You can see here, (Refer Slide Time: 08:56) this is the die and the ILB's have been completed. It is now encapsulated with epoxy polymer material and this is cured. So, the curing temperatures are given by the manufacturer of the polymer. So, you can say about 80 to 100 degree centigrade for about 10 to 20 minutes and then we are now looking at establishing the outer lead bond. So, this is the substrate, which houses the site bond pad, where the outer leads of the lead frame will rest. Similarly, another thermode will come exactly at the bond pad site of the substrate and the lead frame, which is rested on the substrate. Now, using appropriate temperatures pressure and time, you can now do the thermocompression bonding at these sites.

Remember, this is a cross section. You will have multiple leads along this array and also here. So, this is what you call it as a gang bonding. So, in one shot, various number of lead frames are bonded. So, this is known as outer lead bonding and you can see here, the original polymer tape, which housed the lead frame is still present there. So, this is the advantage of using tape automated bonding, where the lead frames are very small in size, in terms of pitch. They can be very flimsy and they do not bridge each other

because they are held by the polyimide tape. Now, you can see that there is a solder joint on which the lead frame is resting and then you are doing a thermocompression bonding. So, this is how ILB and OLB are generated in a tape automated bonding process.

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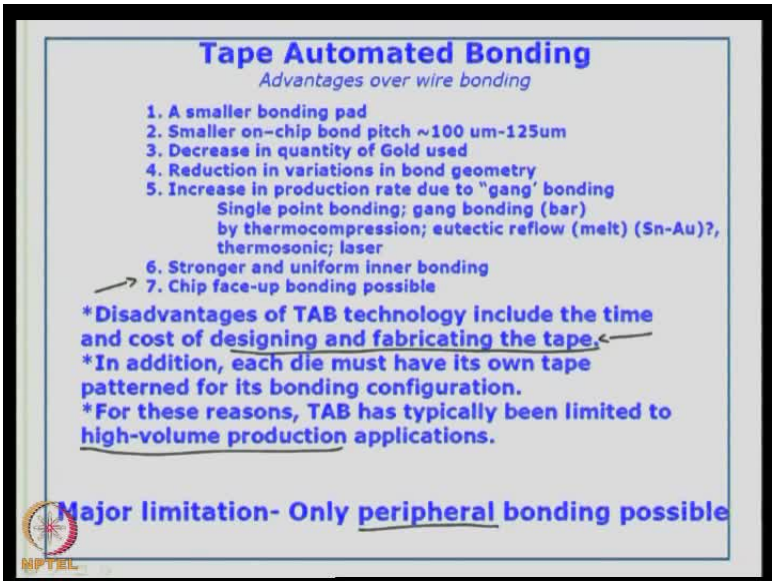

The advantages of TAB over wire bonding is that: it has a smaller bonding pad, smaller on chip bond pitch; typically about 100 to 150 microns, decrease in quantity of Gold used; obviously, you can work with other lead frame materials, instead of just using gold or aluminum and so you have choice of using different materials in the lead frame structure, reduction in variations in bond geometry, increase in production rate due to gang bonding. I just mentioned to you about this. Typically, in a wire bonding it is a single bond operation and that means a bond has to be completed before another bond is established. So, it is time consuming in that sense, but in tape automated bonding, you can finish the entire periphery in one shot by using a suitable Thermode, which will do a single point bonding also known as bar or gang bonding by thermocompression. You can also use thermosonic. If it is a very small structure, you can use laser to activate the bonding process. Now, this is a stronger and uniform inner bonding. The advantage here is chip face up bonding, it is possible and that means the chip IO's are facing the top.

Then you can establish the bonding by introducing the die from beneath onto the alignment sites of the polyimide tape.

The disadvantages of TAB technology include the time and cost of designing, fabricating the tape. So, this is the process, where a lot of time is spent because it is not a universal design. Every application requires a particular circuitry in which you have decided to use a particular die with a particular number of IO's, which does for TAB technology. So, you are required to calculate the area of the tape, the alignment of the pins in the periphery around the die and some time is spent in designing and fabricating the tape. In addition, each die must have its own tape patterned for its bonding configuration. For these reasons, tape automated bonding has typically been restricted to high volume production. So, this particular methodology will be advantageous, if you are running millions, especially in hand held products. As we have seen, this is used in smart cards RF cards or your digital radio circuitry, where such design is being used. Today, the major limitation of TAB process is that you cannot use area array bonding; you have to limit yourself with peripheral bonding.

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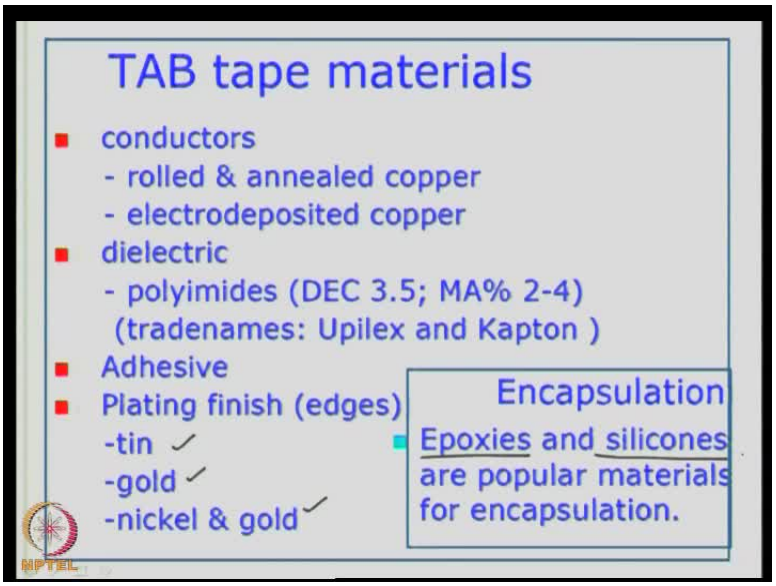

The tape materials that are used in tape automated bonding process are- the conductors can be rolled and annealed copper or electrodeposited copper. You will see later that we

are going to discuss about different types of copper that is used in electroplating. In upfront, I would like to say that these two methods for manufacturing copper: rolled and annealed copper, electrodeposited copper will have different properties for the copper. So, you have to carefully select the type of copper conductor and also the dielectric that is normally used is a polyimide tape, whose dielectric constant is around 3.5 and moisture absorption is around 2 to 4, which is fairly high compared to epoxy. some common trade names Upilex and Kapton are commercially used.

An adhesive will be used because on the polyimide tape, the lead frames are fixed at the manufacturing site. So, you require a very good adhesive to hold the lead frames onto the tape. So, different adhesives may be used and then the plating finish for the lead frames could be either tin or gold or nickel and gold. Obviously, you are looking for better contact resistance and therefore you have a wide variety to choose from. The encapsulation process is a part of the TAB process. As you have seen, the very common epoxy material is used for encapsulation, but other materials like silicones can also be used for encapsulating the inner lead bond.

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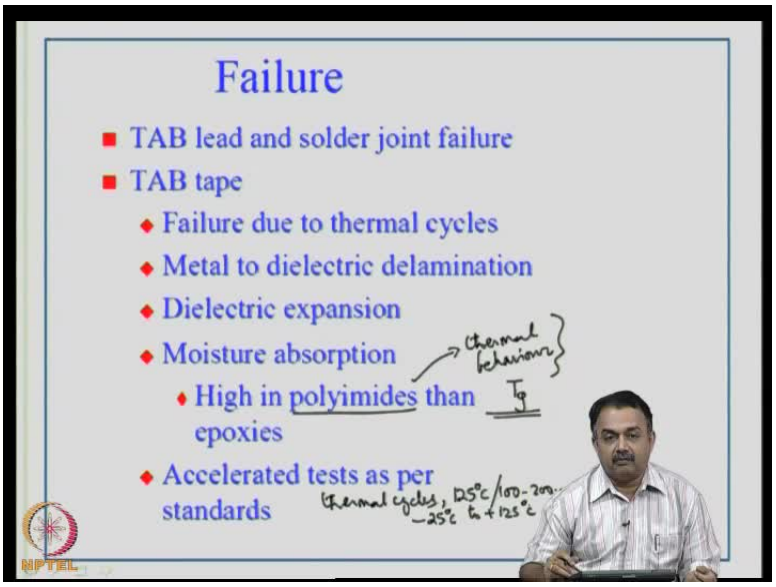

Like wire bonding, here also you have to do the test after the formation of inner lead bonds and also after the formation of outer lead bonds for looking at the failure

mechanism. So, TAB lead and solder joint failure needs to be looked at the tape material that is used can fail due to thermal cycles. There can be delamination between the metal and the dielectric material at the lead frame area. The dielectric should not expand; there should be less moisture absorption at the dielectric choice that you have taken, whether it is a polyimide or an epoxy or cyanate esters and so on.

The moisture absorption property is an inherent property of these polymers and so it is very high in polyimides and epoxies. If you look at the stand point of thermal behavior, then you would like to use polyimides compared to epoxy because there is a property called Tg; glass transition temperature at which these polymers become very soft, when it is subject to heat load. Therefore, people prefer polyimides than epoxies and so we will look at Tg, when we discuss organic substrates at a later point of time. The accelerated tests as per standards need to be done. So, what are these accelerated tests? Typically, you run thermal cycling of these finished TAB boards. There are certain guidelines: it can be constant temperature like 125 degree centigrade for 100 hours, 200 hours and so on, before you really look at the failure happening at the bond site. In some cases, we also use thermal cycling from negative temperatures. It is typically around minus 25 degree centigrade to plus 125 degree centigrade for various cycles, number of hours to qualify the TAB connection.

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Here, I would like to show you a video clip about Tape Automated Bonding process. Tape automated bonding is a high volume technology for making the interconnection with silicon devices. The interconnects are simultaneously attached to the silicon chips using hot pressure welding or soldering processes. It is often used in components like smart cards, the bankcards, tagging devices and SIM cards for mobile phones. The technology is also used in the manufacturing of pocket calculators and digital radios.

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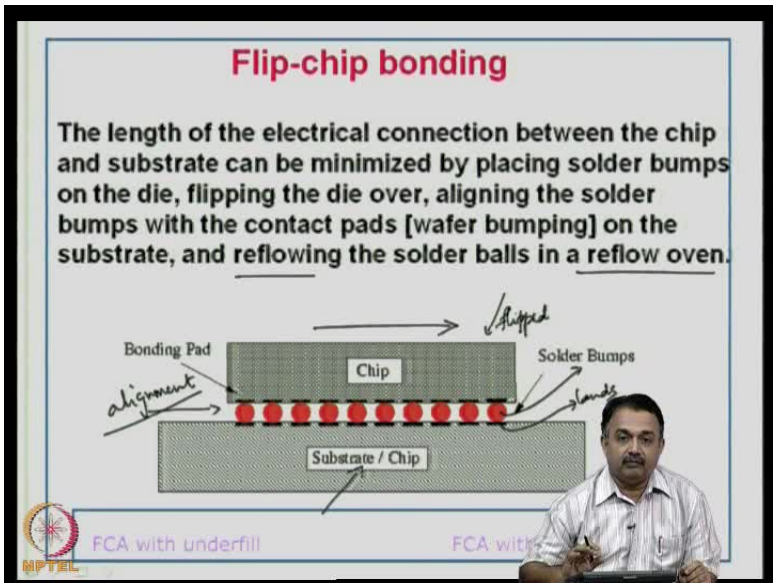

That completes tape automated bonding. Now, we will get into the next method of chip connection or the next choice available for us other than wire bonding and TAB; this is called flip chip.

So, what is a flip chip? I think you are familiar by now. So, basically, the chip is flipped over as you can see here (Refer Slide Time: 20:11). Now, you require a substrate for the chip to be bonded. In some cases, as you will see later in the next chapter, the chip can also be mounted on another chip, which has got the bond pads. So, it is a kind of integration; like a system in package kind of a configuration. In this example, for defining, what is a flip chip bonding? Let us look at it, as a simple substrate it can be an organic substrate or it can be a ceramic substrate. Now, you can see that there are bond pads at the chip side and then there are the bumps. So, these are the solder bumps here and you can see that there are landing sites on the substrate onto which the chip will be flipped over and perfectly aligned using appropriate equipment. So, in this flip chip bonding, the length of the interconnection between the chip and the substrate is minimized by using solder bumps on the die, flipping the die, aligning the solder bumps with the contact pads. You can call it as wafer bumps on the substrate and reflow the solder balls in a reflow oven.

So, here you are going to use a thermal process called reflow in a reflow oven and that means you are going to activate the solder material above its melting point. Then you are going to cool it and so a connection will be established between the molten solder and the material on the bond pad in the substrate. So, this is a complete reflow of the materials; both at the chip side as well as at the substrate side, if it is the same material, which has the common melting point.

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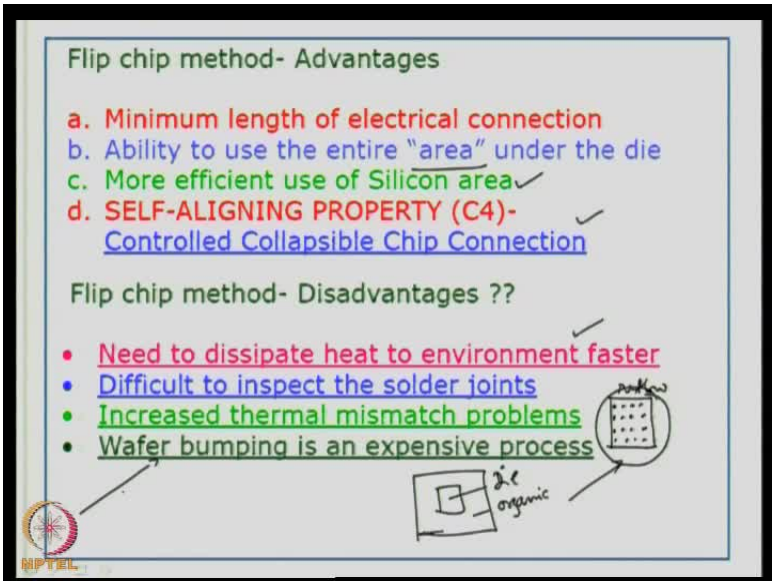

The advantage is that the connections are perfect. It is a metallurgical and it is a complete bond by fusion of one chemical into the other. In most cases, it is the same material that is the solder material. The advantage is that because of surface tension, the alignment is going to be almost at every point of time very perfectly because the surface tension of solder will pull back the die into its original coordinates on the substrate. So, even during reflow, there is a slight movement of the die towards the reflow and what happens is that? Because of the surface tension from the solder, it pulls back the chip to its original position. So, you do not have to really worry about misalignment during flip chip bonding. Misalignment can happen in some cases of wire bonding and TAB, but not in the case of flip chip bonding, if the temperatures during reflow, other parameters during the process are under control. So that is why this is called a C4 process; what is C4? Controlled Collapsible Chip Connection. So, during the reflow, the bump collapses and it melts. It is controlled and the connection is established because of the surface tension property of the solder material, which pulls back the chip to its original position, if a displacement is noticed.

Now, the advantage of using a flip chip is- this is probably the best method, where you can see minimum length of electrical connections. That is what we are desiring because minimum length of electrical connection will take away all the problems that are associated with electrical parasitics. If you look at the DIP package, where the lead frame

length is very high and a QFP package, where again it is minimized. At the same time, the distances are fairly large, but in the case of a solder bump that you see in a flip chip, it is almost 0 and so, you can get the minimum length in a flip chip. So, you need to utilize the advantages of a flip chip.

Flip chip can work without being packaged and that means it actually does not require a package. In a BGA or a CSP, normally we use a flip chip to establish the first level interconnection and then package it using plastic or ceramic material. So, flip chip gives us the scenario, where the entire area under the die can be utilized for more efficient use of silicon area.

We have seen C4 self-aligning property. What are the disadvantages? There is a need to dissipate heat to the environment faster, which a package material or the other processes like wire bond or TAB can probably do because of the length in the lead frames or the lead structures that establishes the first level interconnection. It is very difficult to inspect the solder joints because, if you look at the flip chip die, the bonds are established underneath the die. So, once the bonding takes place after reflow, you cannot inspect the connections under the die with your naked eye. So, you have to utilize equipments like x-ray or acoustic microscopy and so on, to look at the quality of the established solder joints. So, that is one requirement if you are going to work with flip chip bonding. Increased thermal mismatch is a problem because the silicon die is subjected to a lot of heat during power up, if you are going to mount it on an organic substrate, because the coefficient of thermal expansion of the die to the organic substrate are different. So, we will have some opportunity to discuss about this in the next chapter. There can be thermal mismatch problems, which can lead to die crack or warpage on the substrate. Wafer bumping is currently an expensive process; but today, with the increased use of flip chip, wafer bumping is now becoming affordable, but nevertheless expensive compared to a wire bonding or a TAB process. We have seen that wire bonding is most economical.

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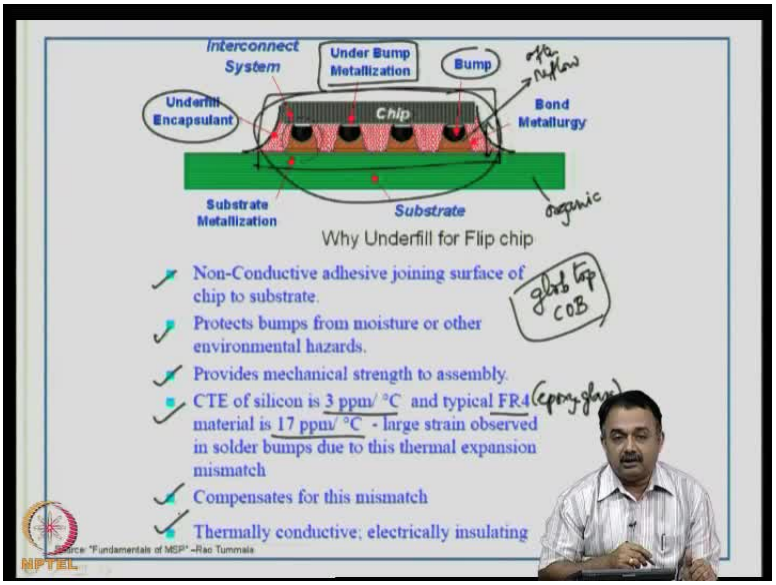

In a flip chip scenario, I told you that there is a small gap between the die and the substrate. You need to take care of that and therefore you use an underfill. Underfill is again an encapsulant, but in this case, the encapsulant is not put over the chip; the encapsulant is put in the area between the die and the substrate. As you can see here, (Refer Slide Time: 28:22) these are the bumps and these are the areas, where the new connections have been established after reflow. A new bond metallurgy has been formed and the shape is also different.

A chip will always have a under bump metallization we are going to see shortly, what is UBM? UBM is very essential for a flip chip to be operating reliably or function reliably. Now, underfill is required because in the previous slide, we saw and we talked about thermal mismatch. So, if you do not use an underfill, there is going to be thermal mismatch between the chip and the organic substrate, if this is organic material like an epoxy. So, the thermal coefficient of expansion of the silicon die and the organic substrates are different. Therefore, if you imagine a power up of this system due to heat building up at the die surface, you can expect the die to crack. There can be solder joint fatigue and also warpage on the substrate.

Nonconductive adhesive join surface of a chip to a substrate. So, underfill is basically a nonconductive adhesive material and it is not a conductive material. It is used in between

the chip surface and the substrate surface. It protects the bump from moisture or other environmental hazards. It provides mechanical strength to the assembly. So, after establishing the bond, you can see that the underfill system protects the entire assembly. Imagine this or compare this with a glob top. I talked to you about glob top and it is used in a COB, whereas underfill is used in flip chip onboard. So, this is a configuration for flip chip onboard.

You can see that I talked about thermal mismatch. This CTE or Coefficient of Thermal Expansion of silicon is 3 and that of FR 4. You can take it as epoxy glass composite, it is about 17 ppm. So, a large strain is observed during operation because of this huge mismatch in CTE. Therefore, the underfill can protect this entire structure or system and typically, you will use an underfill that has a CTE in between that of the die and the epoxy material or the substrate material that you have chosen. So that the heat flow is gradual and it does not affect the die surface or the organic substrate surface, which is also protecting the solder joint. So, the underfill material should be nonconductive, but at the same time, it should be thermally conductive and electrically insulating.

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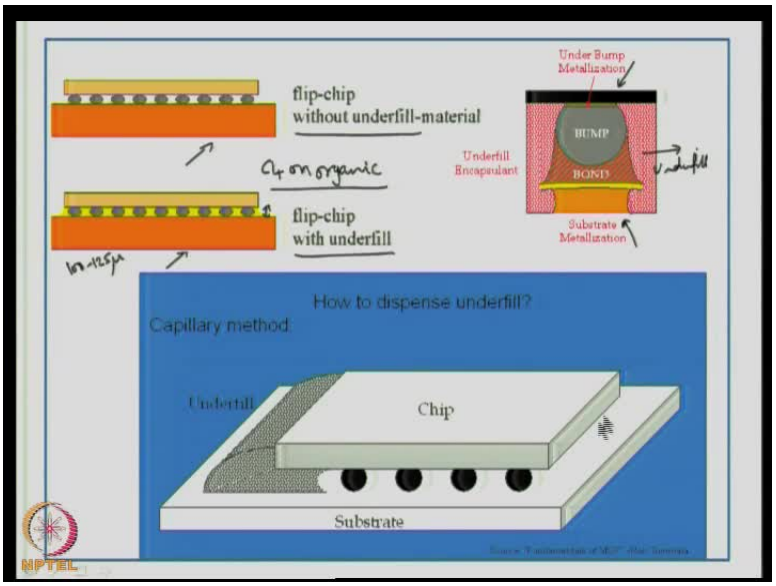

So, this is a example (Refer Slide Time: 31:44) or a illustration of a flip chip without underfill. Here, you see this is an example of flip chip with underfill. So, remember that

if you are going to do a C4 on organic, you should better use an underfill material. How do you use an underfill material or how do you dispense it, because the gap between these two is very small about 100 to 125 microns. Now, how do you dispense underfill? This is a liquid (Refer Slide Time: 32:20) and once the underfill is dispensed, it has to be cured. So, this is a cross section of the system, where you see the bump in the substrate metallization at the bottom. Then you can see the underfill material here, which protects the bump and the bond that has been established.

So, here you see the chip and the substrate. How do you dispense the underfill? You take the underfill liquid in a syringe. Once the bond is established between the chip and the substrate, you dispense the underfill on two sides of the assembly because of capillary action that is present. That is a small gap between the chip and the substrate because of the capillary action. The entire area under the die will be filled with the underfill. So, you do not require extensive mechanisms or equipment to apply underfill in this case. Just apply the underfill on two sides and as you can see because of the capillary action the entire area under the die will be spread with the underfill material.

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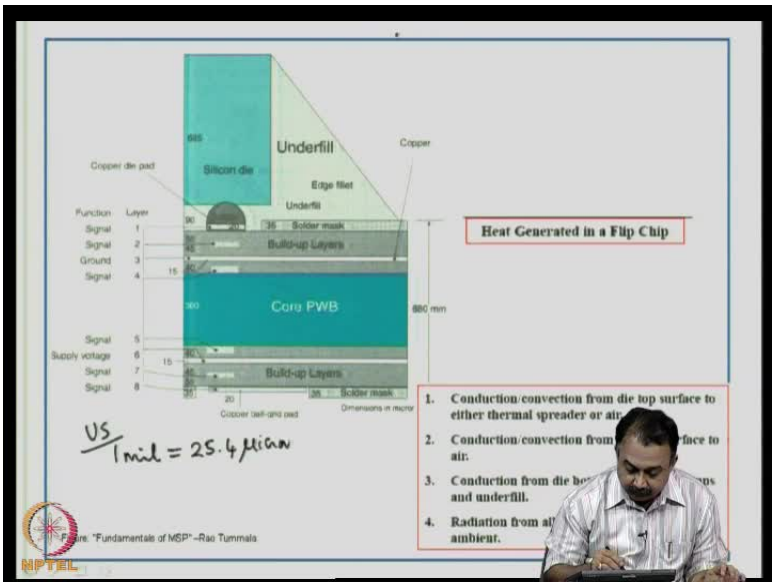

This is a cross section of the underfill. You must now be able to imagine cross sections, where you have the underfill, the bump, the silicon die, the printed wiring board or

organic substrate, which can be a multilayer buildup and so on. Now, the numbers given here are in mils- 1 mil is 25.4 microns; 1 mil is a U S military standard and 1 mil is equal to 25. microns.

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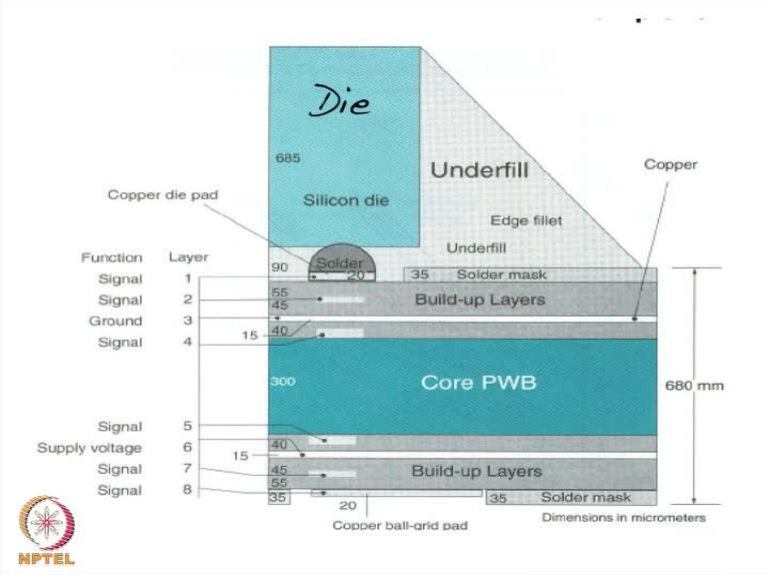

You can see the entire structure is a high density interconnect structure. So, you have an underfill, you have the die, you have the solder mask material, which protects the buildup layers of the PCB. You have the bump here and so on. So, this is a very delicate structure and when you operate or power up this kind of a circuitry, which utilizes a bare die or a package die, obviously heat is generated.

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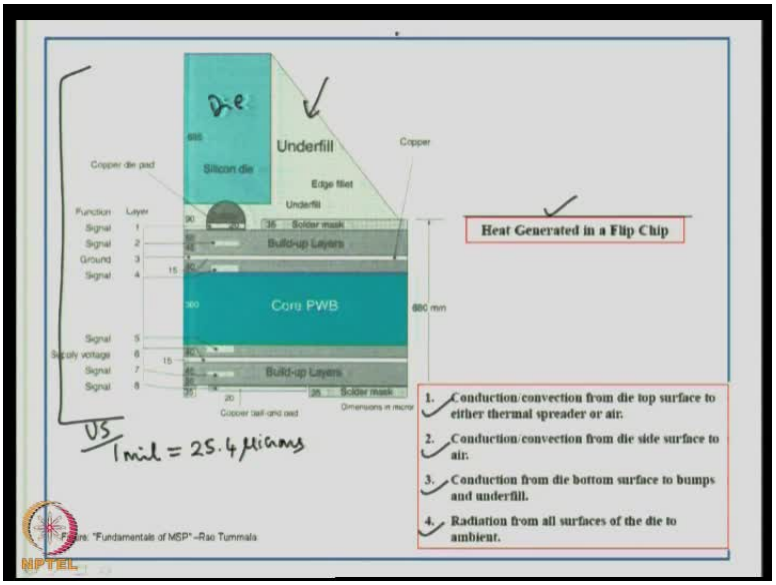

Let us look at the heat generated in the flip chip. What happens typically? There will be conduction or convection from the die top surface to either thermal spreader or air. Conduction or convection is from the die side surface to the air conduction, from die bottom surface to bumps and underfill. So, underfill becomes very important. Here, radiation is from all surfaces of the die to the ambient. So, these are the four methods. Conduction, convection and radiation are the three modes of heat transfer. In the case of a flip chip, if you are using a thermal spreader, it is advantageous. Otherwise, the die surface will take care of the heat dissipation from the air die bottom surface to the bumps, die top surface to the air and radiation from all surfaces to the ambient.

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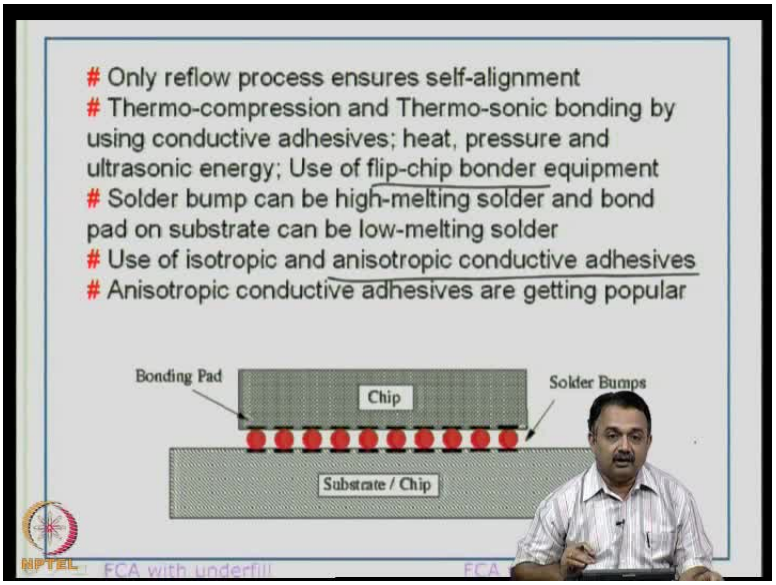

Only reflow process will ensure self-alignment, we have seen that. Thermocompression and thermosonic bonding is also possible for flip chip. Not only reflow applies heat, pressure and ultrasonic energy… So, in that case, you have to use a flip chip bonder equipment. So, flip chip can be attached by reflow or thermocompression bonding or thermosonic bonding in that case, you have to use a conductive adhesive. Solder bump can have high melting or low melting. Depending on the case, application and the bond pad on the substrate can be low melting. So, in that case, you can operate at low melting solder temperatures and establish a coating of the low melting flow to the high melting solder. In the case of a reflow, you can also use isotropic and anisotropic conductive adhesives. More people are using anisotropic conductive adhesives. Today, anisotropic conducting adhesives are getting popular because the difficulty with applying isotropic adhesives on the surface of the substrate, is increasing larger because of low pitch. So, you need better dispensers that need to dispense isotropic material accurately, but in this case, if you are using anisotropic conductive adhesives, you can work intelligently in the sense, how does it work.

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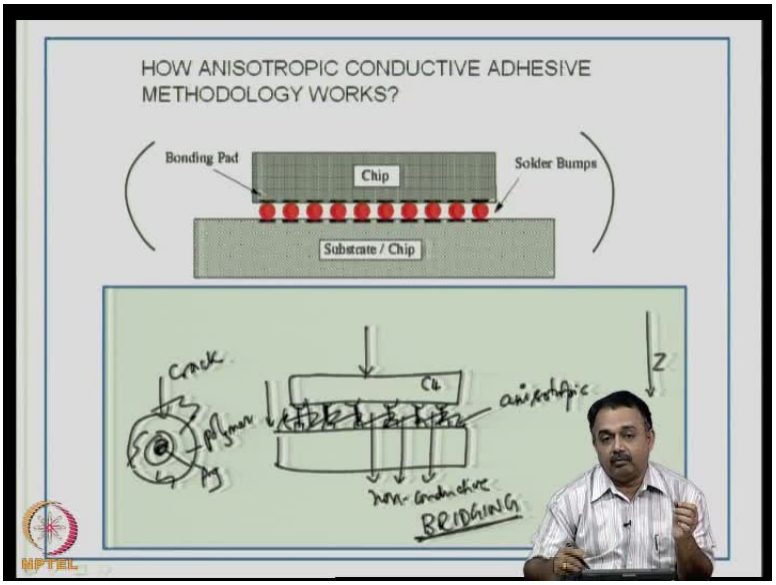

When we say anisotropic conductive adhesive, it basically conducts in the Z direction. So, in this case, assume a system here, where a flip chip and a substrate are there. Now, what you basically require to do is- there are the bond pairs on the substrate, you can apply the entire area with your anisotropic conductive adhesive. Now, you place your flip chip and now the bumps are there. Slowly, introduce them by using proper equipment and so that it aligns with the bond pad on the substrate. Now, what happens is that the entire material is initially conductive, but in the case of anisotropic material, if you look at a microscopic view of a globule of an isotropic material, there will be the conductor. Let us say, silver particle and then you have it coated with the polymer. Now, when you apply thermocompression bonding procedure, the polymer will crack and then this bump will get connected to the metallic particle inside. That will establish the connection with the bond pad on the substrate. So, the synthesis of anisotropic material conductive adhesives needs to be… or is it is definitely different compared to a isotropic material because you are going to embed the metallic particles in a polymer, say it is a globule. The different arrays of globules are present and these globules will crack only at those bump sites, where pressure is applied. So, for example, these areas will still remain nonconductive. Otherwise, you will end up with bridging. So, bridging does not take place because it is anisotropic conduction.

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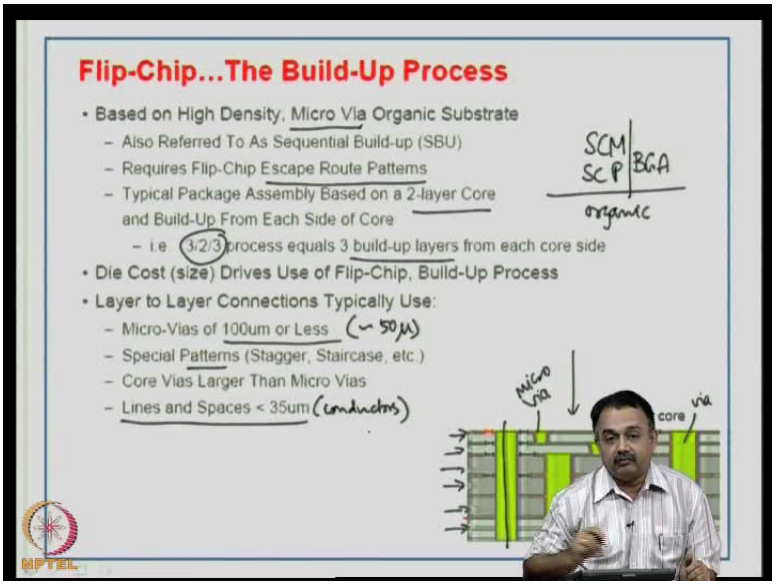

For these kind of flip chip processes, you require a high density interconnect organic substrate, even if you are making single chip modules or single chip packages. For example, like a BGA, where you are going to use a flip chip. You will require to have an organic substrate, after which both the die and the organic substrate are encapsulated. So, you will use micro via organic substrates. The term micro via basically means, as the name indicates smaller dimensions of via structures, which connects one conductive layer to the other. When you say micro via, here the order is 100 micron or less. Today's technology allows us to go up to 50 microns. So, people are using processes like sequential buildup circuits for the single chip packages to allow routing patterns to be distributed over large number of layers to eliminate heat buildup. Typically, you can start with a two- layer core, but six to eight layers are very common today. You really do not have to go above eight- layer material.

So, typically, if you want to use a eight- layer board, you can use a 3,2,3 configuration. We will talk about buildup layers, when we come to PWB technologies. If you look at this figure here, (Refer Slide Time: 41:14) in this particular slide, you will see that there are number of layers of conductors, typically representing PWB structures. These are built on organic substrates and this is a via, which connects two metallic layers. This is also a via, but this could be a micro via because it is built in a sequentially built up pattern methodology. Whereas, this can be through a hole structure and so you have

micro via's and normal via's in a four- layer core in this case. Therefore, these kinds of structures are used, when you are going to work with flip chip because the number of IO's are going to be large. You really need to define escape routing patterns and so you can create various patterns in micro via designs and the lines and spacing for conductors. In these kind of structures, it has to be smaller around 35 microns or even 1 mil 25 micron.

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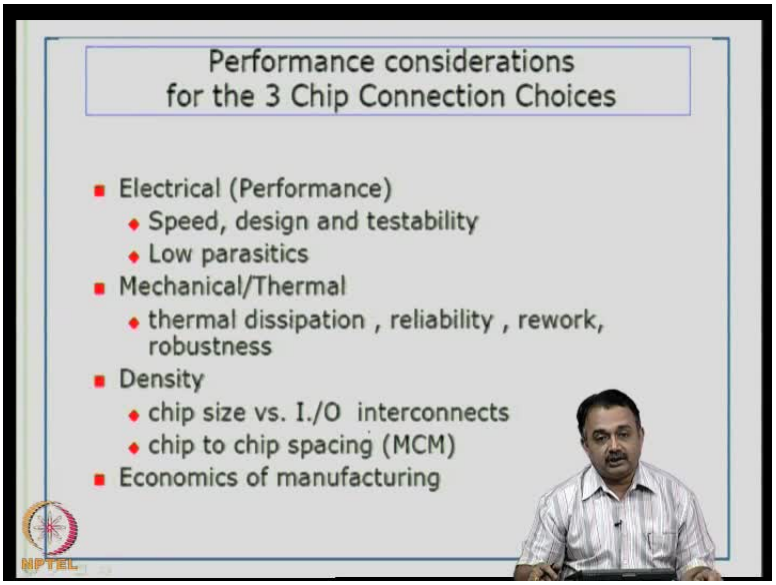

So, we have seen all the chip connection choices. What are the performance considerations? One is electrical- speed, design and testability, low parasitics. So, for the choice of going in for a flip chip or a wire bond or a TAB, you have to look at these parameters to design which one you really need for your custom built package. Mechanical and thermal issues are very important. Thermal dissipation, thermomechanical reliability, reworking and robustness; density and that is- chip size versus number of IO's, chip to chip spacing. As in the case of a multi chip module, where you will have an array of flip chip interconnected. Finally, the very important is economics of manufacturing because it really depends on what volume you want to work with.

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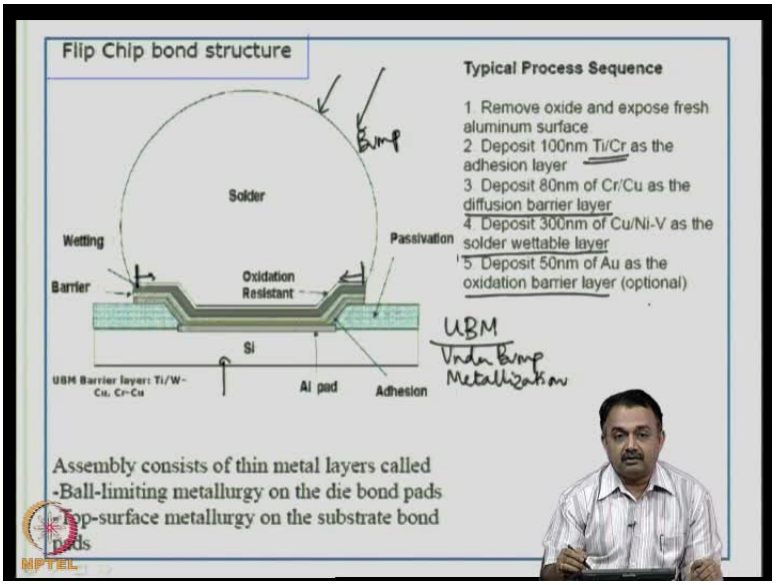

Now, the flip chip bond structure is very important. You need to know about it because I briefly mentioned that every flip chip has got a UBM- Under Bump Metallization. Why do you require a UBM? Before that, we will see what a U B M structure is? This is a cross section and you can see this is typically a bump structure. You can see here, (Refer Slide Time: 43:59) this is the silicon that comes from the wafer, where you have finished all the interconnections. These are the termination areas and so, there is a passivation done. This is the aluminum conductor, there is an adhesive pad and then there is a barrier layer followed by a wetting layer, an oxide resistant layer and finally, comes the solder material that you see here. This is the bump material solder, it can be of different types. It can be high lead solder. Today, we are working with lead free and so it can be tin based solder material and this is what the cross section represents in the flip chip bond, which gets attached to the organic substrate.

So, in some sense, this area that you see here, limits the size of the solder ball. So, your UBM does some kind of a ball limiting metallurgy on the die bond pads. Otherwise, it will attach more solder than the required. This also defines the exact size of the solder bump from adjacent pad to the other. Otherwise, in a flip chip, you will get unequal sizes of bumps. So, to avoid that UBM, it is very essential because it really defines the volume of solder that will get attached to the outer surface of the UBM buildup. Top surface metallurgy on the substrate bond pads is very important to define this. You remove the

oxide from the silicon wafer and so you can do this at the wafer level. So, that is why it is known as wafer bumping process. Instead of doing it individually, once the wafer is complete and these dies are realized, you can do bumping for all the dies and then isolate them or dice them to get the bumped wafers.

Now, you remove the oxide and expose fresh aluminum surface; the conductor. Deposit the addition layer, titanium or chromium or a combination. The thicknesses are given here, then you start using a barrier layer because you do not want inter-metallics to play a major role. If such a thing happens, then during the working or operation of the flip chip the solder can get diffused into the other materials, if there is no barrier layer. New inter-metallics can cause solder joint fatigue and other metallurgical problems, which can give reliability issues in terms of low reliability and so on. So, for the bumps to have long shelf life and high reliability, both in terms of thermal electrical and mechanical properties. You start depositing a solder wettable layer, typically copper, nickel, vanadium. Finally, a oxidation barrier layer of gold and then onto which you attach the solder bump.

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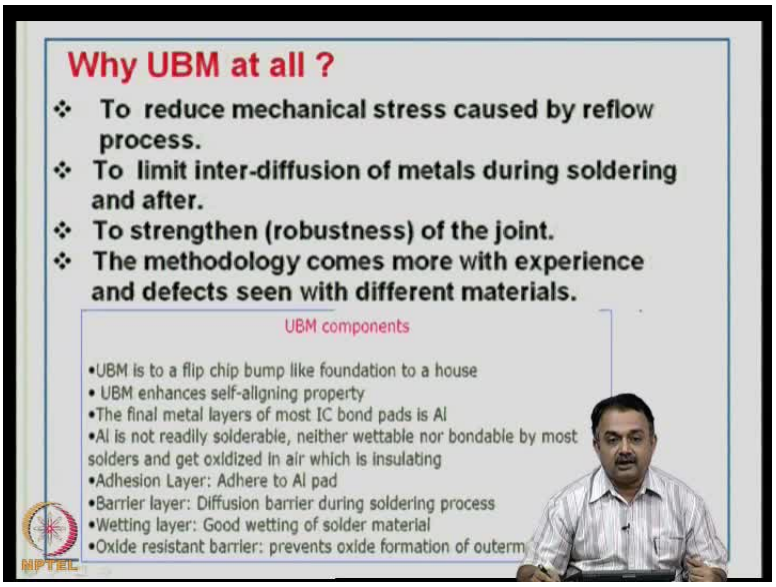

Why UBM at all? It will reduce the mechanical stress caused by reflow process to limit inter-diffusion of materials or metals during the soldering process and after. Then to

strengthen the robustness, to strengthen the joint that has been formed and so, increase the robustness. The methodology comes more with experience and defects seen with different materials. So, you have to be very careful in choosing the right combination of the UBM materials. So, UBM is like foundation to a house. For a flip chip, UBM is like a foundation to a house. UBM enhances the self aligning property and so this is one of the reasons, why you are able to pull back the die back to its original position during reflow because the UBM takes care of the attachment of the solder and the surface tension property. The final metal layers of most IC bond pads is aluminum. Aluminum is not readily solderable or neither wettable nor bondable by most solder. Therefore, it gets oxidized in air, which is insulating and therefore we add all these addition layer. The barrier layer, the wetting layer and finally, an oxide resistant barrier and then comes your solder coating.

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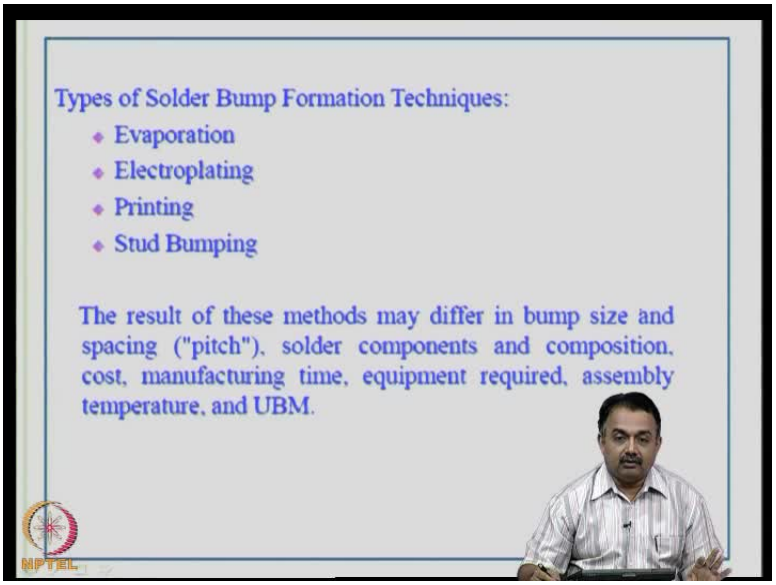

So, the methods to realize the solder bump in these flip chips will be evaporation techniques; typically chemical vapor deposition or evaporation methods. You are familiar that electroplating mechanism and stencil printing mechanism is now available today, where you print these solder paste material and then reflow. During reflow, you can see the bump formation without any solder bridging because of surface tension

property of the solder. You can simply attach a stud and this will be different from the normal bump. So, that is why it is called a stud bump. The results of these methods may differ in bump size and spacing or the pitch. So, you have to carefully select, which bump formation technology you require depending on the pitch and the material that you are using.

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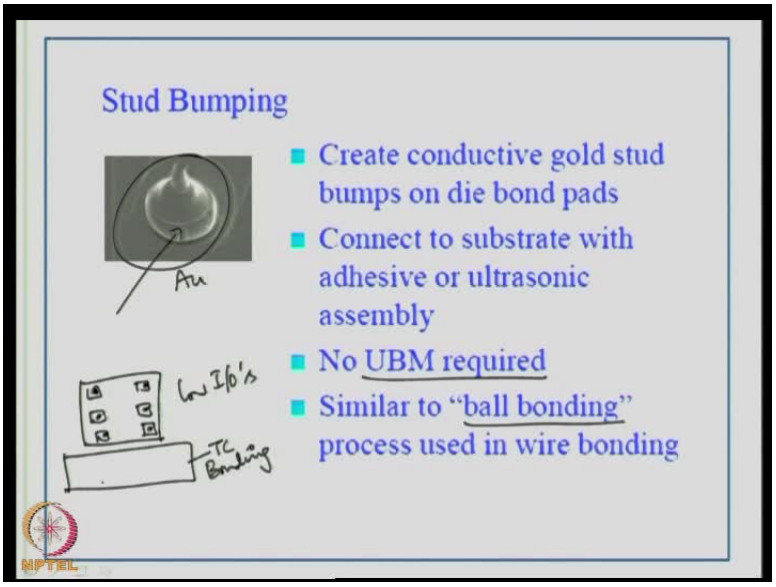

What is a stud bump? Stud bump is different from a normal flip chip bump, where you simply dispense off a gold stud like a ball bonding process that you see here. A spot of gold material is now dispensed on the bond pad and then it is cut off simply. You can imagine a typical ball bonding process to create a stud. You are not going ahead with the loop, but you are simply cutting off the gold material after the stud has been formed. So, you can create conductive gold stud bumps on die bond pads of the die and connect it to a substrate with conductive adhesive or an ultrasonic assembly. So, no UBM is required, if you are going to use stud bumping and this is similar to ball bonding that is used in wire bonding process.

So, if you have formed or manufactured a die, which is low IO's and if you do not want to do stud. If you do not want to do flip chip bumping, you can do it. Let us say, six bond pads on the die, you do not want to do a flip chip normal bumping. You can create the

stud bump, but still you can flip it over onto the substrate. Use a thermocompression bonding by using a conductive adhesive. So, this is a very quick process that you can do in your lab and this is typically for low volumes. You can use the same structure of the flip chip die minus the bump and that is very good for prototyping.

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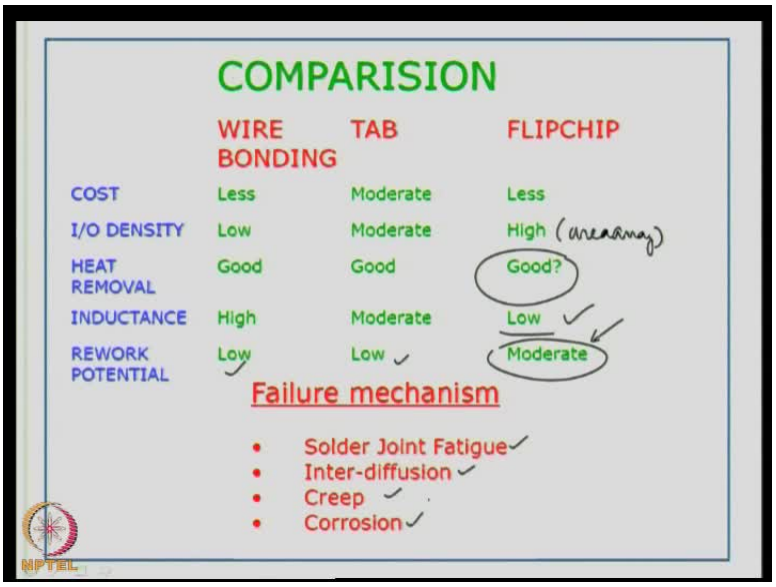

Finally, a comparison of the three processes: wire bonding, TAB and flip chip. The cost for wire bonding is less. TAB is moderate and flip chip is currently less because, if you are going for flip chip, you are looking at high volumes. If you have invested in a flip chip bond kind of an equipment for large volumes, typically your cost comes down. The IO pin density is low in wire bonding, very high in flip chip because this is area array. In TAB, it is moderate. Heat removal is good in wire bonding and TAB. As we have discussed in today's lecture, is it really good in flip chip? Yes, because, if you know the technique of using thermal spreaders and better heat sinks or underfill material then there is no problem with using a flip chip material.

Inductance is low and that is why we want to use flip chip. Rework potential today is very moderate for flip chip, whereas for these, you can do a rework. In this case, you will probably destroy the flip chip, if you are trying to remove it, but if it is a flip chip with a BGA assembly, where you have the BGA solder balls. Then you can rework on the BGA

solder balls rather than really working on the flip chip itself. The failure mechanisms typically are older joint fatigue inter-diffusion creep, corrosion and that is normally present with all types of first level interconnection choices.

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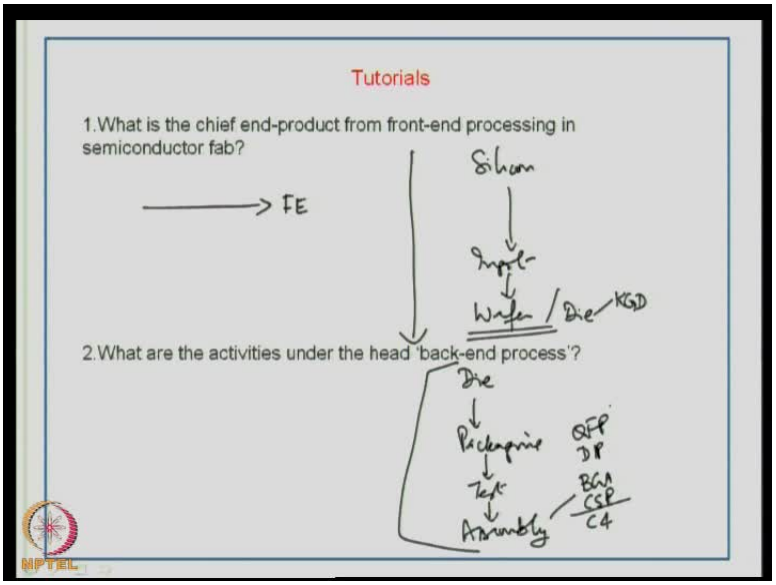

So, this actually completes the chapter 2 on TAB, wire bonding and flip chip. Now, I will take you through some tutorial. This can be discussed in this class or you can send your feedback through an email. As you are going through the tutorials, this is basically some simple questions that can be easily addressed, if you have followed the last five lectures on module 2.

What is the chief end product from front end processing in semiconductor fab? So, here you have to look at the slides pertaining to the front end process, where you are starting from a silicon and ending with a wafer. So, you got a Ingot and then finally a wafer, which is a high purity wafer. Finally, a die; a known good die, typically will be the end product or the final product from the front end processing. So, there are lot of process to be listed in this. So, you have to go through the entire sequence.

The next one is- what are the activities under the head back end process? So, here the starting point is the die and then you do a packaging. You do test and then assembly. So,

this is the sequence for back end process. It starts with a known good die and ends with an assembly. So, finally, it will end up as a BGA or a CSP or a bare die like a C4 or a DIP package or a QFP package and so on. So, I think you must be aware of this.

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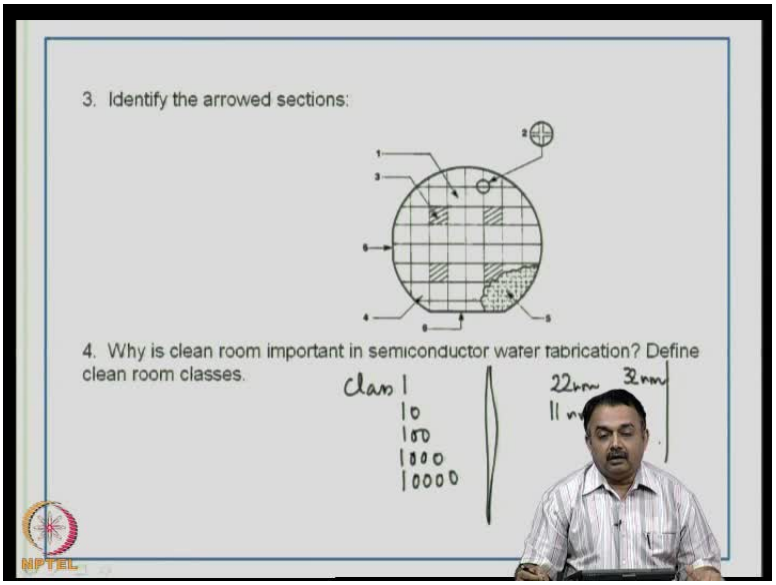

So, this is-identify the arrowed sections of the wafer. I think you can look back at this slide and identify the arrowed sections. So, you can take it as a homework problem and identify all these arrowed segments of a wafer.

Why is clean room important in semiconductor wafer fabrication? Define clean room and try to define, what is class 1, class 10, class 100, class 1000 and class 10000? So, I want you to recollect and reproduce the dimensions of the particle that can be allowed in a clean room for these classes. It is needless to say clean room is very important because we are talking about line widths or technologies today at around 22 nanometers. We are going into 11 nanometers. Currently, we are working at 32 nanometer technology. Therefore, eliminating dust is very important. You can go through some other questions and easily answer here.

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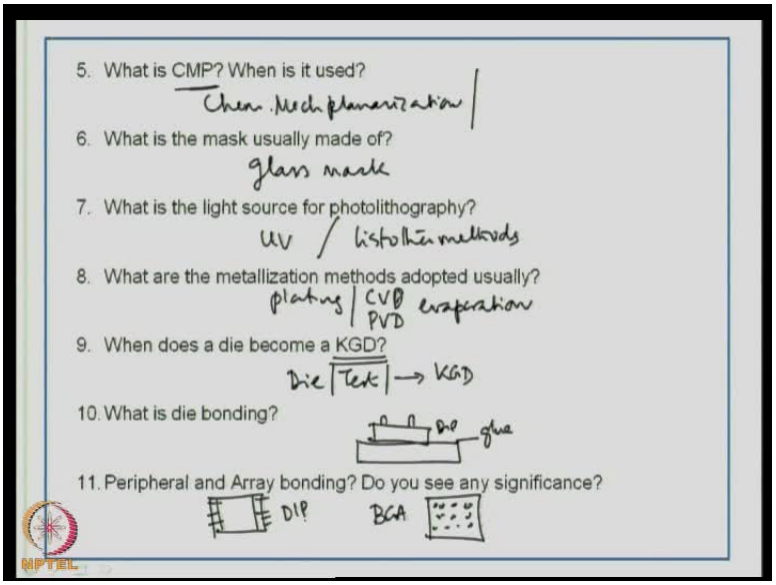

What is CMP? When is it used? So, CMP is Chemical Mechanical Planarization process. Chemical Mechanical Planarization process is used as a final process to remove excess conductive material that has been plated and for example, after electroplating. What is the mask usually made of? It is usually made out of glass. So, in semiconductor fabrication, we use glass mask. Light source for photolithography, typically is UV and you must also be able to list other methods that are coming up today in place of UV. Metallization methods are adopted usually. Typically, one is plating and the others are CVD, PVD evaporation techniques and so on. It can deposit very small thicknesses of conductor or insulators onto the wafer surface. So, when does a die become a KGD? This is known good die. So, after you singulate the die, you test it electrically and then it becomes a known good die. What is die bonding? Attaching a die; this is the face up configuration to a substrate using a glue and this is die bonding.

Peripheral and array bonding- do you see any significance? So, this I have discussed a lot. So, basically in a DIP package, you see peripheral bonding. In a BGA, you will see area array bonding. So, you must be able to explain, why the density is higher in a BGA compared to a DIP package. So, in some sense, you will be able to define peripheral and array bonding highlights.

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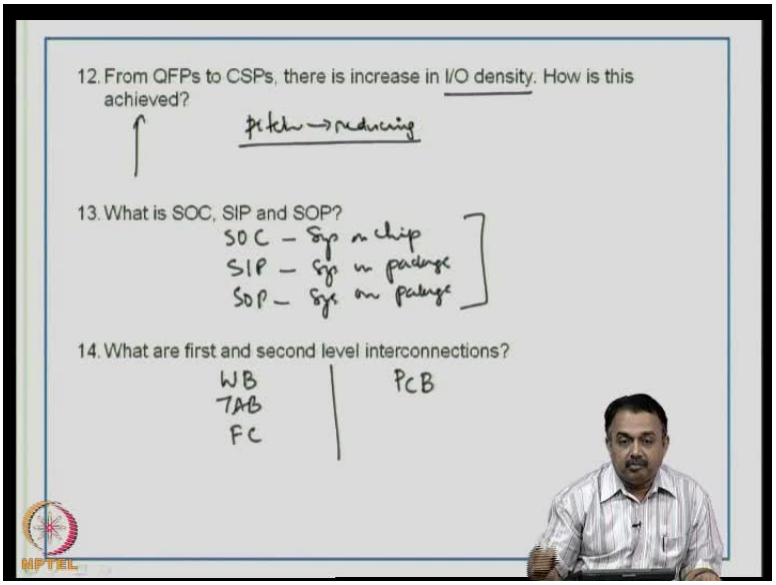

From QFP's to CSP's, that is, from quad flat packs to chip size packages, there is increase in IO density. How is this achieved? Because we are playing with pitch, we are reducing the pitch and reducing the dimensions of the attachment in the CSP. It is a solder ball. In a QFP, it is a lead frame. So, because of decrease in pitch, we are able to decrease the package size and the overall format is reduced. So, I think you can elaborate more on this question.

You must be able to answer, what is an SOC system on chip, SIP system in package and SOP system on package? All three are different. I think you should be able to come out with explicit reasons or definition of these.

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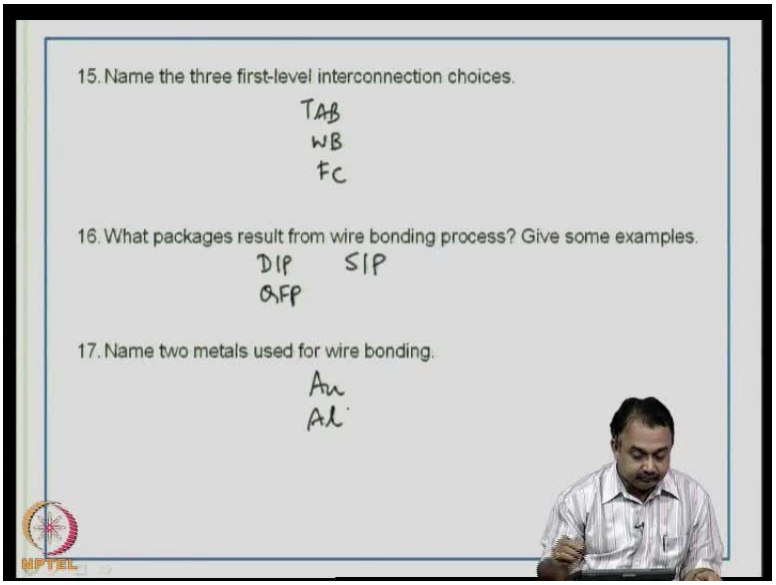

We have seen in today's class about first level interconnections. Wire bond, TAB and flip chip and the second level interconnections are typically taking place at the PCB or the PWB stage. So, the three first level interconnection choices are TAB, wire bond and flip chip. What packages result from wire bonding process? Give some examples, it will be DIP package or a QFP package or a SIP package- Single Inline Package and so on.

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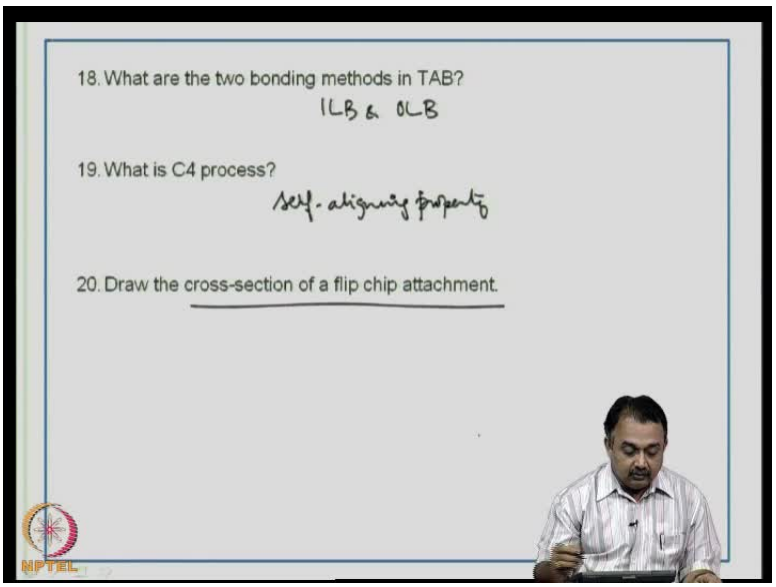

Name two metals used for wire bonding: gold, aluminum. What are the two bonding methods in TAB? We have seen inner lead bonding and outer lead bonding. C 4 process is basically a self-aligning process and we have seen in today's class about direct chip attachment onto a substrate. So, the self-aligning property is basically known as C4 and this you can take it as a homework problem; cross-section of a flip chip attachment that goes for a BGA.

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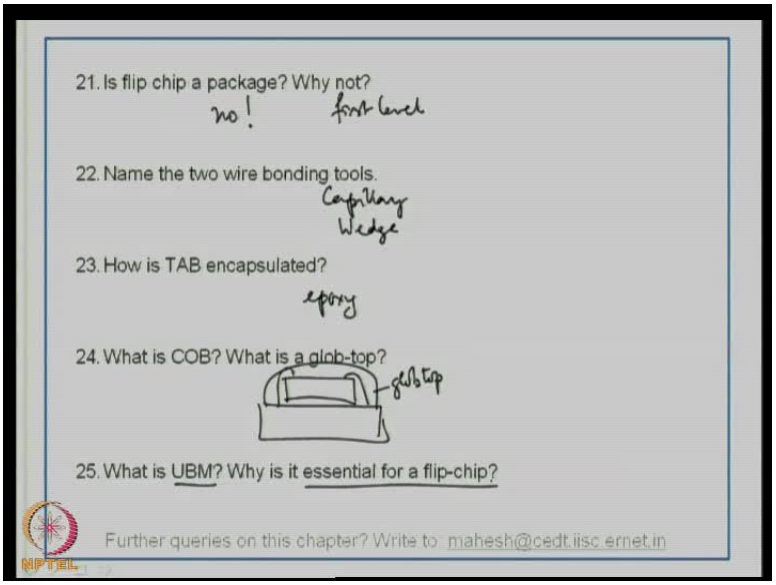

So, this will cover some of the major points that we have discussed today. Finally, is flip chip a package? Flip chip is not a package because it is only a first level interconnection choice. Two wire bonding tools: capillary and wedge are the two tools used for wire bonding TAB is encapsulated by epoxy resin chip on board. If you have a chip mounted on an organic substrate. Do a wire bonding and then apply glob top. So, this is the cross-section for a glob top. UBM is under bump metallization and we have seen today in the class that the essential reasons for using a UBM for a flip chip. So, these are some of the questions that you need to refresh yourself and this completes the module two of this chapter