VLSI Physical Design with Timing Analysis

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Week - 06

Lecture 31

Min-cut placement

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about Min-cut placement algorithms. So, the content of this lecture includes basically first of all we will discuss about the routing condition, then we will discuss the Min-cut placement algorithm. So, what is the Min-cut placement algorithm? There are two popular Min-cut placement algorithm which is extensively used. One is the Min-cut placement algorithm using the Kernighan-Lin algorithm and the second one is basically the FM algorithm. So, what is the routing condition? This plays a very vital role because whenever you do any kind of VLSI chip design or something we cannot route our design.

So, we should understand why it is not routable. So, here we will discuss why a net is not routable, reason behind it. So, before going to that one we will discuss about two things. One is called the channel CH stands for channel and the SB stands for the switch box. So, whenever we have only path from basically two sides, path from two sides, if you can see here that the net can go this direction or net can move in this direction, but vertical nets cannot be routed. So, this is called your CH or the channel. But in case of switch box, you have routing possible in this direction as well as this direction, vertical direction as well as in the horizontal direction. So, this is called switch box. So, what is basically happening is that we have a ratio of the demand of the routing track to the supply available in the routing track.

So, we have a requirement of how many signal I can route and there is what is the availability of the routing tracks. So, based on that we can define a routing condition factor. So, this routing condition is estimated by number of nets that pass through a boundary of individual routing region. Whenever I have this switch box or the channel, these are the routing regions. So, here, how many nets can be routed? So, that is fixed. And so once that is fixed, then we can utilize that resources. We can utilize that resources. So, formally the local word density, the fie of P of E of an edge E, basically we

have edge E between two neighboring grids is denoted by this is fie of P is equals to eta of P of E by sigma of P of E. What is eta of P of E is the estimated number of nets that cross E. Now sigma of E is basically maximum number of nets that can cross. So, that maximum number of net is basically provided by the resource available to us and estimated is what we are doing the routing. So, the wire density of a placement is fie of P is basically the maximum E belongs to E for all edges. I am finding fie of P of E, then what is the maximum of that one? And this E is basically set of all edges. And I am finding, so this small, this is basically the lower case fie of P of E is for each edges and the upper case fie, so it is for each edge, upper case fie is for maximum of upper case fie of P is maximum of all the edges. So, we are worried about all the maximum value not worried about individual edges.

So, if my fie of P is less than 1, then design there is no issue, your design is fully routed. If fie of P is greater than 1 means we have more demand, we have less supply, more requirement of routing, but there is less resource available. In that case, your design is not routable. What you have to do? We need to change the nets, detour means change the nets through the less congested area. Let us say if I go in a car, my car is in a congested area, I need to go in a less congested area such that I can reach the destination. The same method is applicable here. If some path is congested, I need to change my direction to a less congested edges such that I can route that net. So, the congestion driven placement seeks to minimize the fie of P. Whenever I have basically congestion driven placement, I am trying to minimize the fie of P such that all my nets should be routable. So, basically this is the main concept of routing congestion.

So, let us take an example to understand this concept. So, we have a wire density, we need to find out the wire density of a placement. So, these are the parameters given to us number of nets, the number of vertical cut line, horizontal cut line, then sigma of E of 3 for all local cut lines and I have all the nets N1, N2 and N3 is given to me. Now I need to find out my wire density fie of P and determine whether all the nets are routable or not. So, first of all I will find out eta of P of H1. So, eta of P of H1 is basically this one. So, this is 1 here. So, in this cut I have 1 here. So, this one is 1. Now basically eta of V1, eta of V1 is this one. So, this is also 1 here because I have only 1 cut. Now I will take one more example let us say V6. Whenever I have V6, this is my V6. So, there is no cut. So, this is 0. Similarly, you can calculate for all other cuts. Now what is the maximum eta of E? Maximum eta of E is basically if I can see here, this is the thing and this is the thing. These two are the maximum eta. So, the maximum eta of E is 2. Then I have the sigma.

Basically I need to find out the fie of P. The fie of P is basically eta of P of E by sigma of P of E which is basically 2 and the number of routing track available is 3. So, it is 2 by 3 and your fie of P is less than 1. 2 by 3 is less than 1. Hence the P is the placement is routable. Hence the placement is routable. So, we will discuss about some placement algorithms. So, Min-cut is one of the popular placement algorithms. So, what is the input

to the Min-cut placement algorithm is the netlist and the layout region. So, what it does is that it divides the overall layout region into smaller and sub netlist and some regions. So, we are dividing the overall design into smaller designs. So, the process is carried out till each sub circuit. What is happening in this placement versus the partitioning? Whenever we are doing partitioning, we do the partition and we have created two different partitions. But in this case we repeated that partitioning till each sub circuit will occupy a space in the layout. Means each single gate will get a location in the layout, unique location in the layout. So, each logic gate will find out its unique place in the layout. So, the Min-cut placement algorithm finds the unique place for each logic gate in the design. So, this is the main theme of this Min-cut placement algorithm. So, there are basically it all depends upon heuristic. So, each CUT heuristically minimizes the number of CUT nets.

So, there are two popular algorithms there KL and FM, but we discussed in case of partitioning the same algorithm can be exploited to do the mean placement of the logic gates. So, we will discuss the KL then the FM algorithm. So, here what is this Min-cut placement algorithm? So, what are the inputs to the Min-cut placement algorithm? We have a netlist and we have a layout area. We have netlist is given to us, we have a layout area given to us. So, what basically the minimum cell minimum number of cells for a region is cell underscore mean so that is also given to us. So, what is the final output? These are the inputs and final output is my placement of all the logic gates in that area. So, what is happening here is that initially there is nothing is there. So, the p is 5. Then what we are doing? We have a assigned netlist and the layout is given to that one. So, we are assigned the netlist to a layout area.

So, we created a variable regions here. We operate this flow till this one runs for one time. Till this one is the run for one time. After this there is a while loop which will be repeated. So, when it will stop? When there is no element in the regions. So, we have some element in the regions then we are basically processing that one. So, first we will take this is regions. Remember S is there. This S is there. Then we take one element from that regions that is called region. Now what we are doing? Once I have taken that one I want to remove that first element from the set. So, I am removing that region the first element from the regions because I want to process that. Now what we are doing is that we will do the bisection. We basically region contains more than cell underscore mean cell. So, if the region which is the element we found out if it is contained more than cell underscore mean cell a minimum cell what is given in the algorithm then what you have to do? We bisect the region into two part that is SR1, SR2 two part we divide that into two part. Then what we are doing? Now we are adding that one SR1 to the region the original set. Now we are adding SR1 to the original set. Now which is the first element? SR1 is the first element. So, now in the region set I have two elements. The first element is SR1 after executing this statement. After executing the second statement I have SR2.

Now what is happening is that now we have sub blocks. These are sub blocks because I have already done the bisection on that one original region. These are having less elements inside that. Then what we are going we will repeat this thing because we will repeat these things till the region is empty.

Then we are repeating this one till it will reach the minimum cell area, minimum cell what is defined in the algorithm then we will place that one. Place and place the region then what we are doing? We are adding the region to the P. So, in this case what we have to do is that once it SR1 is processed then this placement of the SR1 and each of these things will be done then we will go to SR2 block and do the same thing again. So, this is the mean cut placement algorithm. But in case of a partitioning algorithm we do this bisection for one time. So, basically here we have alternately applying the cut line directions and repeating the cut line directions. So, the algorithm divides the layout by switching between the set of vertical and horizontal cut lines. Basically it switches between horizontal and vertical cut line. So, once it is do it for a vertical cut in the next time it will go for a horizontal cut. Then finally once all the cells are placed then it will terminate.

So, the first time let us say if it is horizontal next time vertical then again horizontal then vertical like that it will repeat. It is very useful for standard cell based design with high wire density in the center of the layout region. It is very useful for the standard cell based design methodology. So, this is the basically actual layout area. First we do a horizontal cut line. So, this is the one horizontal cut line. Now we have two vertical cut lines from here to here is one and here to here is the second one. Now we have four horizontal cuts. This is one horizontal cut from here to here. This is two horizontal cut from here to here. This is three horizontal cut from here to here. This is the four horizontal cut from here to here. So, this process will repeat it. So, we are basically repeating the cut line directions. The layout is basically completely divided or divided using only the horizontal and vertical cut line until each column or a row is the width and height of a standard cell. This is very important. So, finally what we will do? One of the column or a row will have either one standard cell width and height of the fit to the width and height of the standard cell. So, the layout is divided using the orthogonal set of the cut lines. The layout is divided repeatedly into set of cut lines actually which is orthogonal and it often results in a greater wire length because aspect ratio of the sub regions can vary from one. Now we are discussing how we can do mean cut placement using our KL algorithm. So, the KL is a popular algorithm. So, we will discuss how we can do the placement using the KL algorithm. So, we have six gates are there. Our layout area is 2 x 4 and initial cut is this. This is our initial cut. Since I have basically 4 x 2 placement area is available. So, I have basically eight elements need to be placed. However we have basically six gates are there in the circuit. So, what we are doing is that to find a placement with minimum wire length using the alternate cut line direction and using the KL algorithm. So, what we are

doing here is that we are converting the basically our netlist into a graph. So, this is the basically node corresponds to this one the logic gate one. Similarly this is corresponding to node corresponding to this gate.

So, now this is the first cut. And if you can see here whatever I told you have 2 x 4, 8 placement origin is available. But we have 6 logic gates are there. So, we need to add basically two extra nodes to the graph. These two extra nodes are added. And basically there is no connection but these two extra nodes are added to the graph. Now what we are doing we are finding the if I have this cut one then what is the gain. So, left hand side this is the left hand side this is the right hand side left hand side is basically having ABC because this 1, 2, 3 corresponds to ABC and basically this is 1, 2, 3 and DEF is basically 4, 5 and 6. So, now what I am finding is your D of B whatever I discuss in partitioning D of B is basically EC of B minus E of NC of B. What it is doing is that how many nets are cut by the cut line minus how many nets are not cut by the cut line. Let us say I have this cut line is there. So, the node 1 let us consider the node 1. How many cut by the cut line is 1. This is 1 and what is not cut by the cut line there is no S which is not cut by the cut line.

So, D of 1 is basically 1. D of 1 is basically 1. So, similarly you can do it for other but then there is a gain formula what we again discuss in the K-L algorithm. Delta G of A, B is basically D of A plus D of B minus 2 CA, A, B. So, basically this formula is used to find delta G of 1 which is 2. So, the 2 which is having the highest gain is basically node 3 and 4. So, what we can do here is ideally we need to find for all combination of delta G but because of time we are just going showing it for 1 delta G and which is giving you the maximum gain. So, then we can swap node 3 and 4. So, 3 will go to this partition and 4 will come to this partition. So, now if I do the swap then my new cut line will be look like this 1, 4, 2 in the left hand side and 3, 5, 6 in the right hand side. So, again we are not going to the full cut line. Now we are considering in the basically left hand side only or right hand side only. So, here what we are doing the cut 2L because it is a left hand side and the second cut. So, if I do that cut then I have a top, top is having 1, 4, bottom is having 2, 0 and similarly I have cut 2R. So, here top is having 3, 5 and the bottom is having 6, 0. Now what we are doing here is that here we are again finding the for d of 1, d of 2, d of 4, d of 0 like we did for the KL algorithm in the partitioning algorithm. So, here then we found out no delta G is greater than 0 hence there is no swapping of the nodes possible here. So, we can repeat the same thing no swapping for the other case also cut 2 there is no swapping possible because no gain in delta G, no delta G is greater than 0 here.

Then we will repeat for the same procedure for cut 3TL, cut 3TR, cut 3BL, cut 3BR. So, T stands for top I can write here T stands for top and B stands for bottom, L stands for left and R stands for right. So, these notations are used to individually cut each of the

subunits such that each basically location will assign one block, each region has one node, each region has one root. So, after it all the node each gate, logic gate is assigned one node then you can terminate the algorithm. So, this is the final placement and so this is in the graphical domain and this is the actual placement of the algorithm.

So, this is using the min-cut placement using the KL algorithm. So, now we will discuss the min-cut placement algorithm using the FM algorithm. So, what is given here the circuits with gates A to G then the ratio factor then the gates area of each of the gates and the initial partition then the fifth one of course the layout area. So, here what is the target is to how we can place all the gates in the 2 x 4 layout. So, we need to find a placement with minimum wire length such that we can use the two concept here one is the alternate cut line direction. First we will do a horizontal cut then we will do a vertical cut, again we will do the horizontal cut then we will do a vertical cut like that and then we will exploit the FM algorithm here. So, this is the layout area. So, first vertical cut is basically this cut one. This cut one you have L equal to ABC and means left hand side is ABC and right hand side is DEFG.

Then what you have to do we need to find out a balance criteria. The balance criteria is basically area of A should be less than equals to the ratio factor area of A or partition A let us say the total area is denoted by AT. So, ratio factor multiplied by AT minus the maximum size gate logic gate max of let us say the gate logic gate AG should be less than equals to so R multiplied by AT plus max of AG. So, the max of AG in this case you can see which is the max of AG here NAND and NOR gate which is having the maximum 2. So, here max of AG equals to 2 and total area AT is 11 and ratio factor R so this is given this is one parameter this is second parameter and the third parameter is your ratio factor R which is 0.5.

So, after we do this we have area of the partition is bounded by 3.5 and 7.5 area of the partition should be bounded by this much. Now we will find out the in case of FM algorithm we need to find out our gain. So, for finding the gain actually we have a formula is that delta G of a node is basically FS of C minus P of C. So, this FS of C is what FS of C is basically is the number of nets is a number of nets connected to C but not connected to any other node any other cells within C's partition.

So, this FS of C then TE of C is basically uncut net connected to C. So, for example if you can see here for let us say the node D. Node D if I go by node D basically node D is connected to this cut by the cut line is 1. So, the FS of C is 1 for node D and TE of D is basically 1 because this net is not cut by the cut line uncut nets. So, this TE of D is 1. So, the gain of moving the D to the other side is 0 because 1 is if I take the D to the other part then my gain will be 0 because it has one cut net that will be reduced and another cut net will be created. So, in this method we will calculate all the delta G's then after I found the delta G then I have to see which is having maximum gain A, B, C and G is having the

maximum gain. Then I need to check my balance criteria. In this first case A the balance criteria is violated. So, I cannot do the moment of A in case of B the balance criteria is violated so B cannot be moved to the other partition. In case of C the balance criteria is violated so it cannot be moved to the A's partition. Then in case of G the balance criteria is maintained because the 6 is basically the area of A is become 6 which is bounded by 3.5 and 7.5 and it is satisfying the balance criteria and G can be moved to the other partition.

So, G can be moved to the other partition. Now the new partition will look like this. Now the new partition will look like this. Earlier I have 3 cuts now it is becomes 2 cuts. Earlier I have 3 cuts 1, 2, 3 now I have only 2 cuts. This is one cut and this is the second cut. This is the one cut and this is the second cut. Hence the number of cut is reduced by 1. Similarly I can do for the second iteration. So, this is the gain which is having the highest gain then the balance criteria is satisfied here for the node A. So, this is the new partition. So, this is my new partition. So, I have number of cut earlier is basically if I can see here earlier this is 1 and 2. Now after doing the partition I have only 1 cut. So, number of cut is reduced by moving the A to the other partition I have number of cut becomes 1. So, this process will be repeated till all the gates will be assigned to each of the locations and this is the final placement using the FM algorithm. So, in this lecture we discussed about the routing condition first then we discuss about two mean cut placement algorithm such as KL and FM algorithm which is very useful to find the location of the logic gates or the standard cells in the final placement.

Thank you for your attention. Thank you.