**VLSI Physical Design with Timing Analysis**

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**Week 03**

**Lecture 17**

**STA for Combinational Circuits – II**

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about the static timing analysis for combinational circuits. So, in this lecture, we will include how we can find a critical path of any circuit with an example. So, in the last class, we discussed about the arrival time and the required time. So, in today's class, we will discuss this one in detail with an example. So, if I write down the formulas for the inverting types of gate, so if I have any kind of inverting type gate, so I have two things, one is input arrival time and output arrival time. So, what is the first one I need to calculate is the output arrival time or output rise arrival time is basically max of input fall arrival time plus rise delay. Similarly, I have output fall arrival time is basically max of input rise arrival time plus fall delay. Then this is for the output arrival time, this is first and the second is the output arrival time. Then if I know the output arrival time, then how I can find the input arrival time.

So, in this case, I have to find out the input rise arrival time. So, since I am finding the slack, so here I also can write this as input rise required time. So, input rise required time is basically minimum of output fall required time minus fall delay. Then the fourth one input fall arrival time or I can write input fall required time because the required time is needed for my slack calculation. So, I need to do minimum of output rise arrival time minus rise delay. So, these are the four formula I will use throughout my calculations. So, we will take an example and discuss how this is happening. So, three gates, it is easy to explain. So, I took a very small example. So, these are the rise and fall delay. So, this is my node a, node b, this is node d, this is node e, this is node f. So, each of the nodes I need to find the first arrival time, and this is the nodes basically input c which is going to input of the basically my NOR gate. So, what is my task here? What is the question here? If this gate, if this netlist or the circuit is given to me and what are the things given to me here? The given is the rise delay by fall delay for each gate it is given to me. Then second thing what is given to me? My input node arrival time is given. So, what are the primary

inputs here? a, b, c. So, the arrival time both rise and fall, let us say basically the rise and fall arrival time of node a, rise, fall arrival time for the node a is basically 0, 0, 0 by 0. So, that is the rise and fall arrival time for node b is also 0, 0 and arrival time for the node c is also 0, 0 that is given to me. And one more thing is given to me. What is that? That is called the required time. The required time at node f is 5 by 11.

So these are the things given to me. What I need to find it out? I need to find it out basically the arrival time required arrival time at each node. I need to find the required time at each nodes each node and find the this is the first point find the find the slack at each node. Then the third point is find the critical path critical path path in the circuit in the circuit. Correct? So, this is the thing. So now I will basically solve some part here and some part in the second slide. So here if I take for the node a, I will start with the node a. So, node a I have the arrival time is given to me. So, whenever I am writing arrival time the basically it is not a division. It is basically top one is saying the rise arrival time, and the bottom one is telling the fall arrival time.

So, this is your rise arrival time which is given in the fall arrival time. So, this is given. Now I cannot find the required time right now or slack I cannot find. So, I will give some space there. So, for the node b, I have basically arrival time same arrival time. So this is 0 by node c also the same thing. So, I will take to the next slide. Now I have the same circuit. So now I have to do it for the node c here. Node c arrival time rise, and fall is 0 by 0. Then the node d arrival time is basically if I take the node d arrival time, so it will be basically 2 by 3. Why it is 2 by 3? I will write the reason for here for the reason here. Basically, the input arrival time, input fall arrival time is 0, input rise arrival time is 0, then the rise delay, delay is 2 and the fall delay is 3. So, these two will be added up to give me this one. These two will be added up to give me this one.

So now I have this node basically node d then node e. I have node e arrival time; I need to find it out. So, the node e arrival time is basically I need to find it out. So, I will write the reason here. So, the input arrival time, input fall arrival time equals to node e. The input fall arrival time is 3 and input rise arrival time is basically 2 and you have the rise delay equals to 4 and the fall delay equals to 3. This corresponds to basically this gate, NOR gate. Now this arrival time will be 3 plus 4 and 2 plus 3. So, 3 plus 4 is 7 by 5. So, this comes from here, this comes from here. Now I will do the next node. So, I have one more node is there, node f. I have one more node is there, node f. So, node f I have arrival time. So the arrival time here is the I have to do two things input arrival time fall which is 5, input arrival time rise equals to 7, then I have rise delay of the inverter, rise delay of inverter is 1, then the fall delay of inverter is basically 2.

So here if I do this addition, the arrival time at the node f is 5 plus 1, then 7 plus 2. This is basically 6 by 9. So, this is my arrival time. Now I have given the required time. So required time is basically 5 by 11. Then my slack here is basically required time minus

arrival time. So, I need to subtract my rise required time with the rise arrival time. So required time rise will be subtracted from arrival time rise. So, my rise required time fall will be subtracted from arrival time fall. So, it will be if I do the subtraction, this will be 5 minus 6 divided by 11 minus 9. It is basically -1 by 2. So now I have to go back. So, if I have to go back here. So now I need to find the required arrival time at node. So, I have to find the required arrival time here. The required arrival time at this point is basically I have two things here. One is called my output fall required time that is 11, output rise required time is basically 5. Then fall delay is 2 and the rise delay is 1. So now the required time in this case will be 11 minus 2 by 5 minus 1.

So, it will be basically 9 by 4. Then the slack in this case like I discussed in the previous example, slack will be required time minus arrival time at node e. So, this will be basically 9 minus 7 divided by 9 minus 7 for the rise. Then it will be 4 minus 5. So, it will be 2 by -1. This is my slack. Slack is basically 2 -1. So now I will go to the node d. Node d I need to find the required time. So required time at this point first I need to find what are the inputs for the required time. I will write down here then I can do that. So, you have the output fall required time. Output fall required time is 4 here. So basically, the output fall required time is this one, is basically this one and this will be for the rise. So basically, if I can write the output rise required time will be 9.

Now I have a fall delay. The fall delay will be which fall delay. So now already I have discussed about the inverter. Then it comes the NOR gate. So, the fall delay here, the fall delay is basically the NOR gate. So, this NOR gate fall delay will be basically 3.

Then the rise delay of the NOR gate is basically 4. So now my required time at node d is basically 4 minus 3, 9 minus 4. So, this will be basically 1 by 1 and 5. So now the slack I can find it out. The slack at this point I can write down the slack here.

So this is the slack I am writing. It will be basically node D will be -1 by 2. So, this is the slack at this point. Similarly, now I have to go for the node c. So, if I know the required time at node d and the required time at this point will be the same because both the inputs are connected to the same gate. So, I am writing in the same colour. So, this will be copied here. So, this will be 1 by 5. The required time is same, but the slack will be different because your arrival time is different. So, the required time is same. However, the slack at this point will be different. Slack will be your required time 1 minus 0 then 5 minus 0. So, it will be 1 by 5. Now I will go to the previous slide. So here I have two more points are there. So, for the node b, if I look into the node b the required time at this point, so I have four things, four parameters. One is called my output required time fall which is 5 then my fall delay. Fall delay is basically the delay of the fall delay of NAND gate which is equals to 3. Now output rise required time is basically 1 here then the rise delay of NAND gate. So, this is basically your 2. So, using this one I can find the required time. So required time will be the first row will give me my rise required time. So, 5 minus 3 by

1 minus 2. So, this will be 2 -1. Then I can find the slack here. The slack at this point will be 2 by -1. Similarly, that required time at this point is same as the required time here. This required time here is same as the required time here. So, the required time at this point will be again 2 by -1. So now if I have that one then slack at this point also will be 2 by -1. So here so now I need to draw the final diagram. So now I need to find the final circuit with all the slacks. So, I have basically this one. So here delays are 2 by 3, 4 by 3, 1 by 2. Then I have a, b. Now I have a. So, this is the d. This is c. This is e. This is f. Now I need to write down all the arrival time and slack. So, I am writing for a and b together because both have the same arrival time. Arrival time is 0 and the required time at this point is basically 2 by -1 and the slack here is 2 by -1. So, this is related to this a and b. Now for the basically d, c arrival time is basically 0 by 0 and the required time at this point is basically 1 by 5, and the slack is basically 1 by 5. This corresponds to node c.

Now for the d, so the d what is the arrival time. So, for the d is basically arrival time is basically 2 by 3. Then the required time at this point will be basically 1 by 5 and the slack at this point is basically 2 minus 1 by 2. So, this corresponds to node d. So, the node d I put it inside the same circle. Now basically if I go to node e, I have arrival time. So, arrival time at this point is basically 7 by 5 and the required time at this point is basically 9 by 4 and the slack is basically 2 by -1. Node e I put it in the same thing. So now for the f node. So, in this case for the f node, the arrival time is basically 6 by 9, required time is basically 5 by 11 and the slack is basically -1 by 2. So, this is my this one. So, the critical path is having the which is having the largest negative slack. So, my critical path in this design is basically if I write, so the f rising, e falling, then d rising, then either a or b both falling. So, if I can see here, this is negative here. So, this is negative, so minus rising. So, this is corresponds to this one, this -1 corresponds to E falling, then this -1 corresponds to d rising.

So, this is corresponds to d rising, then you have a b falling. So, this corresponds to a b falling. So, this is basically whenever I am finding the critical path, I need to trace the slack from the output or the primary output towards the primary input. So, the slack I need to see which is having the highest negative slack to find the critical path. So, whenever the slack is negative, then your circuit will fail in the actual design. We need to design or use another logic gate to satisfy that constraint such that my overall required time should be satisfied.

So, in this lecture, we discussed about how to find the arrival time and required time and finally the slack at each node of the circuit which is useful for finding the critical path of any bigger circuits. If you have a negative slack, then means that the circuit or the path is critical, we need to redesign the circuit to meet the required time given by the designer.

Thank you for your attention.