VLSI Physical Design with Timing Analysis

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Lecture 14

STA in Sequential Circuit with Clock Jitter

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about how my timing analysis of the sequential circuit will be impacted by clock jitter. So, clock jitter is one of the source of non-idealities, how it will impact my timing analysis. So, the content of this lecture includes what is clock jitter, then we will discuss about how to do maximum timing analysis or the setup check with clock jitter, then the minimum timing analysis or the hold check with clock jitter, then we will discuss about what are the sources of clock skew and clock jitter. So, this is very important, if you know the source then you can correct it. So, first of all what is clock jitter? So, jitter is basically a temporal phenomenon, the clock jitter is basically a temporal variation of clock age, clock arrival time. What is this clock arrival time? Temporal means with respect to time. So, the arrival time is the clock ideally let us say the clock arrives here, but it can arrive anytime between this to this. So, it has a band of time interval at which it can arrive. So, this is called jitter.

So, the arrival time of the clock will vary with time. So, basically the arrival time, what it says that is basically arrival time of the clock is will vary with time. So, in this case what is the impact? The second point here is that your clock period will increase or decrease, the clock period will increase or decrease with time. Let us say I have a band here also in between your signal can change, ideally let us say the time period is this one. So, ideally the time period is this one, but with jitter if I take a different color with jitter it can change, it can change to T clock plus 2 t jitter. So, this is plus or minus, this will be plus or minus it can vary. So, this is whatever I showed is the plus 1, whatever I showed is the plus 1, but it can vary to minus also. So, this is the maximum time period whatever I showed, and it has also a minimum time period here which is basically T clock minus 2 t jitters. Because of the jitter, my clock period can increase means that your T clock plus 2 t jitter, decrease means that T clock minus 2 t jitters. So, this will definitely impact our performance of our design. So, we need to consider the worst case. Then we have basically cycle to cycle jitter

is there, means that time varying deviation of the time period means whatever I told from one cycle to other cycle how much my clock single period will vary. So, time varying deviation this is basically time varying deviation of a single period. So, how we can model this? Because if it is there, we need to model it and use in our simulation. So, how I can model this actually? So, we can model is using zero mean random variable. It can be modeled using a zero mean random variable. So, basically it is not deterministic. So, we need to take the help of random variables to model it. So, unlike clock skew, which is more or less deterministic, here we can model this one using a zero mean random variable. The zero mean is that mean is basically across our arrival time of the clock signal around that we need to introduce a basically random variable whose mean of all the arrival times average of that one will be 0.

So, we will discuss about the timing analysis with jitter actually. So, maximum timing analysis with jitter actually. So, I have to consider two flip flops, one is launch and capture. So, the flip flop one this is flip flop two this is the combinational delay. So, this is D pin, this is Q pin, this is D pin, this is Q pin. Now, I have three delay parameters here one is clock to Q from here to here is basically t clock to Q maximum. Since we are doing max timing analysis this is t combinational maximum from here this edge till this edge and data should be stable before the setup time of the second flip flop t setup of the flip flop two. Now, because of the jitter what is happening I have to draw the timing waveform. Ideally, I have a timing edge like this. Now, because of the jitter it can arrive early, or it can arrive late. So, there is a band of time it can arrive. So, it has a edge 2, it has a edge 1, this is 3. Similarly, it has a edge 4, this is 5, this is 6. So, now, ideal case in case of ideal case I have my time period this to this which is t clock. This is my time period t clock which is having no jitters.

So, there is no jitter in this case, but if I have jitter so, your clock can vary this is your jitter actually this one is your t jitter, and this is the both are all the things are same actually. I have four small time intervals those are t jitter only all are same amount t jitter. So, now, I have two cases. So, I have two cases case 1 without jitter without jitter. So, in case of without jitter I have to consider only edge 2 in this case the flip flop 1 in this case your flip flop 1 samples at edge 2 and flip flop 2 samples at edge 5.

So, time period it reflects a time period of T clock. It reflects a time period of T clock. So, in this case my

$$T_{clk} \geq t_{clk2q}^{\max} + t_{comb}^{\max} + t_{setup}$$

Now, if I consider the jitter case 2 with jitter, I have the flip flop 1. So, we need to consider the worst case. So, in case of worst case the flip flop 1 will samples at basically edge 3 it will samples late and captures first. So, the flip flop 2 will sample at edge 4. Basically

because of the jitter it samples late, and it captures early. So, this is my worst case. So, in that case my time period T clock should be reduced by 2 jitter. So, this amount will be reduced this amount will be reduced and this amount will be reduced. So, my new time period will be from 3 to 4 which is basically t clock minus 2 t jitter. Now, my max timing analysis equation

$$\left(T_{clk} - 2t_{jitter}\right) \geq t_{clk2q}^{\max} + t_{comb}^{\max} + t_{setup}$$

So, in other case,

$$T_{clk} \geq t_{clk2q}^{\max} + t_{comb}^{\max} + t_{setup} + 2t_{jitter}$$

So, this is my new equation. So, what happened is that it requires more time in the right-hand side. So, this basically is larger. So, this part is larger means it requires now more time period. If your time period increases in summary if your t clock will be increased by 2 t jitters. So, your T clock increases imply that if clock my maximum frequency of operation will decrease. The jitter will reduce the speed of your operation is not good, reduce the speed of your operation it is not good. This is all about max timing analysis. Now, we will look into mean timing analysis. In case of mean timing analysis, in case of minimum timing analysis with jitter we need to consider all the minimum path. I have flip flop, this is the launch flip flop, this is the capture flip flop, I have some combinational delay is there, this is D, this is Q, this is clock, this is clock.

So, now, you have a clock is there, but clock is varying because of the jitter, you have two delay. So, if I say this delay is basically t clock to q minimum, we need to consider t clock to q minimum at this case. So, this delay is basically t combinational minimum and your data should be stable before the D pin of the flip flop 2 actually, this is flip flop 1, this is flip flop 2. So, here as we are doing the minimum timing analysis, so, we need to consider the t hold of the flip flop 2. So, now, I will do the basically waveform first, how my jitter waveform will look like. So, ideally it should arise here, and it is going like this. So, this is my edge 1, this is edge 2 and this is my edge 3. So, the edge can vary anytime between 1 to 3 and this is your launch clock edge. So, this is captured clock edge. So, here this is basically this is 4, this is 5 and this is 6. So, in this case, since I am considering the minimum timing analysis, I have two cases with jitter and without jitter. So, basically case 1, without jitter. So, what is happening here is that here we have to consider only the edge 2. So, the edge 2 is considered by flip flop 1 and flip flop 2. Edge 2 is considered by flip flop 1 and flip flop 2 and here,

$$t_{hold} \leq t_{clk2q}^{\min} + t_{comb}^{\min}$$

So, your hold time does not depend upon your time period. It is independent of time period. So, here this is the constraint whenever there is no jitter, and we need to consider edge 2 only. Now, we will consider the case 2 with jitter. So, in case of with jitter, I have two edges to consider for flip flop 1 and flip flop 2. So, in this case, your flip flop 1, in order to consider the worst case, the flip flop 1 should sample at edge 1, flip flop 2 should sample at edge 3. So, this will create a worst-case condition. So, now, since the flip flop 1, this will be sampling edge for the flip flop 1 and this is for the flip flop 2. Now, my hold t hold around this, this will be my t hold, this will be my t hold of the flip flop 2. So, now, my hold requirement is increased actually. So, now, earlier it is t hold, now it is t hold plus 2t jitter. So, my hold requirement is now increased from t hold to it is increased to t hold plus 2t jitter. Now, my equation will look like

$$\left(t_{hold} + 2t_{jitter}\right) \leq t_{clk2q}^{\min} + t_{comb}^{\min}$$

So, this one it will increase the impact of hold violation. So, now,

$$t_{hold} \leq t_{clk2q}^{\min} + t_{comb}^{\min} - 2t_{jitter}$$

So, this is my final constraint which will basically degrade your hold constraint, it will degrade the hold constraint hold requirement compared to without jitter. So, jitter is not good in terms of max timing analysis, and it is not good in terms of min timing analysis. So, it should be minimized as minimum as possible in your design.

Now, we will discuss about the sources of skew and jitter. So, there are different sources of skew and jitter, we will discuss those in detail. So, these are not desired. So, basically if you look into these clock skew and clock jitter, it will definitely depend upon one parameter clock basically the clock generation circuit because it is the clock generation circuit is responsible for this. So, you have a clock generation circuit. So, the clock generation circuit you have a PLL, the phased lock loop is used to generate a clock high speed clock inside a chip, or you can use some kind of crystal to generate a clock. So, PLL or crystal. So, both are having some amount of jitter depending upon their design specification.

You need to check the specification of the PLL specification of the crystal that you are using to generate the clock that is the source of jitter actually. So, that need to be minimum and that whatever the amount it is there that should satisfy our requirement. We need to take that value while doing the timing analysis. So, clock generation is one of the source of clock jitter. The second one is basically your power supply variation. So, your supply noise, if there is supply noise is there that will come to your clock frequency that will also create clock jitter. So, this will go to your clock generation circuit and that will lead to clock jitter. So, this PLL has a VCO, VCO noise will create clock jitter. So, we need to

look for a VCO which is producing less jitter actually. Then the third point is your basically coupling to the adjacent line. So, let us say if I have one line is there, one line is going and one another line is there. So, they can couple capacitive coupling between the two lines that will also create jitter that will also create jitter. Now, these are the sources of the jitter and clock jitter. Then what about the skew actually, clock skew? So, this is clock jitter. Clock skew basically if I look into the clock skew, it is the delay to the clock path actually. So, your interconnect variation, basically interconnect variation, then you have basically if you have a buffer, the buffer will also vary. Let us say I have a clock distribution network. So, I have a buffer here, I have a buffer here. So, both buffers even if it is in the same chip that will also vary. So, device variation, device or process variation. Process is here, I am not going into the process variation because a process variation has multiple components. I am just considering the within die variation, within the same die within die variation. So, it has multiple reasons, one is a random dopant fluctuation. The second region is that line edge roughness and the third one is called oxide thickness variation. So, these are the region for the basically device or process or within die variation. Then if you have a capacitive load, let us say I have a higher load here, let us say the number of flip flops it is driving, and flip flop is different. Let us say I have 3 flip flops here driving the network and here I have let us say 5 flip flop driving the network. So, because of the capacitive load, your delay of the path will also be vary. So, that is one of the reason of clock distribution. Because the delay of the buffer will be different. Then the fourth is basically temperature variation. Temperature variation will also lead to your variation. Let us say it can cause both jitter and skew, it can cause both clock jitter and skew. Let us say some part of the chip is working more, it has more active compared to the other part of the chip. So, there will be temperature hotspot will be there. So, because of the temperature hotspot, your path will also have different delay that will lead to the your clock skew. So, this diagram if there are the all these device variation, clock generation, power supply variation, interconnect variation, then capacitive load variation, temperature variation, coupling to the adjacent line, all these are responsible for your sources of clock uncertainty and indirectly your clock skew and clock jitters. In this lecture, we discussed about clock jitter, what is clock jitter and what is its impact on timing analysis. We also discussed about the sources of clock skew and clock jitter in detail.

Thank you.