VLSI Physical Design with Timing Analysis

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Week 03

Lecture 13

STA in Sequential Circuit with Clock Skew – II

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about Timing Constraint in Sequential Circuit with Clock Skew. The content of this lecture includes what is negative clock skew and how we can do timing analysis using negative clock skew. That maximum timing analysis or setup check with negative clock skew and minimum timing analysis or hold check with negative clock skew. After that, we will discuss some of the examples involving clock skew, positive clock skew and negative clock skew. So, in the last class, we discussed about negative clock skew. In case of negative clock skew, your clock and the data moves in the opposite direction. In this case, if you can see here, your data moves from left to right and your clock signal is moving from right to left. You have two flip flop, one is called the launch flip flop. This is your launch flip flop, and this is your capture flip flop.

So, the clock signal arriving to B is faster. So, the rising edge of the T1 will appear faster, rising edge of the clock arriving to the capture flip flop is T1 and rising edge of the clock arriving to launch flip flop is T2. So, T1 minus T2 is a negative. So that is why it is a negative skew. That is why it is called a negative skew.

So, now we will discuss maximum timing analysis considering negative skew. So, how my timing will change based on negative skew. So, here I have let us say flip flop 1, flip flop 2. I have a clock and clock is moving. This is your clock, and this is your D pin data pin, this is the Q, it is going through a combinational logic and this is the D pin, this is a Q. So, now we will see how my maximum timing analysis will change here. So, let us say this is your clock 1 and this is your clock 2. So, if I draw the clock signal like this, this is let us say clock 1, then the clock 2 will appear early. So, let us say that my clock 2 will appear early, the time period of the clock will remain the same. The time period of the clock will remain the same. So, now I have clock 1 and clock 2 and this is my skew which is negative, delta is negative, this is my skew. So, here how many edges I have? Let us say this is my first edge, this is my second edge, this is my third edge, this is my fourth

edge. So, basically if I can see here, so the first flip flop, this is your flip flop 1, this is your flip flop 2, flip flop 1 will sample at edge 1, the flip flop 1, first point is that your flip flop 1 will sample at edge 1, second point is that the flip flop 2 will sample or capture or sample or capture is same thing, sample at edge 4, edge 4. So, now my time period from here to here is basically T clock and this is my delta, this is my delta. So, the available time for considering skew is basically from here to here till this point.

So, this is T clock minus delta. Now in without skew my equation is that t clock to Q, I have two cases now, case 1 without skew, clock skew, I have maximum timing constraint equation,

$$t_{clk\,2q}^{\max} + t_{comb}^{\max} + t_{setup} \leq T_{clk}$$

But now case 2 with clock skew what will happen? My T clock is now T clock minus delta. So,

$$t_{clk\,2q}^{\max} + t_{comb}^{\max} + t_{setup} \leq \left(T_{clk} - \delta\right)$$

because my total available time to do the operation starts at edge 1 at this edge and ends at edge 4. So, the total available time will be reduced by delta because of the negative skew.

So, now my final equation will be t clock to Q maximum plus t combinational maximum plus t setup plus delta should be less than equals to T clock. So, now if you can see here your total time period will increase by delta. So, your basically the clock period will increase. Since delta is added in the left-hand side, your clock period will increase. So, implies that your f clock or the maximum frequency of operation will decrease.

So, your speed will decrease. Your speed of maximum speed of operation will decrease. Speed of operation will decrease. So, negative skew will impact your performance. It is not good for performance speed of your design. So, we have already discussed the max timing analysis. Here the main point is that the flip-flop 1 will sample at edge 1 and flip-flop 2 will sample at edge 4 and available time for doing the operation is reduced by delta. So, your total time period will be T clock minus delta. So, your left-hand side will have more thing to do by more evaluation to do by amount of delta. So, the clock period will increase since the clock period will increase your frequency will decrease. So, maximum speed of operation will decrease. So, the negative skew is not good for speed prospective.

Now we will go to the minimum timing analysis considering negative skew. So, here what we discussed is you have t com max. So, this is your t com max and this I have been added. This is your t com t clock to Q maximum. So, here in the next slide I have two flip-flops. My combinational path is smaller here, your t com min and your clock to Q min. So, now

I have a negative skew. This is your clock source clock. This is my D, this is your D, this is your queue, this is your D, this is your Q. We will draw the timing diagram. Next your clock, this is your clock 1, this is your clock 2. The clock 1 is coming late. So, it rises late like this. So, this is clock 1, my clock 2, this is your clock 2, clock 2 will come like this. It will come early because it is going to the capture flip-flop first. So, if you can see here, this is my delta, this is my delta negative skew, delta is negative. So, here in case of minimum timing analysis or hold check, this is also called the hold check. So, we have to consider the one edge, one of the edge. So, here I am considering this is the edge 1, this is edge 2, this is my edge 3, this is edge 4. If there is no skew is there, your clock 1 and clock 2 will be aligned at t equals to 0. But now what is happening is that in case of hold check, in this case we are checking we are checking edge 1 and edge 2 such that there should not be any hold violation. So, such that there should not be any hold violation. But in case of, if I have no skew actually, clock basically case 1 without clock skew, my hold constraint is basically,

$$t_{hold} \leq t_{clk\,2q}^{\min} + t_{comb}^{\min}$$

But in case of case 2 basically with clock skew, hold time with skew, negative skew actually. So, here negative skew whatever I was talking about negative skew only. So, your t hold will be changed to t hold plus delta, t hold plus delta, delta is negative. So will be delta. So here now, so

$$\left(t_{hold} - \delta\right) \leq t_{clk\,2q}^{\min} + t_{comb}^{\min}$$

So, my hold constraint with negative skew will be t clock to Q minimum plus t combinational minimum plus delta. So, this is my final equation in case of negative clock skew. So, what happens is that I have a term added in the right-hand side this delta, I have a term added in the right-hand side this delta helps to fix my hold violation easily. So, there will be there is less chance or no chance of hold violation if you have a basically negative skew because it is added in the right-hand side. So, your basically it is easy to fix your hold violation in case of negative skew. The negative skew reduces the risk of hold violation. So, in case of negative skew, you have an impact on the speed of your design. In case of negative skew, you have no hold violation. So, these are the two things because why this t hold minus delta? Earlier we are checking the hold across this second edge.

Now this will be reduced by delta, t hold minus delta. So, let us take an example how my timing analysis will impact with and without skew. With one example we will discuss this, basically example 1. So, we have a circuit given to us. Here the left hand side I have a circuit, it is the flip flop 1, this is the flip flop 2, this is the flip flop 3. So, this is f f 0, f f 1, f f 2. Now I have a clock, clock is same to all of them. So, this is the case for without

skew because the clock is arriving to all the flip flop at the same time. So, this is D Q, there is some combinational logic is there, then D Q there is some combinational logic is there. So, now I have some parameters given to me to do use that. One is your t setup is 2 nanosecond, t hold is 1 nanosecond, t clock to Q is 10 nanosecond, now I have two combinational, let us say this is comb 1, this is comb 2, I have two delay. So, but it has two paths are there. For example, t comb 1 has 5 nanosecond, this is the max delay and this is 2 nanosecond, this is the min delay. Similarly, I have another thing is t comb 2 which is having 6 nanosecond is your max delay equal to 1 nanosecond min delay. So, now I will do the first find the maximum frequency of operation. So, find the maximum frequency of operation for this design. So, since it is a maximum frequency of operation, I will do the max timing analysis. So, my answer will be like this. So, I have to consider two paths. Case 1, path between flip-flop 0 and flip-flop 1. So, here my T clock, so I have a equation T clock should be greater than equals to T clock to Q always start from rising edge of the clock, T clock to Q max and plus t comb 1 because I am considering flip-flop 0 to flip-flop 1 max plus t setup of flip-flop 2. So, here one set up time is given. So, it will be considered for flip-flop here in this case of flip-flop 1.

So, now if I change to my previous notation, I will just I can make this will be sorry this is flip-flop 1, 2, this is 3. So, this is 1, 2, this is flip-flop 2, correct. So, now I have basically clock to Q maximum. In this case both clock to Q max and min is same even but if it is both the numbers will be given you have to use the max value. So, here 10 nanosecond plus t comb max is 5 nanosecond plus t setup is 2 nanosecond. So, combined your T clock in this case is basically in this case this T clock is greater than equals to 17 nanosecond. Now case 2, if I consider between flip-flop the path between flip-flop 2 and flip-flop 3. So, now my T clock should be greater than equals to my clock to Q maximum, this value is 10 nanosecond plus t comb 2 maximum is 6 nanosecond, correct. So, this is your t comb maximum, t comb 2 maximum plus t setup of flip-flop 3 which is 2 nanosecond. So, it comes out to be 18 nanosecond, T clock should be greater than equals to 18 nanosecond.

I have to take basically the worst-case time period, the worst case time period is 18 nanosecond which is the max of that. So, if I can write the maximum frequency of operation, now I have T clock should be I should consider the max of both the path. So, I have let us say this is 1, this is 2 max of T clock 1 comma T clock 2, here it is basically 18 nanosecond. My frequency f clock, maximum frequency of operation is basically 1 by T clock which is basically if I found 1 by 18, it comes out to be 1 by 18 nanosecond.

So, it comes out to be 55.56 megahertz. So, this is my maximum timing analysis and this is my maximum frequency of operation for this design. So, now if I go into hold violation, if I go to the hold violation, now if I check the minimum timing analysis, so whether there is a hold violation is there or not, I have to do the minimum timing analysis in the same circuit. I have two paths. So, a minimum timing analysis, a hold check I am doing for the same circuit. So, hold check I am doing for the same circuit. So, what is happening here

is that this t hold, the case 1. So, case 1 is basically between your flip flop 1 and 2, flip flop 1 and 2. So, in this case your t hold should be less than equals to t clock to Q minimum plus t combinational minimum. So, now if you can see hold time if I go to the previous slide, t hold is 1 nanosecond. So, here 1 nanosecond should be less than equals to your t clock to q minimum, t clock to q minimum is 10 nanosecond. So, 10 nanosecond plus t combinational minimum is basically 2 nanosecond. So, here there is no hold violation, 1 nanosecond is satisfying 12 nanosecond, so no hold violation. So, then let us say case 2. So, case 2 is basically flip flop 2 and flip flop 3. So, you have to consider the path between flip flop 2 and 3.

So, t hold should be less than equals to t clock to Q minimum plus t combinational minimum. So, now if I see here my hold is 1 nanosecond, hold value is same for both the path and hold value is same for both the path and the clock to Q delay is also same 10 nanosecond plus t comb minimum is basically if I go to the it is 1 nanosecond, it is 1 nanosecond. So now, this is basically your 11 nanosecond, so it is satisfying the constraint, so there is no hold violation in this case. So, here if I assume one thing, here if I assume one thing, if I assume my t clock to Q minimum is basically 0.5 nanosecond and my t comb minimum is basically 0.2 nanosecond. So now, and my hold t hold is basically t hold is let us say same 1 nanosecond. Now if I have t hold is I have this equation same equation I am writing to make it familiarize you how these things is working. So, t comb minimum, so your hold is 1 nanosecond, now this is 0.5 nanosecond plus 0.2 nanosecond. So, here this constraint is not satisfied 0.7 nanosecond. So, this constraint is not satisfied, so this is not satisfied. So, here there is hold violation.

This is an example of how the hold violation will happen. So basically, we need to check that this is a case for hold violation. So here one more thing you notice that hold violation is does not depend upon your clock speed actually. If you change the clock speed also you cannot mitigate or solve the hold violation problem. Only way you can solve it by inserting buffer in the combinational path. Now we will discuss this example with clock skew. Same example with clock skew. So, we will discuss this example with clock skew. So basically, I have three flip flops. So, this is basically a pipeline design.

Three flip flops are there. Flip flop 1, flip flop 2 and flip flop 3. Now I have a combinational delay here. Now I have a combinational delay here. Now the clock is going, but here we have considering positive skew. So, your clock and data is moving in the same direction. So, this is your D, this is your Q, this is your D, this is your Q, this is your D, this is your Q, and your clock is basically like this. can have a clock here also. This path also you can add a buffer. So, this is my design. So here if you can see, here you have some buffer is there. So, the buffer delay is considered. Here I can writing the buffer delay. Buffer delay is 1 nanosecond. This is 1.5 nanosecond and here it is 2 nanosecond. So, this is given in the example itself. Now I will find with the both two cases. One is max frequency of operation, then the hold check actually. Hold check we are, hold check will

do and the other parameters whatever we consider is remain the same actually in this case. So, other parameters will remain the same. So here one reality is that actual circuit we have buffer, but in this case also we have added the buffer. This is we are going closer to our actual implementation in a chip. So, if you add the buffer how my timing will change. So, if we see here, I have a case 1, I have a case 1 with basically positive skew. So, there are two cases is also there like the previous case between flip-flop 1 and flip-flop 2. So, I have to write the timing constraint equation considering positive skew. So, your T clock plus delta should be greater than equals to t clock to q, t clock to q plus t combinational 1. So, this is comb 1 like the previous example t comb 2, t comb 1 max plus t setup. Now I have to find the value of delta in this case. Delta is basically here it is reaching at 1 nanosecond, here it is reaching as at 1.5 nanoseconds. So, your delta is whatever I defined earlier the capture arrival time, capture clock arrival time minus launch clock arrival time. Here if you can see 1.5 nanosecond minus 1 nanosecond, your delta here it is 0.5 nanosecond.

So, if I substitute here my previous equation, I have found this equation. So, here it is 10 nanoseconds, this is I will see the values 10 nanoseconds, 5 nanoseconds and 2 nanoseconds. 10 nanoseconds, 5 nanoseconds and 2 nanoseconds. Now my delta value is basically 0.5 nanoseconds. So, now my T clock 1 in this case, T clock 1 in this case will be greater than equals to basically 17 minus 0.5 which equals to 16.5 nanoseconds. So, the T clock 1 implies that T clock 1 is 16.5 nanoseconds. Now the case 2, basically you have flip flop 2 and 3. So now I have to find the skew at this point. Skew is in this case is basically at this point what is the arrival time versus at this point what is the arrival time difference. So it is 2 nanoseconds. So now if I find out the clock in the previous case, the clock whatever we find it out it is basically 18 nanoseconds, earlier it is 18 nanoseconds. So, this will be the T clock 2 was found to be 18 nanoseconds. Now my delta is 2 nanoseconds, my newt clock skew this is without clock skew. Now with clock skew my T clock 2 will be 18 nanoseconds minus 2 nanoseconds, it will be 16 nanoseconds with clock skew. So here now I have to find out the maximum frequency of operation. So, this is my T clock 2. So now I need to find out maximum frequency of operation. So, I have to find the T clock which is max of both of them. So max of both of them it is T clock 1, T clock 2, it is max of 16.5 and this is 16 actually nanosecond, 16 nanosecond. So, it is comes out to be 16.5 nanoseconds. So, my frequency of operation F clock will be 1 by 16.5 nanoseconds. So, the maximum frequency is basically 60.61 megahertz. So earlier case without clock skew the value is without skew is basically found to be 55.56 megahertz. So, this is without skew, but now with skew my F clock is changed to 60.61 megahertz. So, with the positive skew your speed increases. So, the conclusion is that with positive skew basically your speed of your design increases, speed of operation increases. So, this is the conclusion. Now we will go to the hold check. So now we will discuss the if I have positive skew how it will impact my hold check.

So, if I have a positive skew then how my hold violation will impact, hold check. So, I have two cases, case 1, the case 1 is between flip-flop 1 and 2. Then if I have between flip-flop 1 and 2 then if you can see here, you have basically the skew delta at this case found to be, delta value is found to be 0.5 nanoseconds. So, if this is the case my t hold plus delta should be less than equals to t clock to Q plus t combinational minimum, both are minimum. So, my t comb minimum, t clock to Q minimum this is basically if I can say the clock this is 2 nanosecond, this is 10 nanosecond and your t hold plus delta is basically t hold is 1 nanosecond and this is basically 0.5 nanosecond. So, it is 1.5 nanosecond less than equals to 12 nanoseconds. So, there is no hold violation. Then case 2, if I take between flip-flop 2 and 3, so what is the skew delta here is 2 nanoseconds. Here this is the skew. So, this is 2 nanoseconds, delta in this case is 2 nanoseconds. So now t hold is same, and delta is different but t clock to Q as we have taken both the thing same but t comb 1 here, this is t comb 2, second path. So here t hold is basically 1 nanosecond that is no change, delta will change by 2 nanoseconds and your t clock to Q minimum is basically 10 nanosecond, t combinational minimum it is 1 nanosecond, this is 1 nanosecond. So now this is 3 nanosecond less than equals to 11 nanosecond. So, this constraint is satisfied no hold violation. So, but if I assume, let us say this t clock to Q minimum is 0.5 nanosecond and this combinational minimum is 0.5 nanosecond. Now and let us say the t hold is basically 1 nanosecond and delta is 0.5 nanosecond. So, in this case, if I put the same equation again t hold plus delta should be less than equals to t clock to Q minimum plus t combinational 1 minimum.

Now if I apply the equation here, t hold is what? t hold is 1 nanosecond plus delta is 0.5 nanosecond should be less than equals to this is 0.5 nanosecond, this is 0.5 nanosecond. So, it comes out to be 1.5 nanosecond less than equals to 1 nanosecond. Hence this constraint is not met, so there is hold violation. There is hold violation. If your delta is more, the hold violation will be severe. So, in order to solve the problem, you need to insert buffer in the combinational path. It cannot be solved by changing the clock frequency or frequency of operation of your design. So, hold violation is a severe issue in case of digital design because of the clock skew there might be some of the paths have hold violation which is cannot be estimated during the analysis. So, there should be more attention should be paid for doing the hold violation check in all the paths in a sequential circuit. So, we discussed about the how to do timing analysis using negative skew. We discussed about also one example how to do timing analysis with and without considering the clock skew.

Thank you for your attention.