VLSI Physical Design with Timing Analysis

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Week - 02

Lecture 10

Delay Parameters of a Sequential Circuit

So, welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about different delay parameters of the sequential circuits. So, delay parameters of any path is very essential. Why? Because it is used to calculate the speed of your design. The speed of a processor will depend upon the delay parameters of the critical path. The critical path consists of both combinational circuits and sequential circuit. In the last lecture, we discussed about the delay parameters of combinational circuits. In this lecture, we will discuss about the delay parameters of the sequential circuits. So, first of all, we will discuss about what is sequential circuit with some examples. Then we will discuss about different delay parameters of the sequential circuits such as setup time, hold time and clock to queue delay. And we will discuss about what is the reason of setup time of a sequential circuit such as flip-flop and what is the reason of hold time in case of a flip-flop. We will discuss those things in detail.

So, what is a sequential circuit? So, in case of a combinational circuit, if you change the input, your output will appear after a certain delay. However, in case of sequential circuit, if you change the input, it will not appear immediately or after a delay, but it will wait for a signal, another signal called clock. So, here in this case of a sequential circuit, your output will depend upon the clock arrival time. When the clock will arrive, based on that it will react to the input. Otherwise, it will not do any operation. Even if your input changes, your output will not change. Similarly, so what we are doing in case of a sequential circuit is that your data is checking for the clock. When the clock comes, then only it will be sampled by the flip-flop or a latch.

What is a flip-flop or a latch? There are two types of sequential circuit which is popularly used. One is called flip-flop or FF and the second one is called the latch. So, which is the fundamental building block of sequential circuit is the latch. Why? So, because here we will discuss about what is a latch and a flip-flop first. Latch is lavel trigger. So, if your clock and you have a D and you have a Q, this is the Q. So, this is D, this is clock. In case of a flip-flop, you have a clock edge. So, that is why this symbol is there. If a bubble is

there, then it is a negative edge trigger. If there is no bubble here at this point, then it is a positive edge trigger. So, now you have D pin and you have Q pin. So, these are the minimum pins, but in advance flip-flop has multiple pins. So, how your latch behaves? Let us say I have a clock signal. I have a clock signal is given.

This is clock. Now you have D. Let us say it is a positive, transparent latch means in the positive half cycle, it will be transparent, and in the negative half cycle, it will not be transparent. I will change this line. This is my D here like this. Let us say how the Q will behave. The Q will change when your positive edge will come. I do not care about what is the behaviour at this point from till this point, but after that it will be able to sample this and it will sample till this point. Now even if your data changes here, it will not reflected at the output because it is a positive edge trigger. So again, it will capture at this point.

It will create some delay like this. So, this is basically the edges at which it will change. This is the edges whenever it is basically your positive. When the clock is positive, your output will change based on your D input. When it is negative, it will not change. When it is negative, here it will not change. This reflection will not come. This is the behaviour of a latch. What about the flip-flop? So, flip-flop will behave differently. Let us take this one. This is latch. This is for a latch. That is how the flip-flop will behave. So, I have a clock here. I have a D. So, let us say the D changing 1. Initially it is 1 and changing to 0 at this stage. Like this it is going. So, your Q will change at this edge. So, initially it will be you do not care what is the behaviour of this signal. At this stage, you do not care about it. But at this stage, it will start with 1, and it will hold the 1 till the next clock edge. And it will create a delay, slight delay and it will go to 0 again in the next clock edge. So, this is the behaviour of a flip-flop. Flip-flop will be trigger. A flip-flop is an edge trigger device, and the latch is basically lavel-triggered.

So, this is the basic two sequential circuit. One is latch and a flip-flop. So here we discussed about a positive transparent latch. So, this is a positive transparent latch. And here we discussed about the positive edge triggered flip-flop. So similarly you can create a negative transparent latch and negative edge triggered flip-flop also. So now you can think this is a flip-flop. But your flip-flop consists of two things, two latches. Your flip-flop has two latches. One is called master latch. The first stage is called master latch, and the second one is called a slave latch. So here if you can see you have two multiplexary zone, but indirectly they are latch. Why? Because they have a feedback loop is there. So what it says that if you can see this clock, so the clock when it is 0, it is sampling the input data. It samples the input D. So hence it is a basically when clock is 0, it is a negative latch. When clock is 1, so this first one is a negative latch. The first one, this one, is a negative latch because when the clock is 0, it samples the D; hence, it is a negative latch. When clock is 1, it is opaque. It is not sampling the data to QM.

But when clock is 1, whatever the data here at this point QM, your second stage will sample that this is the first stage. Let us say I will be more clear. This is first stage and this is the second stage. So, your first stage is your master stage and the second stage is your slave stage. So, in first stage, clock is 0, it samples the input D hence it is a negative latch. In second stage, clock is 1, it basically that second stage will sample, it samples the value in QM what is stored there. Hence it is a positive latch. So you should know that in case of a master sleep flip-flop, the first stage is a negative latch and the second stage is a positive latch. And when clock is 0, it samples the D input to QM and in that case, your first stage is transparent in the clock is 0, that is why it is called a negative latch and at the same time, the second stage will hold because you see here the second stage is holding the data. And when clock is getting 1, this QM, what is the value here QM, it will pass it to the second stage.

Clock is getting 1, the QM will be sampled by Q and your first stage will hold the data because here there is a feedback there. So, this is the basic principle of a flip-flop, which is a positive edge-triggered flip-flop. So, this is a most important point is that your flip-flop is a positive edge triggered in this case; if it is a negative edge triggered, these things will be reversed. So things will be reversed. The first stage will be positive latch and the second stage will be the negative latch. Now we will discuss about, so we discussed about a flip-flop, we discussed about a latch and we discussed about how the flip-flop will be created using the latches. Now we will go into detail, there are some delay parameters are there, how things will happen inside that. So what are the delay parameters we have? One is called setup time and the second one is called the hold time and third one is called the T-clock to Q-delay. So what is setup time? Let us say I have a flip-flop here, I have a flip-flop here, I have a clock here, this is D, this is Q, there should not be any arrow here.

First, I will draw the clock, then I will discuss about, then I will draw the D. So what is happening is that if you have something, some delay, minimum delay before the rising age of the clock, you should change the D such that it will be captured by the flip-flop. So the minimum distance from the clock edge, you should sample the D, you should change the D, sample the D means you should change the D such that it will be captured by the flip-flop at the same clock edge. So let us say this distance is the minimum distance, this is called your T-setup. This is called your T-setup. Similarly, there is a time after the rising age of the clock that your data should be stable in order to sample by the flop. This is your T-hold. So we have setup time which is before the rising age of the clock, data should be stable, minimum time before the rising age of the clock, your data should be stable such that the data will be sampled by the same clock age, then it is called the setup time. And the time after the rising age of the clock, your data should be stable such that it can be captured by the flop in the same clock age is your called the hold time. So now there is some time required from the once your data is sampled captured, take some time to come to the output.

So this is your Q. So it takes some time let us say this much of time after the rising age of the clock. So I will erase this line to look it better. So, this delay is my T-clock to Q. This delay is called my T-clock to Q delay. So, we defined all setup time, hold time, T-clock to Q delay of a flip flop. Now, we will go inside a flip flop and check what are the delay is involved here. So before we go there we have to understand two things. One is a inverter and a transmission gate. Inverter I have already repeated multiple times. So you have basically, if you give a signal, then the signal will be opposite polarity after a certain delay at the output.

So I am not going to discuss more about inverter, but transmission gate is need to be explained. So transmission gate is basically is denoted by this kind of symbol. So you have a symbol like this, actual structure consisting of basically transistor is like this. Here I am drawing this is the NMOS transistor, this is a PMOS transistor like this. So, both are same structure. So here you have clock, here you have clock bar, here this is clock and this is clock bar. What is happening is that whenever your clock is 1 and clock bar is obviously 0 then whatever the input you give here that will come as output after a delay when the clock is there. So when clock is 0 here and clock bar is 1 here, so in this case implies is there your output will be delayed version of input. But when clock is 0 and clock bar is 1, your NMOS will off and clock bar is 1 means your PMOS is also off, the output will not change.

What is the previous value? It will hold that. Whatever the input will do the change that will not come as the output. So, this is called transmission gate. We will use those two inverter and transmission gate to create our latch first and from the latch we will do the flip-flop. So, whatever I discussed earlier, basically, the flip-flop consists of two parts. One is called two latches. First one is basically your negative latch and this one is your basically positive latch. So what is happening here is that whenever your clock is 0, so this is basically 0 and this is basically 1. So, this is transparent and here your clock is 0 and this is 1. So here this transmission gate is off, this is off and this is transparent. Let us say whatever the data here, this d data will come in this path and it will come and stay here.

So, if you can see here, your data will come here and stay here. It will not copy to the second stage. Like this example, your data will come here in the negative edge, it will come here and stay here at this point. It cannot go to the next stage because this path is closed here. Similarly, if you go to that diagram, this one, your clock is 0, and clock bar is 1, and this is cut off.

So, this path is not available to you. So what it is saying that, so whatever the data will come here, it will stay at this point, and then in the positive rising edge, this data will copy at this point whatever the data will be there at w, in the positive edge it will sample to your output. So now what is the setup time? Setup time says that let us say if you do whatever I told in the diagram, again I am repeating here, let us say I have a clock signal here, I have

a clock signal here, my data should come earlier than the clock signal. For example, here, if you can see how much time it should come before, it should come before the delay of this inverter, delay of this inverter, delay of this inverter, delay of this inverter, and this transmission gate. So this delay is whatever, so it should be more than this T setup; at this point, T setup should be 3 inverter delay plus 1 transmission gate delay, T x, I am writing for transmission gate. So, this is the delay of T x, this is the delay of inverter, I am assuming that all the inverter is offering same amount of delay.

So, I have 3 inverter delay plus 1 T x delay. So, this is the reason for my setup time. So, this is my setup time. So, your data should come, so data should be available before the setup time. So now it is very clear, if your data is coming late, it will not come to this point, at this point z, so it cannot be sampled when the clock rising happening. So, this is the reason for my setup time. We will discuss what is the reason for hold time in a flip-flop. So, if you can look into this flip-flop, we can have different transmission gates are there. So I am denoting this one by T1, okay, this is one transmission gate, let us say this is denoted by T1, this is T2, this is T3 and this is T4, okay. Then my clock is 0, okay, my clock is 0, so my T1 and T4 is are on and T2 and T3 are off, okay. So now if my clock moves from 0 to 1, okay, clock moves from 0 to 1, okay, so what will happen? My T1 and T4 are off and T2 and T3 are on opposite.

So, this time of transition from 0 to 1 is very important, okay, time for transition from 0 to 1 is very important in terms of hold time. How? We will discuss in a minute. So, what is the thing is happening is that this node W is driven by two paths; it is driven by this path and this path. Let us say whenever it is transition is happening 0 to 1, I am interested in sampling the data Z to output Q but if some data from this side come and return to W, then this W will be go directly to Q which is a undesired effect which is causing a hold violation, okay. So the main reason of hold violation is that I have two path, this is let us say the path 1 and this is let us say the path 2, I want the data from path 2 to be sampled by the flip-flop, not the data which is coming in the path 1 to be sampled by the flip-flop, okay.

So if the data from the path 1 is sampled by the flip-flop, then this is called a hold violation, okay. So this is the main concept of hold violation; then we will go to the three different cases, okay? So case 1, where t, t x, okay is greater than t initial, then your hold time is positive. So I have a clock edge and I have a data, so means that this distance is positive.

So, this is clock, this is data, okay. So there should be, your data should be available after the rising edge of the clock in this case, in the case 1, okay. So, in this case your data should come after the rising edge of the clock such that it will be sampled by the flip-flop, why? Because if you can see here, you have t initial and t, t x. If t initial is smaller, then data can go by the path 1 to w faster, okay. If t initial is smaller, if this delay is smaller, then it can go to w in less time and it can corrupt the hold data. So your hold, your data should come after the clock edge, so hold is positive.

Now I have a case 2, when t, t x is equals to t initial. So your hold is 0, hold time is, so what is happening here? You have a clock, you have a clock and you have a data that can come in the same time, okay. This is a clock, this is your data and both are coming in the same time, means t hold is 0. So here the t hold is positive, okay. So what it says that my delay of the transmission gate t1 is same as delay of the t initial. So by the time the data comes to this point, okay, my transmission gate is closed, okay. So it will not go and reach till w. So, the data cannot reach w because the transmission gate is closed. So t hold is 0 here, okay. Even if the data comes with the rising edge of the clock, it cannot pass the transmission gate, the barrier, transmission gate barrier it cannot pass. So your t hold is 0. Now the third case, case 3 where my t t x is less than t initial, then the t hold, hold time, hold time is, hold time is negative, hold time is negative, okay. So if it is, hold time is negative, how can I represent that one? In timing diagram I am doing it in a different colour. So let us say this, this is my clock, okay. My data, this is my clock signal and this is my data signal, okay. So this is my d. So, in this case, what is happening? So data is changing before the rising edge of the clock, means this hold, this distance is negative because I am finding the hold with respect to the rising edge of the clock.

So, t hold is negative here, okay. So, t hold is negative here. So, means that even the data changes before the rising edge of the clock, it cannot corrupt the data because my t delay of the t initial means the buffer before the transmission gate delay, or the t initial is larger. So, this delay is larger. So, this delay is larger means it never reach to this point, okay, never reach to this point. So, even if your data changes earlier than the rising edge of the clock, it cannot corrupt the data what is stored in w at the rising edge of the clock.

Hence the hold time is negative. But so then the question arises we can add more buffer before the flip flop such that the hold time will be negative, I do not have any hold violation. But what is happens is that if you add more buffer to the d pin or the t initial, so it will your make your hold time negative but it will have a penalty on the set up time. Your set-up time will also increase. If your set up time will increase then your speed will decrease, okay.

So that is the main reason behind the hold time. So, in this lecture we discussed about latch and flip flop. We discussed about the operation of latches and flip flop, how the flip flop is created using the latches, then we discussed about the region of set up time, what are the gates inside the flip flop is responsible for the setup time and also we discussed about what are the gates inside the flip flop is responsible for the hold time.

Thank you for your attention.