Power Quality Improvement Technique
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Lecture - 22
Multi-Level Inverter – III

Welcome to our NPTEL courses on the Power Quality Improvement Technique. Today is our 3rd lecture on the Multi Level Inverter and its control strategy. Mainly we are discussing on the suitable PWM technique for this multi-level inverter.

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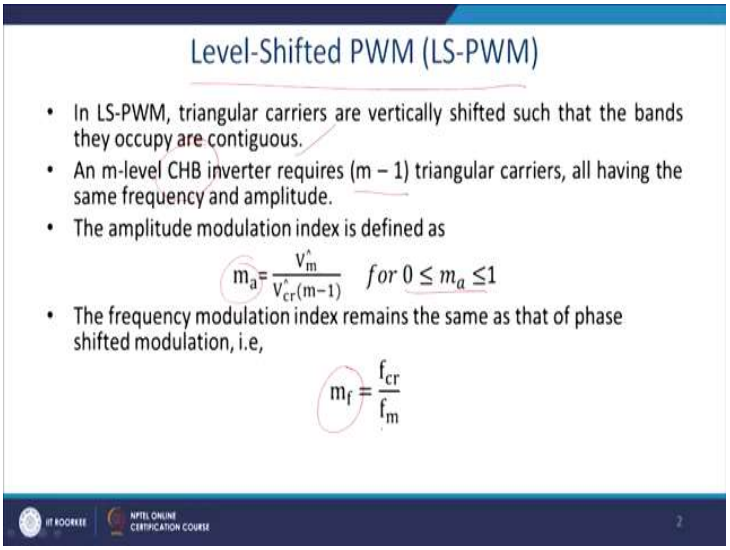

Now, we were discussing the phase shifted PWM and just for the recap I am discussing it. Please refer to my previous lecture. In the level shifted PWM, the triangular wave carriers are vertically shifted. In next slide I am going to show you the picture of the bands they occupy are contiguous. That mean you will find it more compact. In an 'm' level cascade H-bridge inverter requires $m - 1$. If you have a 5 level you require 4 carrier, all having the same frequency and the amplitude.

The amplitude modulation index is defined m_a, $m_a = \frac{V_m}{V_{cr}(m-1)}$ for 'm' is 0 to 1, modulation index. For the frequency modulation index, it remains the same of the phase shifted modulation that been $m_f = \frac{f_{cr}}{f_m}$. So, you do not have any advantage on the frequency for the level shifted modulation. But what is the advantages of the level shifted modulation?

It is very easy to generate same triangular wave and add that dc shift width and thus you reproduce all this waveform.

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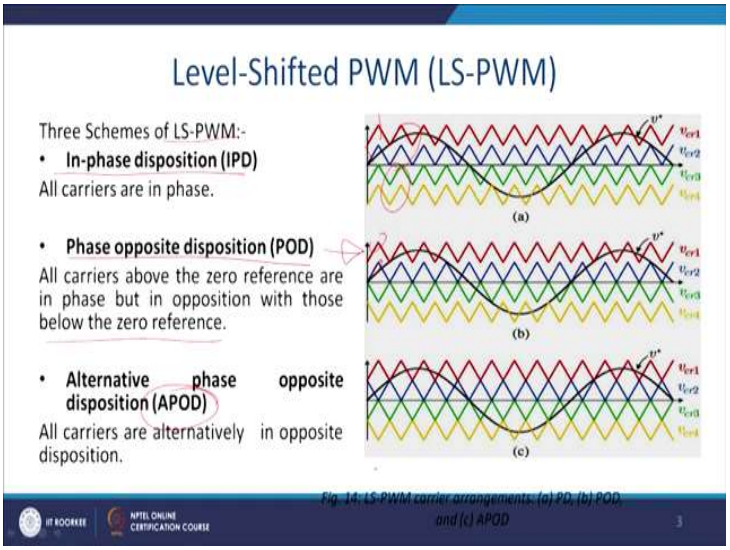

Fig. 14: LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD

This is a same phase. It is red one thereafter this upper triangle, this is the lower triangle thereafter this blue one, then green one, then yellow one. In this scheme the level shifted PWM can be in phase disposition (these are all in a same phase) or it can be phase opposition disposition. This can start at 180-degree phase shifted. It is the same op-amp. We just give it to the inverted logic. So, you can have a 180-degree phase shift. Making this control logic is quite simpler and another is phase opposite disposition that is what I was talking about. Then it will start like this.

Ultimately this has to be this point which will come here for the phase opposite disposition. All carrier wave above 0 reference are in phase out in opposition with those of the above 0 phase reference. So, 180-degree phase shift will be there for this carrier wave and this carrier wave. That is what I was talking earlier, this alternative phase opposition disposition. So, this one is your ultimately this one, where this red and blue are in a same phase, where this green and yellow are 180-degree phase shifted. On the other hand, this is aperiodic. This is more preferred.

Here this one and this one is 180-degree phase shifted and again this green and red are in the same phase. Same for the blue and yellow are in the same phase and it looks like quite compact. So, this APOD. This figure shows that pardon me this cannot be shown properly,

This figure shows that the carrier wave is with phase disposition, phase opposite disposition and alternate phase opposite disposition. his is the (c).

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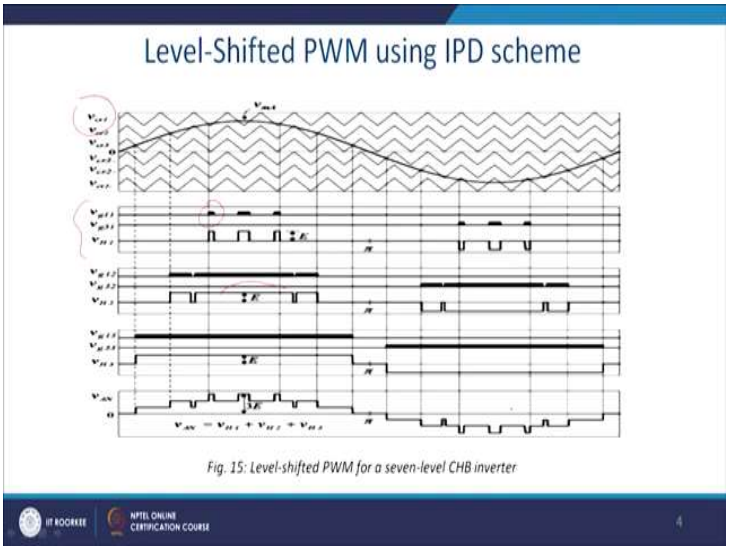

So, what happened, if you have this level shifted? It is a seven-level cascade H bridge. So, you have a six such carrier wave. So, you have these values and you have 1, 2, 3 and 1, 2, 3 and you can see that these are the gate triggering for the first gate, second gate, third gate and same way for the other and ultimately this will come into the picture when the upper carrier wave one is on.

This will come only and ultimately this will come when it is above it and similarly so you get the logic for the others. For this positive half cycle ultimately, you will get this kind of level. Seven level in case of the cascade h-bridge inverter. So, you can see that this is the three levels and rest is also three level. This is a way to work with the level shifted PWM.

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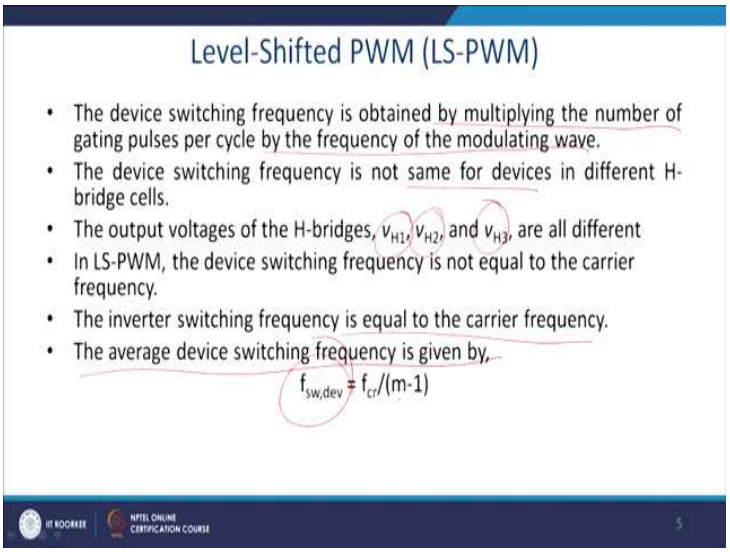

The device switching frequency is obtained by multiplying the number of gating pulses per cycle by the frequency of the modulating wave. This is the way it works. This device switching frequency is not same. That is a one of the major drawbacks. If you go back you can find that this switching is more and for this reason, we can see that in the different cascade H-bridge will operate at different frequencies. If you put them in the same dc voltage bus then the losses will be more to those which is switching more.

Output voltage of this H-bridge, V_{H1} and V_{H2} and V_{H3} are all different as you have seen and the level shifted PWM the device switching frequency is not equal to the carrier frequency and it is different. Inverter switching frequency is equal to the carrier frequency. But individual frequency is generally more than the switching frequency. Thus, the average switching frequency is given by this switching frequency by $m - 1$.

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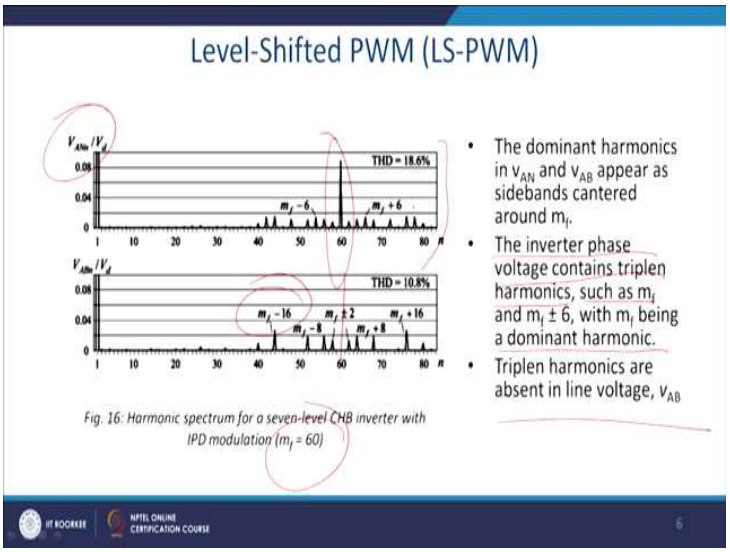

And ultimately this is the case. For the level shift at one (Please recall we have a phase shifted on one also) the ratio we assume that 60 and for this reason we can see that this is the phase voltage versus V_d and you have a fundamental apart from that you have a 60th harmonic and there after a $m_f + 6$ and $m_f - 6$ and so, on and ultimately you get around 18 percent THD.

On the same hand assuming that m_f is 60 for the seven level and for the line voltage you can find that. You know these are the all spectrum at 60. It is less and, but at m_f since it is seven level you will find that it is 8 will come into the dominate figure. You will have a component $m_f - 16$, $m_f - 8$, m_f minus 2 plus n minus both. The inverter that is what I said. The inverter phase voltage contains triplen harmonics such as m_f and $m_f \pm 6$ with m_f being a dominating harmonic this one.

But you can see that this is missing here in case of the line voltage. But the triplen harmonics are absent. Ultimately all this m_f minus 6 this component goes out and thus you get a better THD in line voltage.

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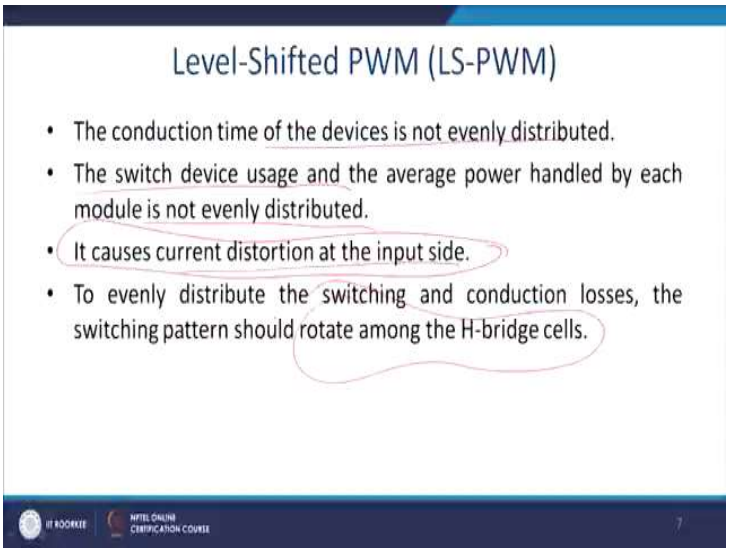

Few more observations. The conduction time of this devices not evenly distributed. As you have seen and due to that what happened? The conduction losses of the different cascade H-bridge multi level inverter, cascade entities, cascade H-bridge will be different. So, losses are not equally placed, so there were local hotspots.

The average power handled by the switch devices of each module is not evenly distributed. That is also a challenge. This is something we have to address and we have to find maybe the better control technique. It causes the current distortion at the input side. So, this is the major drawback from the power quality point of view. So, if you are feeding, input current distortion will occur. To evenly distribute the switching and the conduction losses the switching pattern should rotate among all H-bridge.

So, you first give some kind of pattern triangle wave to some of the H-bridge, then after few cycles you change those patterns which will rotate evenly. So, that these losses get distributed throughout those all the H-bridge equally. This is the way we generally do it.

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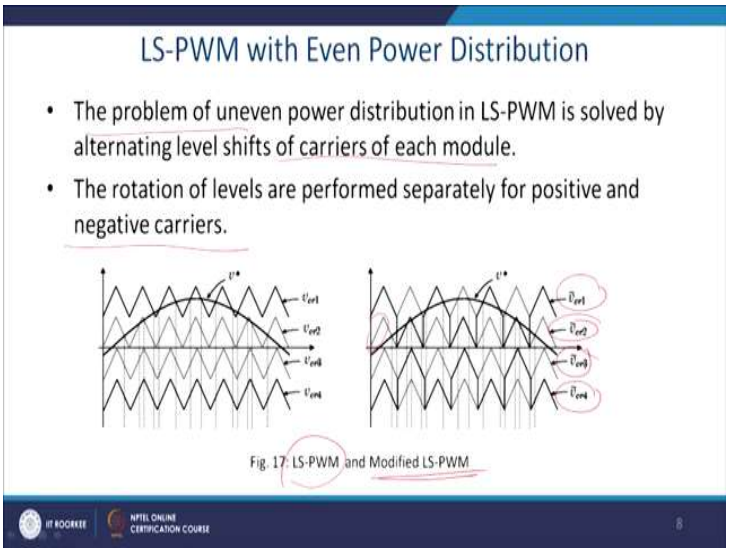

That is what I was discussing right now level shifted PWM and this one is a modified level shifted PWM. Let us see what is the difference between these two. The problem of the uneven power distributions in level shifted PWM is solved by alternating level shifted carrier of each module.

So, what does it do? The rotation on the levels are performed separately for positive and the negative carrier. So, what happen? Firstly, once this will go up and this will come down here and thereafter again this will go up and this will come down. I try to show the bolder portion of it. This is the bolder portion of it. This is the topmost carrier wave. So, it will come down and this wave form which is little gray in color that carrier will go up and then again this will go up and they may can go up down, go up-go down, go up-go down like that.

So, it will have a gothic kind of structures and that will be the carrier wave '1' and this grey one will be the carrier wave '2' same is repeated in the negative half cycle. This is the carrier wave the grey one and the dark one is the carrier wave '4'. After this it will go up, again come down, again go up, come down like that to equi-space the losses conduction as well as the switching. So, now there can be another solution to it. Instead of this require little complex circuitry. Every quarter cycle you have to give one dc boost.

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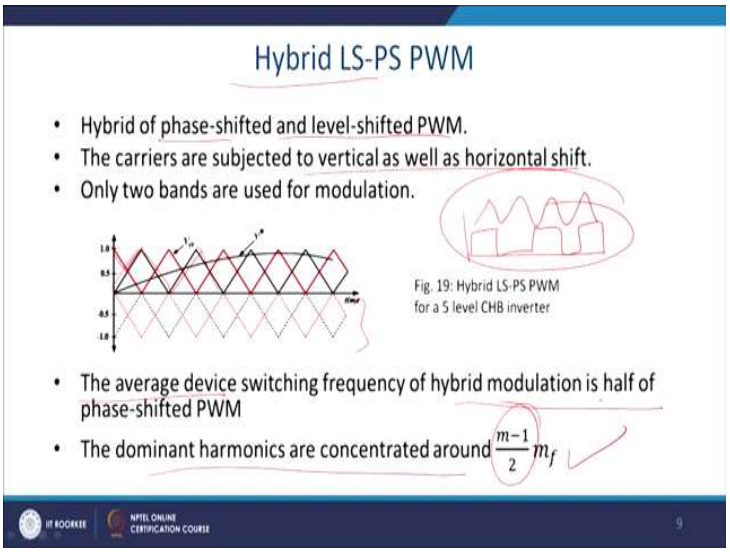

So, ultimately what happened? It is quite easy. So, you have this one and you have a square wave. So, you add a square wave and it will go up then again it comes down, then again goes up, then again comes down like that. So, you have to add these two cycles. Ok? So, this is the way we generate the previous level shifted PWM.

Now, this is a hybrid level shifted as well as the phase shift PWM and it is a combination of both. So, we always believe that hybridization works better. So, hybrid of the phase shift and the level shift PWM both. See that what we do. The carriers are subjected to the vertical as well as the horizontal shift. So, here this is a red line and this is easier to do.

So, you can see that. Otherwise you can have only this and as well as the black portion of it and like that. But you have phase shifted it the red one same for the black one. Thus, its mirror image if you consider this 'x' axis line to be a mirror and this will be followed into the 'x' axis. You just try it out, different control techniques. Because unless you try those techniques, you will not be able to appreciate this lecture.

The average device switching frequency of the hybrid modulation is half of phase shifted PWM. Why? Because you can see that this is your switching frequency of the carrier wave, but effectively you are coming to this red and black as an effective carrier wave. Thus, the dominant harmonics are concentrated around m minus $\frac{(m-1)}{2} m_f$. So, this is the issues here.

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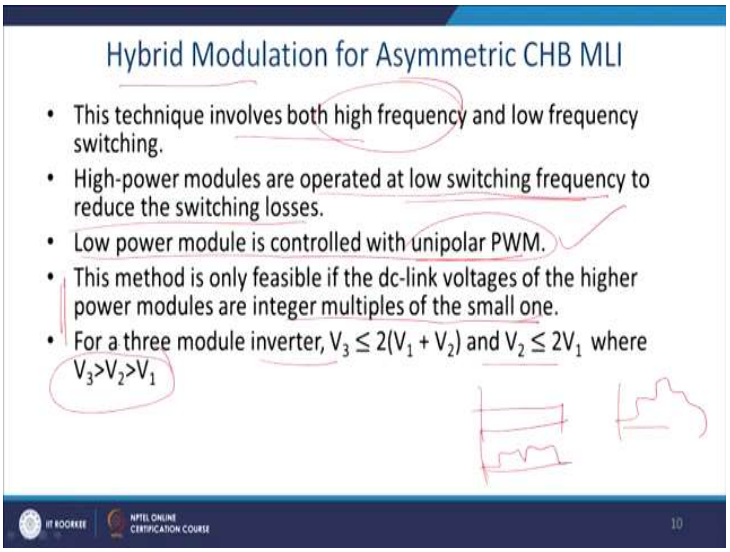

So, what we can conclude from the hybrid modulation asymmetric multi-level inverter? This technique involved both high frequency and the low frequency switching. The power modules are operated at a low frequency to reduce the switching losses.

Power modules are controlled with the unipolar PWM, low power modules and this method is only feasible if the dc link voltage, of the carrier wave and the modulating wave are the integral multiple of some small one. Then only this is a feasible. This is another strategy. This one is called hybrid modulation asymmetric cascade H-bridge multi-level inverter.

In these techniques you know you have a combination of both high switching frequency and low switching frequency. The power module operated at the low switching frequency because you can have a combination of the maybe GTO, IGBT. Some cascade H-bridge is made of GTO, some cascade H-bridge made of IGBT. So, those who are made of GTO they of course can handle more amount of power and they will operate at the low switching frequency to reduce the switching losses.

Lower power module is controlled by the unipolar PWM and this method is only feasible if the dc link voltage of the higher power module is integer multiple of the small one. So, you generate this amount of thing. Then what you do? You add or subtract this thing. Thus, you can get a multi level kind of thing. This is a way it operates. For the module inverter

V_3 is less than this and where to make this condition for fulfilling that V_3 should be greater than V_2 and greater than V_1.

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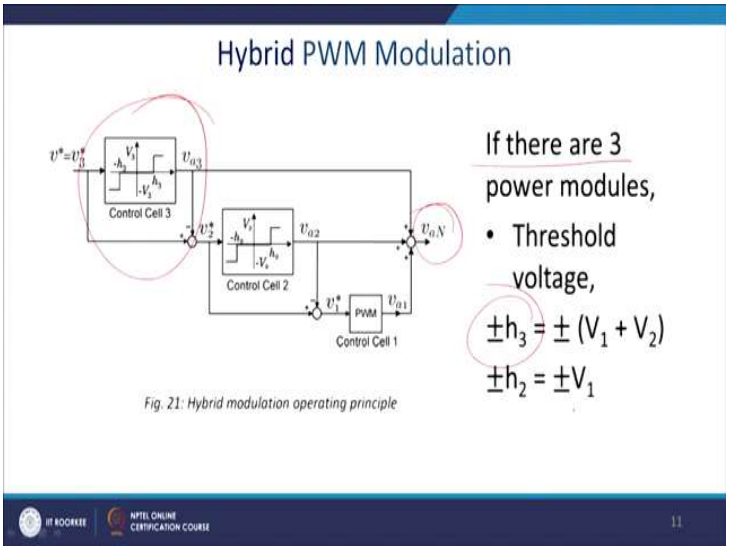

Now, you see that the hybrid modulation technique. This is the one control cell and ultimately you generate the voltage V_3 and it will come out here. So, this one will be fed here. This is another control cell then this will be feeding here ultimately you will get a value v_{aN}.

Here if there are three power modules, the threshold voltage that is $\pm h_3 = \pm(V_1 + V_2)$ and $\pm h_2 = \pm V_1$ and combination of it will give you the different level of voltage. This is the way of hybrid modulation technique. So, see that how it works.

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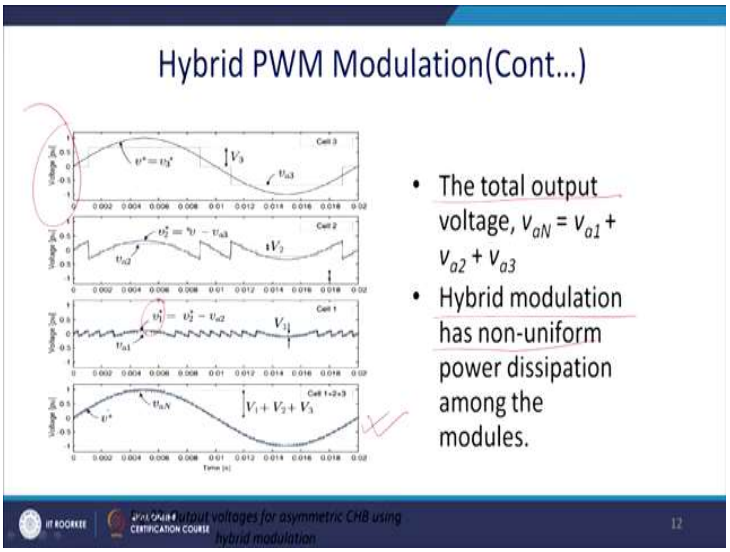

This is the low frequency device maybe GTO. So, it will be on for most of the time with that you can have this kind of carrier wave and thus you have a switching like this. So, ultimately you subtract this is $v - v_{a3}$ and so, you got $v_2 - v_3$ and then again $v_{a1} = v_2 - v_3$ and ultimately what you get essentially is that v_{a1}, v_{a2}, v_{a3}. This is what you see that how to reduce the THD of this output waveform for the inverter.

It is not that you will generate it and you can generate almost close to the sine wave and that we can fed to the motor. Thus, what we can conclude here is that the total output voltage $v_{aN} = v_{a1} + v_{a2} + v_{a3}$ and hybrid modulation has not uniform power dissipation among these devices because you can see that. This is most of the time is on and it may be IGBT it may be GTO and others are IGBT.

So, losses also will be spread over differently. This is also a challenge, but this voltage is less than this voltage. So, for this reason it works. You can see the voltage here. It is a per unit value one and it is restricted to 0.5 almost and here it is restricted to very close to 0.2. 20 percent of the voltage because here switching is more and you can have a faster device with the highest switching frequency and thus you can get this kind of close to sine waveform.

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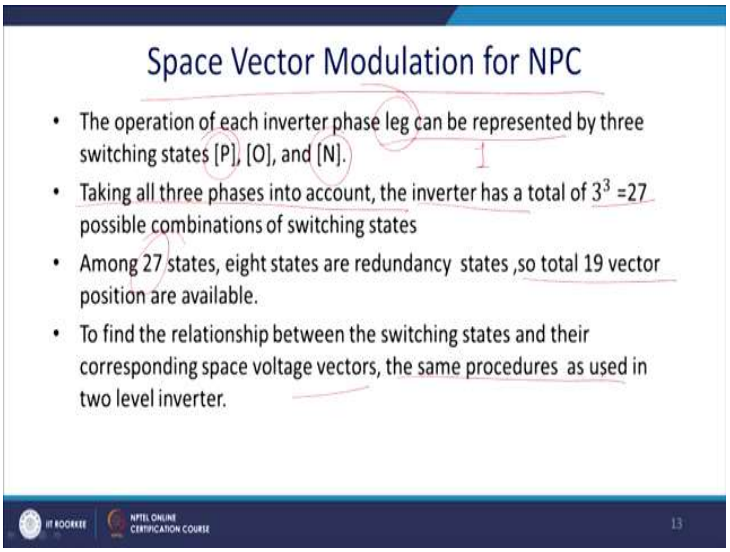

Now, let us come to the space vector modulation technique. I have discussed the space vector modulation technique for this two-level inverter and that has been extended to the three-level inverter. So, basic assumption is same. So, we require to find it out since we managed with 1 and 0 in case of the two level. But we required to since there is a three level, we shall state the concept P for the positive, 0 or O for the middle level and the 'N' for the lower level.

So, this is our convention we are following. We have taken this conversion from the Ben Wo books. The operation of each inverter which leg can be represented by the three switching states. That is P 0, P O, P N. Taking all these phases into account the inverters have a total 3 to the power 3, that is 27 states of possible combinations of switching states. Among 27 switching states, eight states are redundant. So total 19 vectors are possible, to find the relationship between this switching states and their corresponding space voltage vectors, the same procedures as used for the two-level inverter will be applied.

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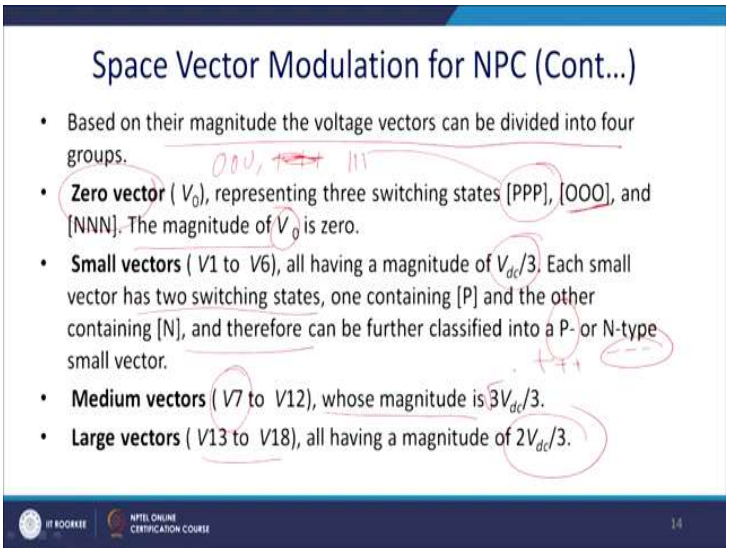

Let us come for the grouping of these vectors. Based on the magnitude of the voltage vector can be divided into the four groups. One is zero vector you know that 0 0 0 or 1 1 1 and the null vectors or here you can have a zero vector. So, zero vector will be as switching states of [PPP] that is corresponds to 1 1 1, but here also there is a another extra thing that was not present in case of the two level inverter, that is [OOO] and then also you can get 0, [NNN] all the lower switches are closed. The magnitude output voltage is going to be '0' then.

The small vector V1 to V6 all having a magnitude $V_{dc}/3$. Each small vector has two switching states. One containing 'P' and the other containing 'N' and therefore, can further be classified as P or N type or some books write triple plus and triple minus type small vectors. So, there will be a medium vector. We will say that it will be these vectors are in between V7 to V12 and whose magnitude is three $V_{dc}/3$. Ultimately it is V_{dc} and there will be a large vector. So, that will be the full length of this. So, that will be $2V_{dc}/3$. So, there will be $V_{dc}/3$. There will be V_{dc} essentially and $2V_{dc}/3$. So, this is the case.

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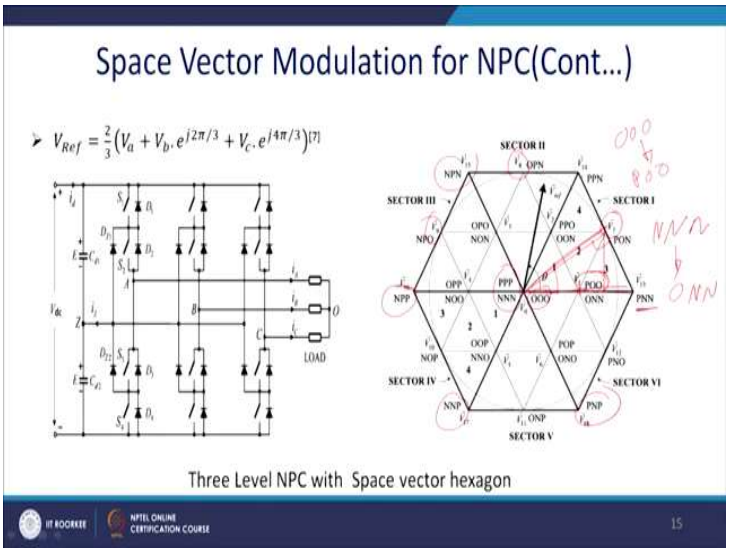

Now, see that I just represent it here, diode clamp three level inverter for sake of simplicity you can extend this to any level. So, this is the '0' and you can have this PPP, NNN, 0 0 0 as a 0 vector. Thereafter V_1 this is the magnitude. Look this magnitude is essentially $2V_{dc}/3$ and essentially you can have a half voltage vector. You can see the magnitude of it. So, from the triangle you can see that this angle value.

That magnitude is essentially the radius and the radius is essentially V_{dc} and this much magnitude will be for the $2V_{dc}$. These vectors are called half angle vectors and this is called the half voltage or the small vectors in some notations. So, what happened here? So, you will have this hexagonal structure. Now, how you will calculate the timing of this hexagonal.

Now, if you are here, then you know that what are the voltage you will be made off. See that is 0 0 0. Now there is a redundancy. That is a beautiful part of it. If you were at OOO or 0 0 0 whatever you say, then if you want to apply the V_1 then you have option to apply POO and ONN. Generally, if you have 0 0 0 then it makes sense to have a one bit change and come to POO. But let us say if you are at NNN and that is also the case.

If you want to apply V_1 then you should apply you know ONN. So, we want that one-bit changes to have. That switching losses will be also minimize if you have a two-bit change. That mean the more switching on and off. So, thus there is a combination. So, you can generate the voltage V_1 with the help of POO and ONN and once you generate, if you want

to generate this voltage the full voltage vector that is essentially your PNN. Same way the negative vectors that will be NPP. Similarly, it will be PPN. It will be NPN. It will be NNP and it will be PN.

So, these are the constant vectors and this also are constant vector. If you want to generate the voltage vector 7 this half angle vector, this angle is 30 degree. So, PON is the only option. But if you want to apply the half vectors for example, here you can have option. You can choose for PPO and OON. So, thus you can see that in this region what are the vectors that will be useful to construct this waveform. So, please go back, since this is restricted here and take those portions of the triangle and those vectors will be useful to construct these devices.

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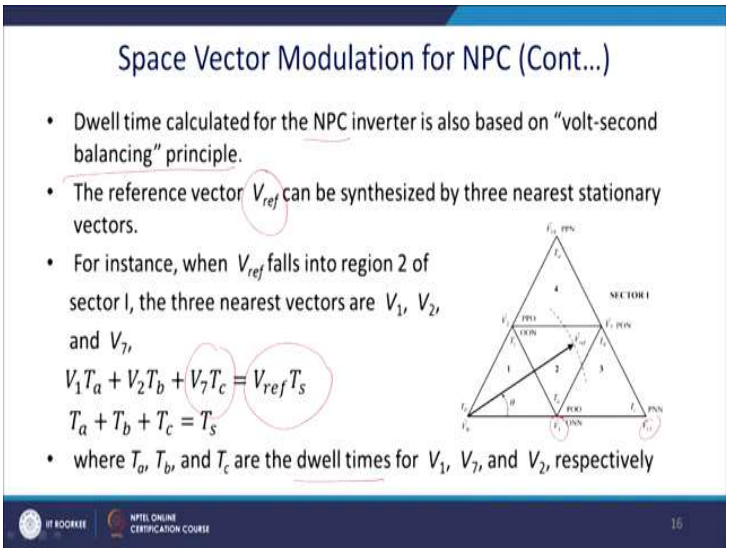

So, let us consider that, it is in this coordinate. First coordinate. So, ultimately you make with this vectors V_1, V_3 and V_2. How you will calculate the timing of this vectors? So, now, this is a way to be followed. Dwell time calculation of the neutral point clamp inverter is also based on the volt balancing principle as we have seen and detailed discussion for the two-level inverter is done. The reference vector Vref can be synthesized with the three near stationary vectors. Here you can see that it is V_1, V_2 and the V_7 and thus you just write it down V_1 into T_a. For this it will be on. Later $V_2T_b + V_7T_c = V_{ref}$ and $T_a + T_b + T_c = T_s$ where T_a, T_b, T_c are the dwell time for the V_1, V_2, V_7 respectively.

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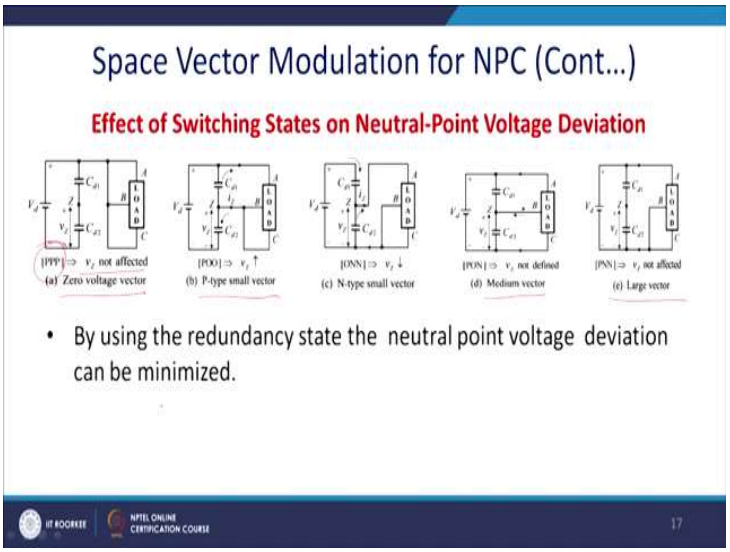

Thus, what happened? These are the options. So, if you have switched PPP all the upper switch is closed. It means that you have v_z and zero voltage vector. Ok? So, you shot all the legs. Same way if you have P00 or POO then what happen? Only one vector gets the voltage others are shorted. So, you got a small vector. Similarly, if you have, you can see that this combination, this is the N type small vectors. That is ONN. So, you can get the same voltage. Similarly, PON, v_z is not defined and it is a medium vector and PNN and it is a large vector.

So, in that way we will be using these vectors and by using the redundancy state, neutral point voltage deviations can be minimized and you can have a redundancy and thus you got more reliability into the system.

Thank you for your attention. Thus, I complete the multi-level inverter and its PWM techniques and that will help you to deduce the drive application mainly, as well as when you connect to the UPQC or the shunt active power filter. This kind of techniques are used to mitigate the voltage and the current harmonics.

Thank you.