Power Quality Improvement Technique
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Lecture – 21
Multi Level Inverter- II

Welcome to our NPTEL lectures on the Power Quality Improvement Technique. This is going to be our second lecture in the Multilevel Inverter. We had discussed about the diode clamp multilevel inverter. We are going to discuss now the capacitor clamp multi-level inverter. So, this is the capacitor clamp as you have seen that, but there is a change in the topologies and component count is also less.

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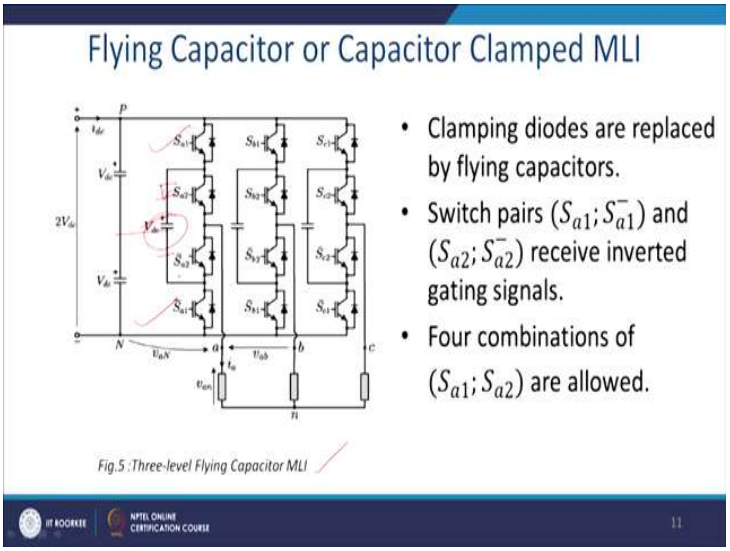

You had two diodes connected in this fashion from this anti-parallel. Mostly you have a diode here and you have a diode here and this is also a diode and you have connected here. So, you have two diodes instead of that you have only one capacitor and thus component count is one of the biggest advantages here. So, you have a least component count. Number of diodes goes abysmally high in case of the diode clamp multilevel inverter if you go for more than 5 or 6 level.

For this reason, we look for the different multilevel solution and that is the capacitor clamp and here there is a little change in the logic. Generally, we have seen that this S_1 and this

one is complementary and this S_2 and this one is complementary. Here you will find this switch and this switch is complementary and this switch and this is complementary.

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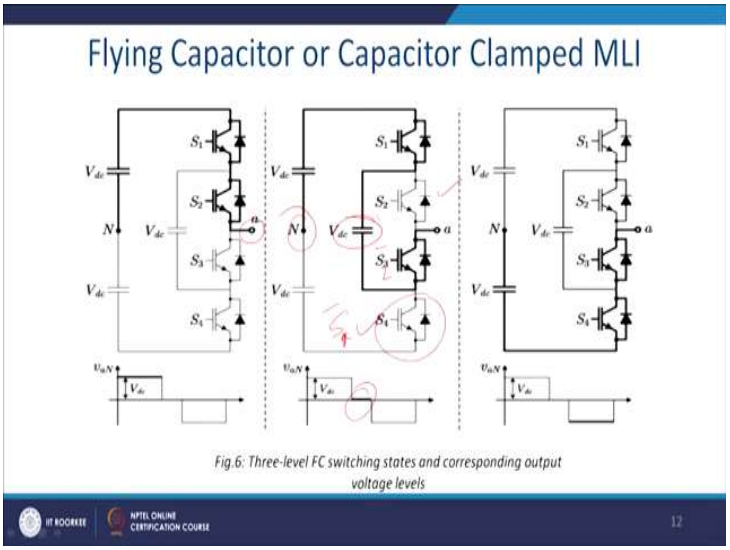

So, let us see how does it work? Here upper one is same. There is no difference here. You apply S_1 and S_2 which should be closed and you get the value of the V_{dc}. So, this is the same as the diode clamp inverter. But there is a change in the switching while you want to get '0' voltage or the neutral voltage at the pole of the inverter. Then you will connect S_1 and S_3 as you have seen. These two switches will be complementary and thus there is no cause of this should be acting. Thus, what happened? You know, ultimately all the voltage will be taken by this capacitor. So, this voltage become V_{dc} and thus what essential you get is a '0' voltage.

Similarly, so you get a '0' voltage here and you can generate the '0' voltage also there. This is a redundancy, through S_4 and S_2. Same thing here, this switch will be on and there after this voltage will come and this. So, there is a redundancy thus you can generate this voltage by combination of S_1, S_3 or S_4, S_2. Where generally S_4 is nothing but is S_1 prime you can also write and you can write also it is as S_2.

This one is same. There is no difference between these two. You required to switch it on, then you have to switch it on S_3 and S_4 and you get minus V_{dc}. So, one of the advantages is that component count is less. You generally made it with the two diodes. Here you have

no diodes. Only one capacitor and you want a controlled voltage across it. That is one of the challenges. Otherwise its works fine.

You also have a redundancy. So, you can generate and you can reduce the switching losses by the one-bit change. Thus, you can generate this '0' voltage by combination of S_1 and S_2 prime or S_3 or S_2 or S_1 prime or S_2, S_4. So. All of it is possible to derive in case of this flying capacitor.

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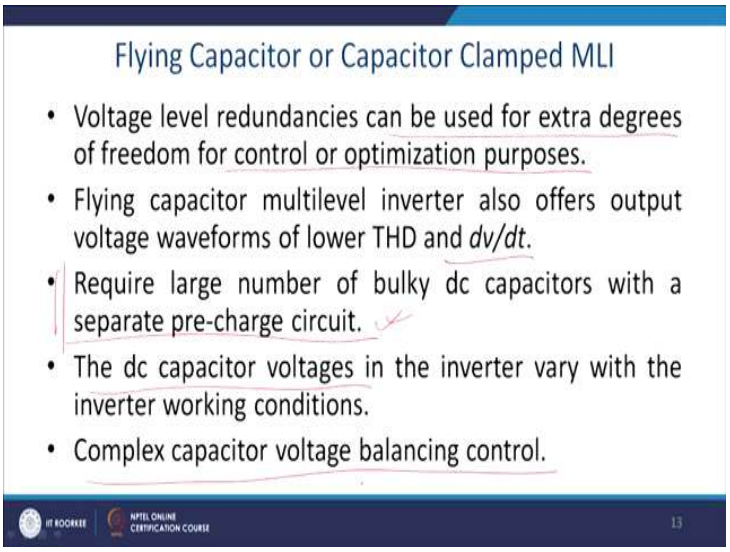

So, what does it say about us? The voltage level redundancy can be used for the extra degrees of the freedom. That is what we have discussed here? To control and for optimization purpose, because you can reduce the switching losses with these redundancies, and also the redundancy gives you more reliability. If some where some switches are not working, you can bypass and still can function very well.

Flying capacitor multilevel inverter also offers output voltage waveform lower THD and dv/dt. It is same as your diode clamp inverter. One of the major disadvantages is that it requires large number of the bulky dc capacitor with a separate pre-charging unit. So, that is something you required to have a V_{dc} that comes into the pictures. You required to always maintain that voltage. So that after some interval of time capacitor always have a weakest link into the component count.

Generally, longevity of this capacitor is least compared to the other devices and for this reason we sometime find it difficult in terms of its min breakdown time and also reliability. The dc capacitor voltage in the inverter vary with the inverter working conditions. Sometime current goes out and sometime current sink into it. You assume that capacitor voltage is also constant, that is also not so and thus you required to have a balancing network. For this reason, we say that complex capacitor voltage balancing is required to control this flying capacitor MLI.

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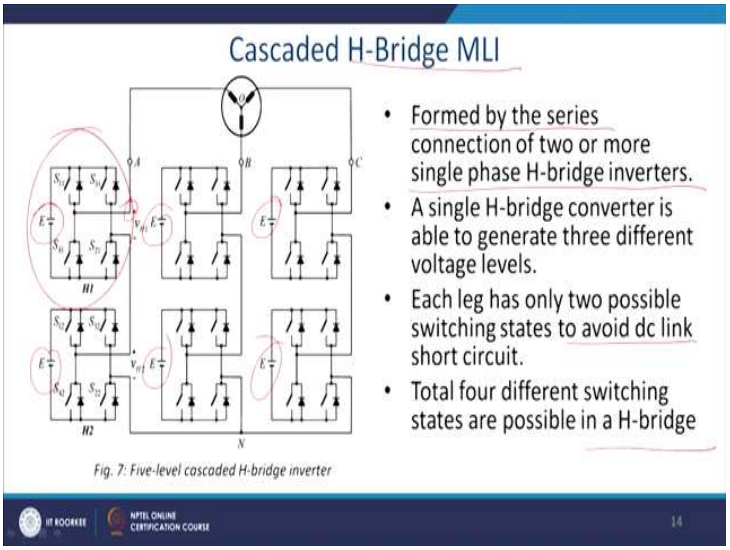

Now, let us go to the cascade H-bridge MLI. One of the advantages of it is that you got blocks. You just put a block and it becomes a functional purpose. So, for the 5-level you can have this 'E' and 'E' that constitute the phase 'A'. Similarly, this will constitute phase 'B' and this constitute phase 'C'.

If you see that number of switches in the 5-level, it is so this is 8 switches per phase you require. Hence, you require the 24 switches. Otherwise you do not require generally anti-parallel diode as it comes with the switches. You need not have to connect any extra anti-parallel diode and also the capacitor. I shall list out the component count after discussions of all this inverter topologies.

Let us see that. This 'E', all those voltages are equal. We are assuming to be so, but it may not be equal. You can change it and another problem is that we required to provide isolated voltage source for each of this block or the H-bridge. So, we can say that it is formed by

the series connections of two or more single phase H-bridge inverter, a single H-bridge or converter. Whatever may be.

The single H-bridge converter is able to generate 3 different level of voltages. Once you switch it on, this voltage and this voltage you generate. If you switch it on this and this, you get a voltage. If you switch it on these two voltages at this point, you get a '0' voltage. Thus, you get a three-level of voltage.

Same for it. The combination makes you the 5-levels. Each leg has only two possible switching states to avoid for dc link short circuit. Total four different switching states are possible in a H-bridge. Just as I show in the next slide.

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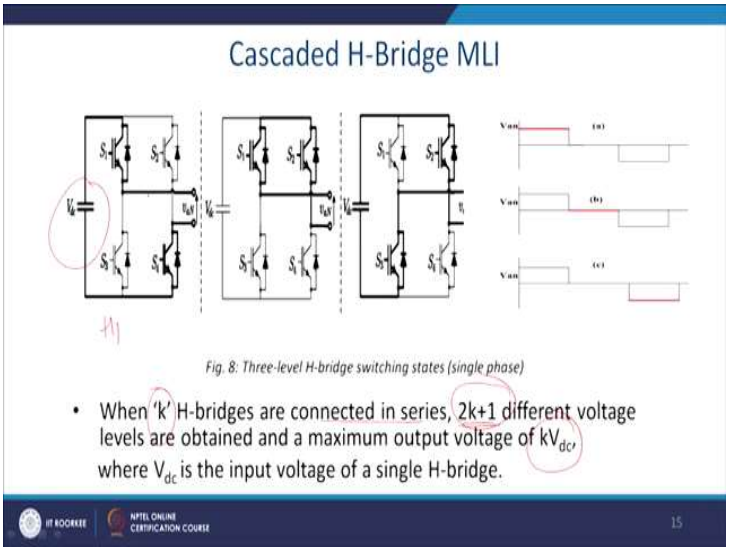

See that this is for one H-bridge one let us say. You can switch it on and thus what happen? You get a Van. You can switch on this two. Ultimately, you can get the '0' voltage and then we can switch on this. You get a negative voltage. Where 'k' is the connected level of the bridges and you will generate $k + 1$. So, you have a two such H-bridge in phase, so $2k + 1$ that is essentially 5-level.

Different voltages are obtained and the maximum output voltage will be $k \times Vdc$. So, you got $Vdc + 2Vdc$. Where V_{dc} is the input voltage of the single bridge and voltage stress across the individual device will be $Vdc/2$. That is also a very big advantage in terms of the bomb cost.

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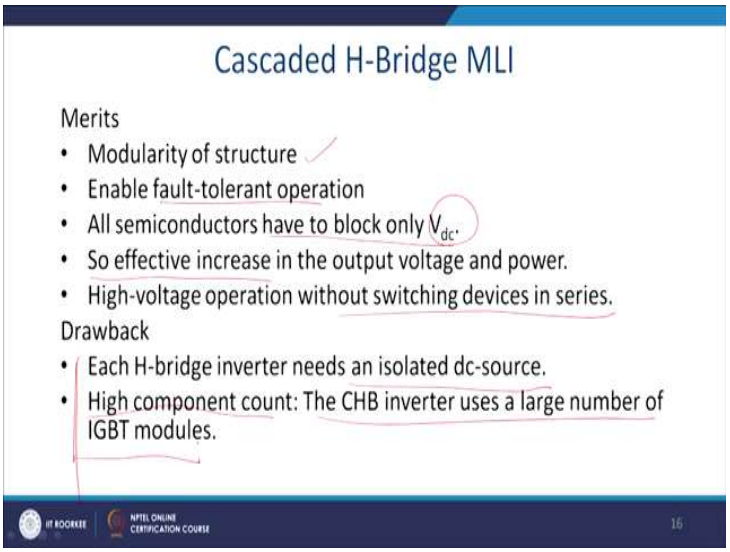

So, what is the advantage of it? Advantage is that it is modulus structures. So, you just put them like a brick and build a house. Enable the fault tolerant operation. We can show that the redundancy is more, because different voltage level can be generated with few more combinations.

All the semiconductor only blocks the voltage level of V_{dc}. So, effective output voltage is increase and power level can be enhanced and if you put the more bricks you can increase the voltage rating. High-voltage operation without switching device in series. But drawbacks are each H-bridge inverter needs an isolated dc source and high component count. CHB inverter uses large number of IGBT modules. These are the few disadvantage of this proposed H-bridge MLI. So, how does it generate? Let us see.

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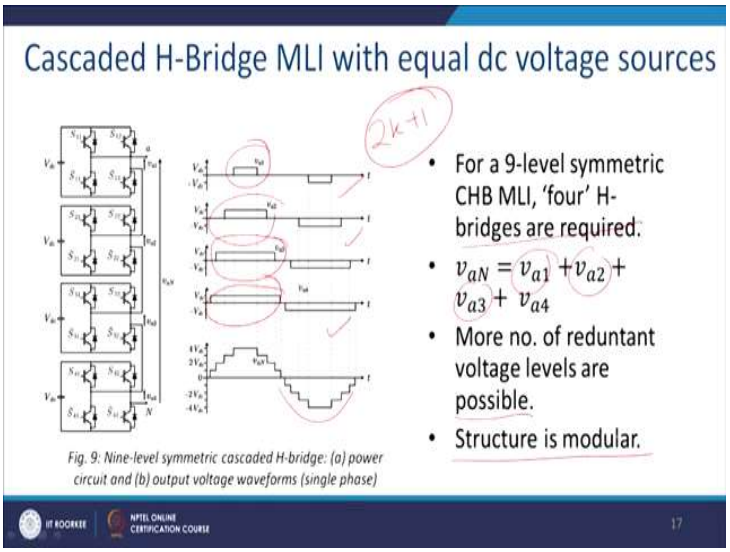

It is a 9-level. If you want that this switch and this switch to be on, (let us say that it is generating v_{a1}) you just spread it over little bit and you generate v_{a2} same way. Similarly, you get a v_{a3} and v_{a4}. You add them. So, you get a staircase kind of waveform and same way for the negative half cycle and thus you also get a stair way kind of waveform and it is quite close to the sign wave.

For 9-level we require four bridges, because it is $2k + 1$. For 9-level symmetric H-bridge MLI. This is Multi Level Inverter four bridges are required. Ultimately v_{a1}, v_{a2}, v_{a3}, v_{a4} these are the all switches, more the number of the redundant voltage levels are possible and the structures is modular. If you want something instead of the eleven-level you just connect another bridge, you get eleven-level.

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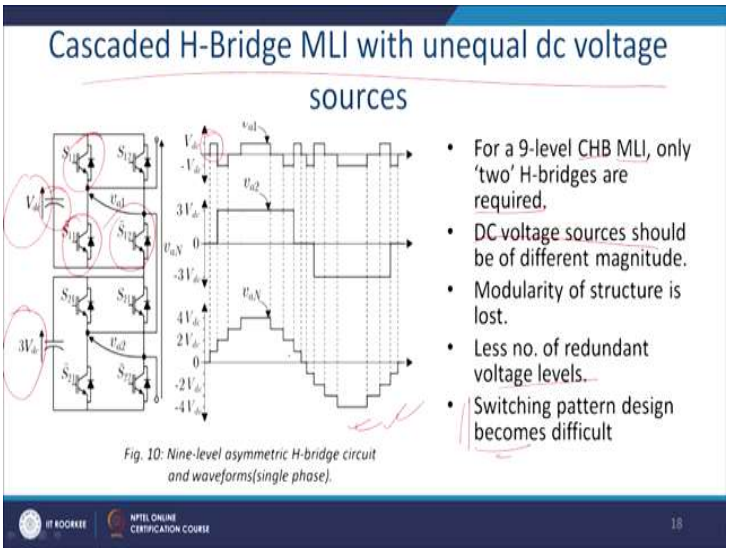

Now, there is another way to do it. This is called the cascade H-bridge MLI with the unequal voltage and that also help you to shape out some kind steps. So, see the beauty of it.

So, this can be upper one. Thereafter once you on it, you get some voltage. This voltage is one-third of this voltage. It is quite easy to do and it has a huge application in solar inverter topologies and nowadays as I told you. Now we will integrate the power quality problem with the renewable energy in a micro grid.

Since shunt active power filter. It can be a shunt active power filter. If you connect, you can keep this capacitor voltage to that level by actively controlling it, in case of the shunt active power filter. You can do it also by putting the solar panel. You can put the one panel or you can put the 3 panel. Thus, you can say that you have a great merit on it.

So, you see that how you generate a different level by just with the 8 switches. That is the beauty of this, unequal dc voltage, but it has to be separate. So, you give a negative peak you get the positive, you give a negative you get a positive and thus you generate this square wave.

So, what should be the level of the voltage? Then optimization is also a scope of the research and you find plenty of research paper on it. For the 9-level CHB MLI only two H-bridge are required. That is the beauty of it.

So, dc voltage source should be of different magnitude. That is a challenge, but for solar it is not a challenge. Modularity of structures is lost. That is one of the disadvantages. If you want to have another voltage, you have to put in a dc bus level and generally this device rating also will be a different, because you do not want the same kind of switch the voltage to stay across this is a $3V_{dc}$. Here it is only V_{dc}.

Loss in redundant voltage level and switching pattern is quite complicated. But with the help of this modern control circuit like a FPGA based systems where implementing algorithm is quite easy, it is easily possible. That is the one of the areas of the research. With lesser number of cascade H-bridge, you can generate multi-level. You can generate different level of the inverter.

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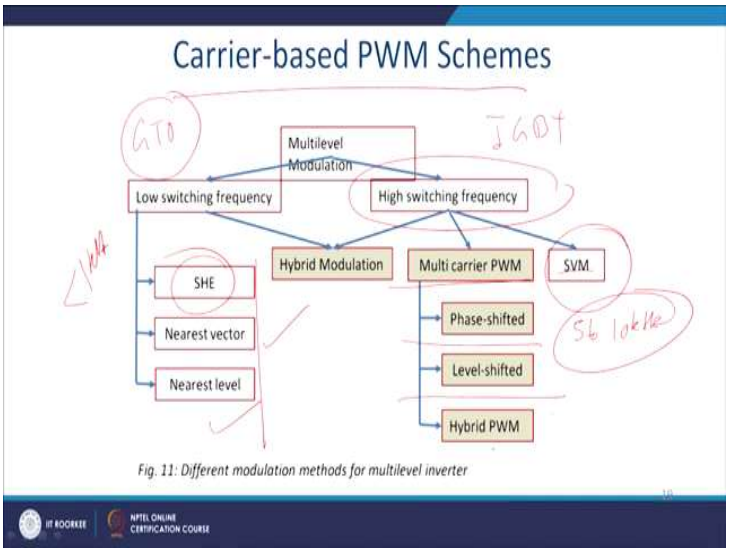

Fig. 11: Different modulation methods for multilevel inverter

So, now let us invest our time on the PWM technique, that is suitable for your multilevel inverter. So, multilevel inverter modulation can be broadly classified like this. If you are using, selective harmonic elimination, we have discussed that already.

If you are using GTO for the higher rating, then we prefer low switching schemes and for the higher switching frequency, IGBT is been used. You can go for this method. So, this is selective harmonic eliminations, generally it is sub 1 kilo hertz frequency and here the frequency range is 5 to 10 kilo hertz.

So, you got a SHE. Thereafter nearest vector. There after nearest level shifting. These are the few technique. With the sake of time we may not be able to discuss all those methods and we can combine. It is high frequency that is called hybrid modulations. Thereafter we can have a multi carrier PWM. We have discussed this space vector modulation. We are touched upon for the 3-level inverter. Students are requested to go through those lectures again. Then phase-shifted PWM carrier, level-shifted PWM carrier and mixing this with it, you got a hybrid PWM carrier.

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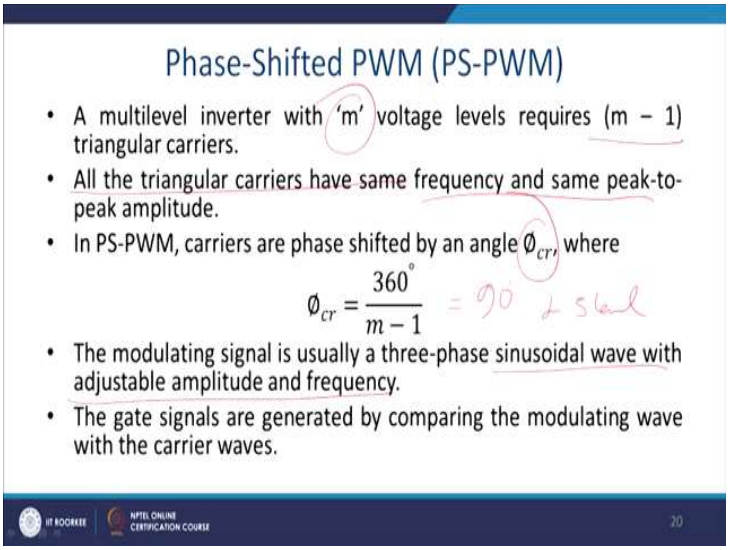

Now, first let us take a phase shifted PWM carrier. If you have a multilevel inverter with 'm' voltage level, it requires $m - 1$ carrier. For 3 level you require 2 carrier. For 5 level you got to have a 4 carrier. All the triangle carriers have frequency and same peak amplitude and generally they have been phase shifted.

In phase shifted PWM carrier, the phase shift is by the ϕ_{cr}, where $\Phi_{cr} = \frac{360^{o}}{m-1}$. So, for the 5-level you can have a 90 degree, because 'm' equal to five. So, m minus 1. It gives you a 90-degree phase shift for 5-level. Modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and the frequency. We can see that in the next slide later. The gate signal is generated by comparing modulating wave with the carrier wave.

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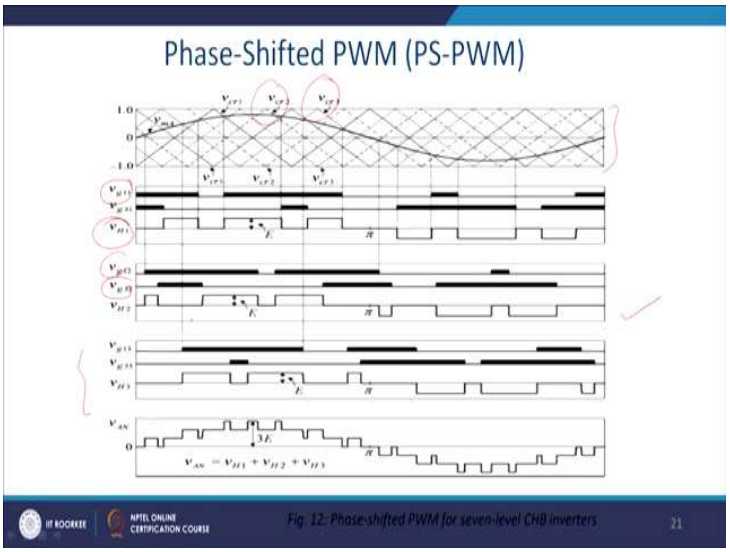

So, this is the waveform where these dotted lines are the carrier. This one is a first carrier wave, there after you will have another carrier wave by some phase shift and this is the 90 degree phase shift. So, you will generate four carrier wave and this is a carrier wave 1, this is carrier wave 2, this is carrier wave 3 and this is the carrier modulating wave.

So, now they are 120-degree phase shifted here, since we have a three-carrier wave. So, you will generate this pulse once logic is pretty simple. When this modulating signal is more than the carrier wave you will be on. Thus, you get v_{g1}, for this purpose and it will be on till this time and here cross over occurs and ultimately this will be the pulses for the first H-bridge converter.

Similarly, this is the carrier wave for the v_{g1} and the v_{g2} and that is coming from this place and this is the v_{g3}. So, ultimately, you will generate this voltage as in the second cascade H-bridge. Similarly, for the third carrier wave you just compare and you will generate the third carrier wave signals. I request you to simulate this circuit, these logics, then only you can generate the gating signals very easily. Thus, you will get these voltages ultimately, v_{AN} will be 3V. It is v_{H1}, v_{H2}, v_{H3}. So, this is the voltage level you will get.

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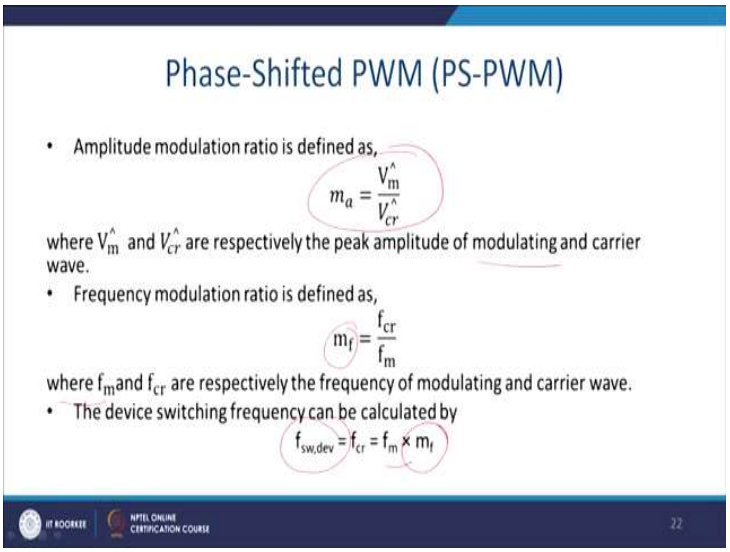

So, amplitude, as we have studied your PWM technique from the power electronics courses. So, nothing new here. Amplitude of the modulation ratio is defined by m_a that is $\frac{V_m}{V_{cr}}$. Where V_m and 'Vcr' are respectively the peak amplitude of the modulating and the carrier wave.

The frequency modulation ratio is defined as $m_f = \frac{f_{cr}}{f_m}$. Where f_m and f_{cr} are respectively the frequency of the modulating and the carrier wave. The device switching frequency can be calculated '$f_{sw,dev}$' equal to the carrier wave frequency equal to a modulating frequency into m_f. Generally, it has to be the multiple of it otherwise intra harmonic will come. For this reason we required to avoid that.

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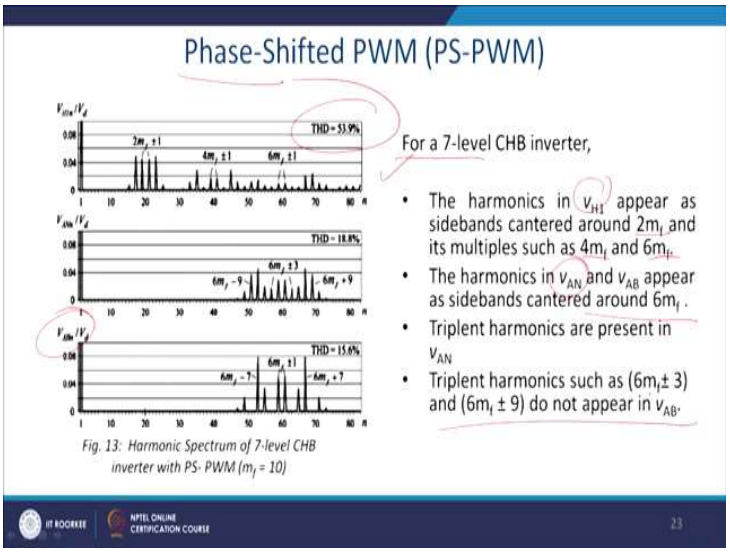

Fig. 13: Harmonic Spectrum of 7-level CHB inverter with PS- PWM (m_f = 10)

For this it is a spectrum for the phase-shifted PWM. There after we will take out the level-shifted PWM. This is for the 7-level cascade H-bridge converter or inverter. The harmonics in v_{H1} appears the side band containing $2m_f$ and multiple of 4 m_f, 6 m_f and so on. This is the case.

You can see that voltage harmonic is as high as 53 percent. Thereafter if you feed it to the machines, the machine longevity will be one-third. The harmonics in v_{AN} and v_{AB}, that is the phase voltage and this is a line voltage appear the side band, in an around that in 6 m_f. So, this is the case here.

Triplet harmonic such as $6mf + 3$, and does not appear in 'AB'. Thus, it has a scope to inject, third harmonic for better utilizations of the dc bus voltage for the drive applications. So, this is some observation, we can make in case of the phase-shifted PWM.

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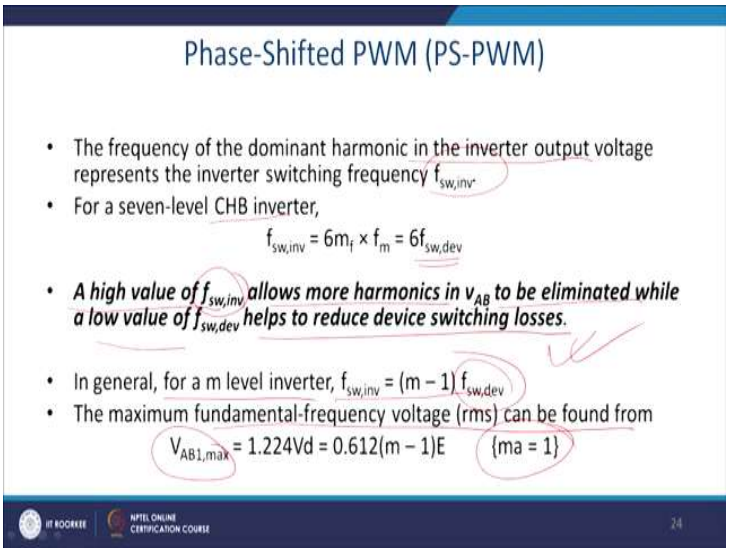

Now, the frequency of the dominant harmonics in the inverter output voltage represents the inverter switching frequency that is the 5 kilo hertz or 10 kilo hertz whatever may be. For the seven-level CHB, you will shift it 6 times. So, it will be 6 m_f into m_f that will be 6f. So, that is the advantage of it. So, effectively you are switching 2 kilo hertz and effectively your side band lies at 12 kilo hertz and you required to design the filter at 12 kilo hertz and thus size of the filter get reduced.

So, we can conclude one of the basic advantages of it is high value of switching frequency allows more harmonics in 'V_{AB}' to be eliminated, while low value of switching frequency helps you to reduce the device switching losses. So, once you are switching at less frequency your switching losses are less but your voltage has higher spectrum. 6 times more. So, what essentially you required to use is a lower filter size and this one is of the greatest merit for this cascade H-bridge multilevel inverter fitted with the phase-shifted PWM. So, it is just like made for each other.

In general for a 'm' level inverter switching frequency is the something that we required to use it frequently. Switching frequency inverter equal to $m - 1$ into switching frequency of the devices. So, this switching frequency of devices is quite low. If you have a 9-level, then it is 8 times and the maximum fundamental frequency voltage rms can be found from $V_{A1,max}$ which is equal to 1.224 into Vd that is 0.162 m into E. And the maximum value of

that carrier wave magnitude equal to the modulating wave amplitude. So, that will be equal to 1. Then in that case, you can get this magnitude of the voltage and that is quite high.

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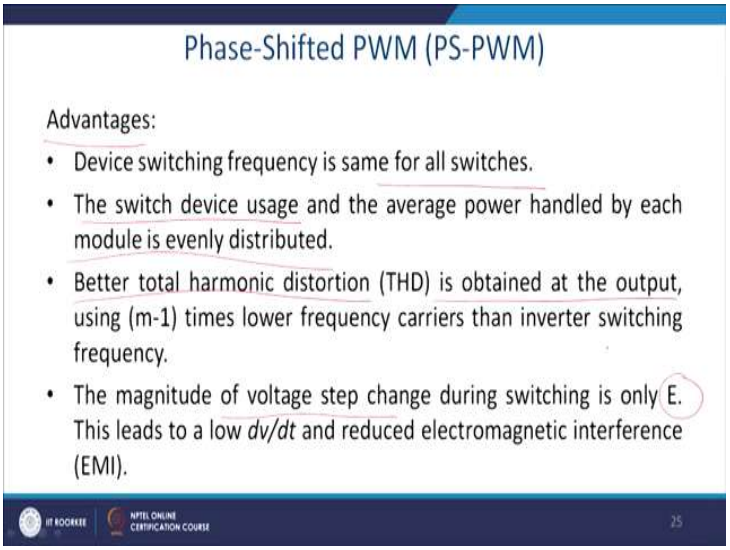

Thus, we required to conclude the advantage of the phase-shifted PWM for the multilevel inverter. Device switching frequency is same for the all switches. So, you can take the same kind of device. Otherwise if some switches have a more switching frequency and some switches will have less switching frequency, as you ever seen in case of the different level of the cascade voltage. 3 Vnb is switching very frequently the lower voltage.

It is switching quite less. But that is very good combination you know IGBT and the GTO combination makes it happens. So, that is the one of the better optimizations. So, we can play around. The switch devices usage and the average power handled by each module are evenly distributed and thus losses also evenly distributed and the design of the heat sinks becomes simpler.

Better Total Harmonic Distortion or THD is obtained at the output using $m - 1$ times lower frequency carrier than the inverter switching frequency. The magnitude of voltage steps change during switching is only 'E'. This leads to low dv/dt and reduces the electromagnetic interference. So, these are the major advantage.

Thank you for your attention, I shall continue our discussions on the multilevel inverter in our next class also. Thereafter we shall discuss about different kind of technique. Thereafter level shifted technique will also be discussed.

Thank you.