Power Quality Improvement Technique Prof. Avik Bhattacharya Department of Electrical Engineering Indian Institute of Technology, Roorkee

# Lecture – 15 PWM Rectifier – III

Welcome to our NPTEL courses on Power Quality Improvement Technique. Today we are continuing with the PWM Rectifier, that will be our 3rd lecture for single phase. We will start from where we have left in our previous class which is current control wave form. As you have seen there is a inner current control loop that will be fast in response and there is an outer voltage control loop that will be a slower response and this implementation is easier for this boost converter.

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Control of the Current Waveform (Cont) Quasi-static approximation: discussion In the literature, several authors have reported success using this method
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Such behavior can be observed in rectifier systems. Worst case analysis to prove stability should employ simulations.
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So, if you study little bit of literatures, you will find that several authors had reported several methods for the current control technique. So, we are required to check that what is the best solution or optimal solution for our design. So, for this reason we should put some constraint to evaluate what is the best method of the current control.

So, we should validate provided the converter dynamics are sufficiently fast. That is one of the requirements. That it required to be sufficiently fast. So, that it can response fast in change of load or other dynamics, such that the convertor always operates near the assumed operating points. Because that is where you have the stability.

Another condition you required to find which is no good condition on system parameters, which can justify the approximation, is presently known for the basic converter topology. It is well understood in the field of the control system that, when converter dynamics are not sufficiently fast, then the quasi static approximation yields neither necessary or the sufficient condition for the stability.

So, what I want to say? Why it is you have to understand it? Let us say you have designed a buck converter or boost converter with MOSFET. We were switching at frequency 20 kilo Hertz. Because of the higher power rating you want to design the same entity buck converter or boost converter, generally boost converter. As I discussed previously, it is easier to implement. You want to make it with the GTO. Thus, what happen? Instead of 20 kilo Watt you required to operate sub kilo Hertz level, maybe 500 Hertz.

So, then what was stable there. it would not be any more. But you have changed the value of the inductor accordingly and all those constrains have been maintain, but the quasistatic analysis may not be sufficient for the slow behavior. Such behavior can be observed in the rectifier system. Worst case analysis proves stability and should be employed for the simulation in this case, to check that whether it perform best in terms of the simulation term. It will be called as Monte Carlo condition.





Now, let us see the same boost converter. How it can be worked in a current control mode or current program control? So, this is your voltage we assume, but this voltage maybe like this and the current also will be like this. So, that it does not have a reflection of it into the ac side.

So, what happened? What you will do? But our discussions will be constrained within this part. So, this is the value of the inductor and it is to be chosen above the critical conduction mode. So, you sense this inductor current and ultimately you know that when it will switch on. Hence the inductor current will ramp on.

Thus, what happened? You have a  $v_{control}$  and from there you will multiply. It is generally of sinusoidal fashion of the double frequency oscillations. So, you multiply it and thus you get some constant  $v_g$  into  $v_{control}$ , where  $v_{control}$  comes from the output as well as the sag or the swell.

So, then what happens? You know you asked to ramp on till you know that there is a highest boosting rate. So, for this reason your duty cycle is fixed to some limit. So, for this reason this ramp will be compared with the clock.

So, as long as clock is high, you will get an output here and ultimately you will map with it. The moment current value goes above this, within the clock fear of time, goes above this, it will reset. Otherwise clock will drive the MOSFET or the IGBT depending on the rating of the device and it will be a current control mode.

So, you are controlling the ramp. Once it crosses within the limit you will turn off the switch. Thus, what we can say that, current program control is a natural approach to obtained because it had an inherent short circuit protection. You would not allow current to be very high. Obtain input resistor emulation.

Ultimately it will emulate it, because you know this is your voltage and this is your current and ultimately, they are in the same phase. Thus, you are emulating this pattern. The peak transistor current program to follow the input voltage. Generally, it will have a double frequency oscillation. Thus, what happened? Before rectification there is no distortion and also have less THD.

So, peak transistor current. Peak transistor current defers from the average inductor current, because of the inductor current ripple and the artificial ramp. This is the artificial ramp you will generate from the clock by means of the integration.

This leads to the significant input current wave form distortion. This is one of the problems. Because it may not match with the ramp. Because you are integrating this. So, you wanted to basically control the rate of change of the current into the inductor and it has to match it. So, you can be programming like this. So, this is one way of controlling. This is called a current program control.

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And it has one of the advantages for static input. So, it is  $i_gTs$ . If you are working on a discontinuous conduction mode it is quite challenging to operate. So, it will be  $v_g(t) \frac{Li^2_c(t)f_s}{(V-v_g(t))(v_g(t)-m_aL)}$  in DCM. But this equations in the CCM will be very much simplified, that is  $i_c(t) - (1 - \frac{v_g(t)}{V})(\frac{v_g(t)}{L} + m_a)T_s$ .

So, what we can say that, at the boundary condition when transition occurs to CCM to DCM, then  $\langle i_g(t) \rangle_{T_s}$  has to follow this logic. If it is equal then it is, in boundary condition if it is more than it is in CCM. So,  $\frac{T_s V}{2L} \frac{v_g(t)}{V} (1 - \frac{v_g(t)}{V})$  or  $i_c(t) = \frac{T_s V}{L} (\frac{m_a L}{V} + \frac{v_g(t)}{V}) (1 - \frac{v_g(t)}{V})$ .

So, it is desired that  $i_c(t) = \frac{v_g(t)}{R_e}$ . So, minimum slope compensations  $(m_a)$  we want to be  $\frac{V}{2L}$ . So, this is the slope that you will get. So, you want to have a slope compensation, you

act on a slope. Thus, this method is quite fast than your current mode different current mode control.

The static input characteristics of this current programming mode boost converter, we can see that these effective resistances become  $\frac{2L}{T_s}$  which is your base resistance and you can see that how it will be changing this value.

So, when duty cycle is this ratio  $\frac{v_g}{v}$  then this is the your current  $i_g$ . So, if you see that if this ratio is less, you know till this is the envelope of the CCM and the DCM, below it will be DCM after that, you will have the 0.1 of the base value. Gradually you know at this point around 2, you will have this is to be the base value and thereafter base value will increase.

So, you can control the equivalent resistance of the circuit. But you see that if you want to operate at higher resistance that means at the no load then your DCM is quite large. So, for this reason you know that control will fail.

But whereas, if you try to highly load this device or you load close to your base resistance, then their DCM values is optimal. This is the DCM value. After that you can see that, the range of the DCM increases. So, it is a challenge to operate this PFC. We call it Power Factor Connection in a no-load condition, for this the discontinuous operation.



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So, let us see that. We have considered that  $i_g$  by i Peak as a normalized value. So, input current waveform with the current mode control with respect to the omega, this will be sinusoid and it will be close to sinusoid if  $R_e = 0.1$ . Then gradually it will start to be peaky 0.33 and you can see like this. Once this happened to 10 times, you can understand that there will be a quite peaky current.

So, a substantial distortion will occur in a waveform if you have a higher base resistance. It can meet the harmonic limit, if range of the operating points are not too large. That is a condition.

So, you can see that you are operated for this R. If it is more than R, then you will find that peaky kind of transition and THD will not be fulfilled by any of the standard. So, for this reason we say that, it is difficult to meet the harmonic limits in a universal input supply. So, you required to redesign the circuit. Mostly we change the switching frequency. That is something in your hand, because switches are costly. But if you change the network then chip gives the provision to set the switching frequency.

Then what do we do? You know this is the Ts, Ts is the switching frequency. So, we have to play around with the Ts, so that you can keep it close to the sin envelope.



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So, how to do that? This is the hysteresis control and as I told you U C 38, 54, 55, 56 belonged to this category. The critical conduction mode and it is the hysteresis control. Ultimately you got  $v_g$ .

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And you will generate the cost and hysteresis band while discussing the PWM technique. I have discussed in detail about the hysteresis. So, this will be the hysteresis band.

And this current is required to be restricted. Green one is this current. So, what happens? You know, you got an inductor thereafter you have switch. So, you start from this point, crosses your value of  $v_g$  then it will touch this upper envelope and thus switch will open up. Previously till this point to this point switch was closed. Then automatically the current will discharge and assuming that it is a continuous connection mode. So, current will fall here.

Again, once it will heat the lower limit. Again, the switch  $T_1$  will be closed and this ramp will be repeated. So, this ramp is basically the  $m_a$ . Ok? So, in that way this chip will work. So, this is the case of the hysteresis controller.

And there is a one chip FAN 562 that is for the Fairchild chip. So, this will have a different mode of conduction. Generally, it will be 'on' considering the voltage level of the  $v_g$ . So, let us go back and understand it. What does it mean by that?

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So, what happens? You have this voltage  $v_g$  and current  $i_g$  which will be ramping on still it touch this value. Then it will be off and then it will again touch this value. It will be off and again touch this value, it will off. So, what happened here? You need not have to get the input. You need not have to sense this current and ultimately you got a petal like wave form and you filter it out.

But here filter is a challenge you required to have this petal kind of wave form. Thus, petal kind of wave form will essentially replicate this sinusoidal wave form. This one. This is the way it will work. So, ultimately it will filter. Ultimately your input current will be chopped like this. As an Australian Sydney opera or something like that. So, you will get like this.

So, this is the way of conduction. And what happened here? You required to have this mode. Because you can see that inductor current which you have to follow and track. Mostly it works in a continuous conduction mode. But here you can go till discontinuous conduction mode and it can operate in a discontinuous conduction mode for the lower load. So, if we have a lower load this mode is preferred. For the higher load this mode is preferred.

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So, let us implement it into the practical circuit. So, you got an EMI, EMC filter x and y. There is a differential mode filter and the common mode filter. I have not shown it in detail. This is a practical circuit. Of course, there will be an anti-parallel diode.

So, ultimately you have this  $v_g$  here and from there you will sense  $v_g$ . And you should have a  $v_{control}$ .  $v_{control}$  is something that we will take care of whether there is a voltage sag or swell anything. That we multiply and ultimately you will get  $v_r$ . Once you multiply you can say that  $v_r(t) = k_x v_g(t) v_{control}(t)$ .

Thereafter what happened? You will sense the current and you will emulate the resistance Rs by the PI controller mostly and you will compare it. Thereafter if this multiplications of the iL into Rs is more than the drop, then you are going to reset this flip flop. Otherwise there will be a zero-crossing detector. In zero crossing detector you will start every cycle and it will be stopped till input of this Op-amp input is higher than 0.3 and when it is higher than the input of the that Op-amp 0.2, you are going to reset.

This is a buffer you know. Why? Because it can be, you can easily implement this circuit. Of course, the chip is available to you by discrete components. You know this is the unity feedback Op-amp, voltage follower. And of course, you are going to give a resistance to it. Whereas, you required to sink a certain amount of the current. That has to be provided by the buffer, because these devices cannot provide this much of this thing. Ultimately if you see that you are not here then there is a clock. It is synchronous. Generally, what happened? Here it has been reset at every zero crossing. So, it can run in an asynchronous mode also. That is also the added feature to this circuit.

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So, what are the advantage and disadvantages of this critical conduction mode control? One aspect is that nowadays it is quite cheap. Then also simple, low cost controller for ICs. So, we can fabricate the ICs and it is already available for past I think 15 years. So, you can make those easily. Low frequency harmonics are small, with constant transistor on time for the boost converter. So, it can be eliminated. Since you can operate it in to discontinuous conduction mode, size of the inductor is quite less.

But however, you will increase the peak current. You have a petal kind of wave form. So, there is an increase in the peak current and thus EMI, EMC will be more. For this reason we have put that. It is something like to stop the bleeding. We put some EMI, EMC condition. But where there is a stringent EMI, EMC requirement, this kind of design may not be satisfying. For your designing purpose, we required to have a different design procedure. We may require to have a soft switching also for that reason.

So, increased conduction loss, reduced switching loss, because number of switching is less. If you compare this method, here switching is quite high but whereas here switching is less. But if switching is less then switches are operated at a longer duration. So, conduction loss required to be higher. But MOSFETs generally have lower conduction loss and the higher switching loss and for this reason it is been preferred.

However, this requires larger input filters as well, because you know this will be reflected in ac side. AC is your input. Thus, it has to make a sinusoidal and thus you required to have a large input filter. Thereafter variable switching frequency smear out the EMI current. So, once you have a high dv/dt and you also got di/dt with this interference of the both, EMI will be produced and spectrum cannot synchronize the converter switching frequency. You will find some awkward spectrum. That is also coming due to the variable switching frequency.

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But anyway, we use it very frequently. Transistors is on for the fixed time t<sub>on</sub>. Generally, it is a constant t<sub>on</sub> operation. And transistors are off when inductor current reaches to zero, so you are always in a critical conduction mode. So,  $\frac{v_g(t)}{i_g(t)} = R_e = \frac{2L}{t_{on}}$ .

On time is a function of the load because you have to ramp on and thus, we can calculate the value of the inductor by the inductor voltage balance method. So, charge should not be stored into the inductor. So,  $v_g t_{on} + (v_g - V)t_{off} = 0$ . If you solve it for  $t_{off}$  then  $t_{off} = t_{on} \frac{v_g}{(v-v_g)}$  that is what we want, a symmetrical triangle.

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We can solve for how the controller varies from the switching frequency. So,  $T_s = \frac{4LP}{V^2_M} \frac{1}{\left(1 - \frac{v_g(t)}{V}\right)}$ . Thus, you can change this switching frequency if required to make it a fast and low depending on the resistance.

For sinusoidal line voltage variations switching frequency we assume that with respect to this. We can consider that since it is a 50 Hertz and the switching frequency is maybe you can put it. It will be in a kilo Hertz. With respect to this switching frequency with respect to this particular operating point, we can consider that this  $v_g$  is almost constant. That is our approximation.

So, it is a quasi-static process. So, though 50 Hertz is for us it is quite fast but with respect to the switching frequency it is quasi-static process. Thus, for the sinusoidal line voltage variations, the switching frequency therefore, will be varies as follows:  $\frac{1}{T_{r}} =$ 

$$\frac{\frac{V^2}{M}}{4L}\Big(1-\frac{V_M}{V}[\sin(\omega t)]\Big).$$

So, there will be a little variation of this switching frequency because of the slowly varying voltage. You may fit it to these applications in avionics. Avionics generally require a 400 Hertz supply. So, there also you can fit it and it will work.

The minimum and the maximum limit of the switching frequency thus you can calculate. That is maximum  $f_s = \frac{V^2 M}{4LP}$  and minimum will be  $f_s = \frac{V^2 M}{4LP} \left(1 - \frac{V_M}{V}\right)$ . This equation can be used for selecting inductor value of L.

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Now let us come to the control part of it. We have said that it is a quasi static process, so we can apply the linear control and we can get a satisfactory result. But how much it is acceptable? So, it can attain the simple control of input current wave form without sensing the ac input voltage. This is one of the merits of previous method, which is petals method. So, petals method does not require to sense the actual voltage and operates with the continuous conduction. So, as it will charge the petal always, it is always a continuous conduction mode.

The integrals of the sensed switch current (the charge) is compared with the carrier wave. That is a non-linear carrier wave because of this modulation in a cycles by cycles basis. So, every cycle it will be controlled. Carrier waveform depends on the converter topology. Our discussion is totally dependent on the boost converter and that is the simplest. You can carry on this for the buck and other as well. You will find a lot of difficultly. Very low harmonics in CCM and wave distortion in DCM occurs. So, we want to operate this in CCM. Peak current mode control is also possible with a different carrier. That also gives you the steady state stability. (Refer Slide Time: 30:31)



Here this is the inductor. This is non-linear. This is a control block diagram or non-linear carrier chest control of the boost converter. This is  $i_s$ . This is a current through the inductor, and this is  $v_c$ , and this is  $v_i$ . You can see that you sense the current, thereafter by the coupling inductor so it will be reflected to you and ultimately there is a switch. Switch can be on & off.

So, you will be shorting the capacitor once this output voltage goes high. Otherwise it will be off. So, this will go to the  $v_i$ . So,  $v_i$  will be charging because of this capacitor and you will compare with this  $v_g$ . That is the control waveform  $v_c$  and you will compare it. Once this  $v_g$  by  $v_c$  will be reached, you will have a turn on. So, you will reset the latch. So, you will be switching on this devices and this is the way it will work.

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So, what can we say? This is an average switch control because of the capacitor and ultimately you can integrate over it. We make the controller to regulate the average switch control by integrating the monitored switching current. Previous one was the peak current. Resetting the integrator to zero at the beginning of each cycle. This is the way you are resetting this integrator by discharging this capacitor every time.

Turning of this transistor when the integrator reaches a reference value. In the controller diagram, the integrator follows this equation:  $v_i(t) = \frac{1}{c_i} \int_0^{dT_s} \frac{i_s(\tau)}{n} d\tau$ . And thus, what happened?  $\frac{\langle i_s \rangle_{T_s}}{nC_i f_s}$  for this discharging operation.

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So, from there you can say that the effective current and becomes  $\langle i_g(t) \rangle_{T_s} = \frac{\langle v_g(t) \rangle_{T_s}}{R_e(v_{control})}$ . We relate this switch control input current assuming that it is CCM. So, it will be  $\langle i_s(t) \rangle_{T_s} = d(t) \langle i_g(t) \rangle_{T_s}$ .

The rate of the input voltage to the output voltage assuming that it is CCM will be  $\langle v_g(t) \rangle_{T_s} = d'(t) \langle v(t) \rangle_{T_s}$ . And thus, we can substitute these equations to find out the average current. That is  $\langle i_s(t) \rangle_{T_s} = d(t)(1-d(t)) \frac{\langle v(t) \rangle_{T_s}}{R_e(v_{control})}$ .

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And from there, whole derivations are there. I wish the student to go through the derivation. So, this is the value of is and thereafter to generate carrier wave these are the equations. So, ultimately 'd' will be replaced by t/Ts. If you replace then  $v_c(t) = v_{control} \left(\frac{t}{T_s}\right) \left(1 - \frac{t}{T_s}\right)$ . So, you get  $v_c(t + T_s) = v_c(t)$  for the boundary condition.

And the controller switched transistors off, when integrated voltage equals to the carrier wave and thus  $v_i(dT_s) = v_c(dT_s) = v_{control}(t)d(t)(1 - d(t))$ . And thus ICs by this one and ultimately  $R_e(v_{control}) = d(t)(1 - d(t))\frac{\langle v(t) \rangle_{T_s}}{\langle i_s(t) \rangle_{T_s}}$  and this is the value of the effective resistance or the v<sub>control</sub>.

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So, what we can say? This is the overall part. This is the integrated reset, is a current source that is coming from this coupling inductor and the capacitor and this is a  $v_{control}$ . And ultimately  $v_{control}$  will be reflected as a current source. Once capacitor will be saturated, then by this. This and this will be made reset. This is the average current mode control for this generation of the parabolic carrier wave or because you can see that this is the parabolic carrier wave.

Now, I have mainly finished the single-phase power quality problem. That is been desired and generated for the diode bridge rectifier for the single-phase operation. Now, we shall require to take the industrial one, that is for the three-phase. So, first we will discuss the problem of three phase converters and the kind of harmonic present there. Because of the time constrained I leave out that portion of the problem for the single phase. you are well aware of those facts.

Now, we shall take out the three-phase solution of it with the higher power rating. So, we shall first discuss about the three phase solution in a different mode. Then at last we shall discuss the three phase PWM converter.

Thank you for attention.