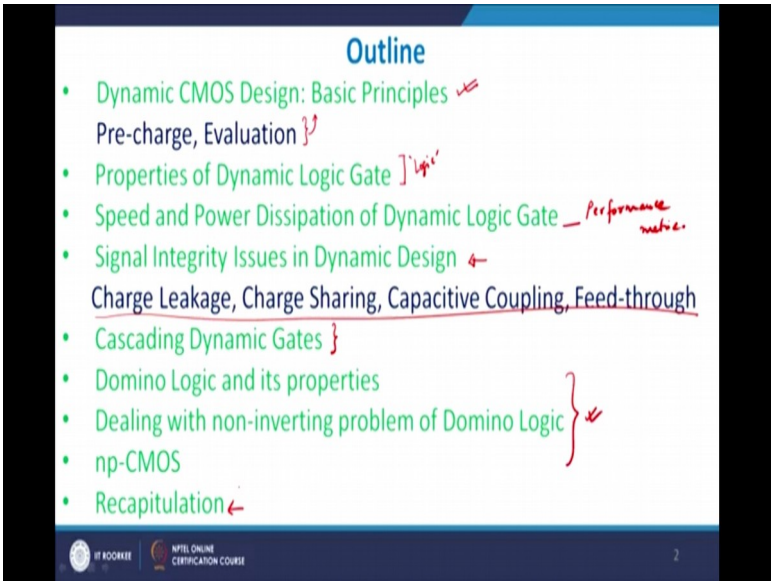
Microelectronics: Devices to Circuits
Professor Sudeb Dasgupta
Department of Electronics & Communication Engineering
Indian Institute of Technology, Roorkee
Combinational Logic Design-IV
Lecture 56

Hello everybody and welcome to the Online Certification NPTEL Online Certification Course on microelectronics device circuits. This module is combinational logic design module number four. In our previous modules we have looked into past transistor logic, we have also looked into transmission gate logic and we have seen how these logics behave under various signals given to it. What are the relative advantages and disadvantages of each of these logic design.

Today, in this module we will take up dynamic logic and see how is it different from static logic. As I discussed with you in the initial slides the very first slides of my combinational logical blog that static logics are those logics which are in which the output is either connected to V_{DD} or to ground or V_{SS} and therefore it is basically a low impedance node whereas when you talk of dynamic logic you can have a floating node picture available to you.

(Refer Slide Time: 1:33)

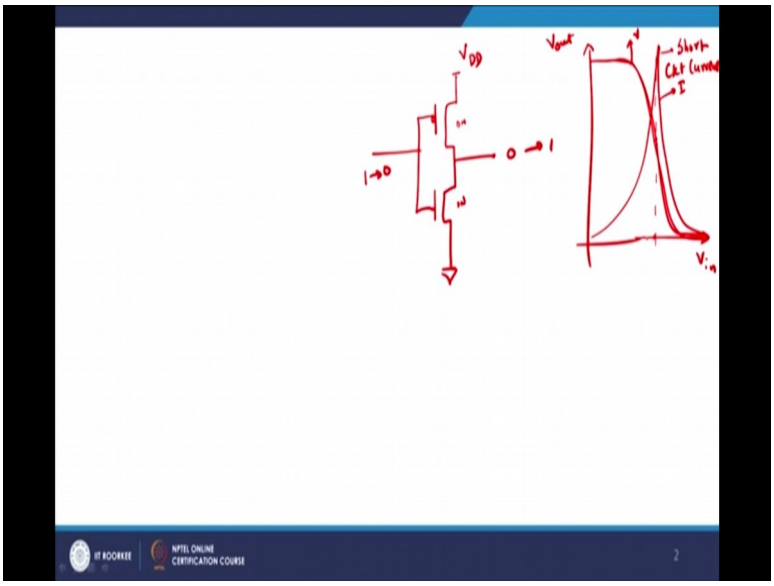


So with this let me come to the first outline of the module and the outlines of the module are: we look into dynamic CMOS circuit design, we understand what is the meaning of pre-charge and evaluation with respect to dynamic CMOS, we look into the properties of dynamic CMOS logic

design, dynamic CMOS logic, then speed and power of dynamic logic, so these are performance matrix here right and we then look into the signal integrity issues of a dynamic design. Typically dynamic design has got a major problem of signal integrity that means there is heavy leakage and so on and so forth so that is what I was in blue it is marked here that within this we will be looking into feed-through, capacitive coupling, charge sharing and charge leakage.

We will try to understand how we can cascade dynamic gates for a performance enhancement and then looking into domino logic and then NP-CMOS we will look into. This is the final one we will do and then we will recapitulate finally the whole discussion. So this will be the outline of the whole talk, as far as this is concerned.

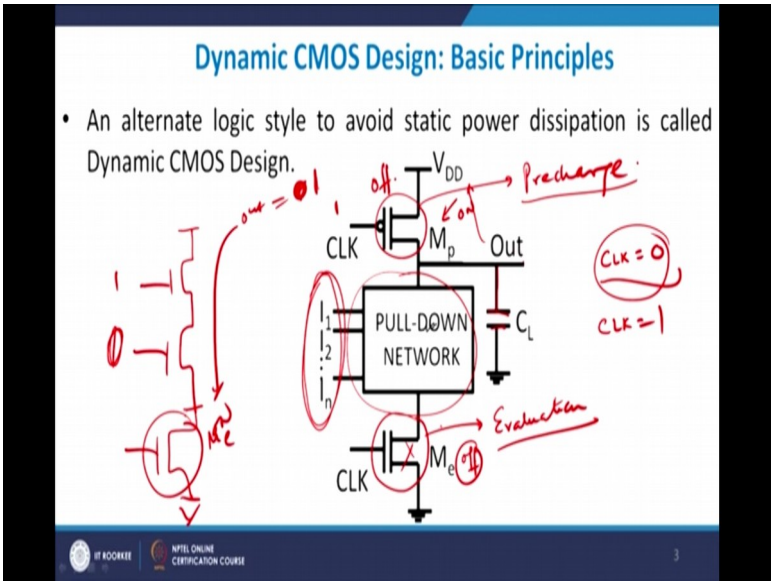
(Refer Slide Time: 3:06)



Let us look at the dynamic logic here. An alternate style to remove static power dissipation is called a dynamic CMOS logic design. If we remember at one point of time when we were using CMOS architecture, simple CMOS architecture and you had NMOS and CMOS as your PUN and PDN. Then remember when you are going from 1 to 0 and the output was going from 0 to 1. If you plot the VTC it comes something like this right? So if plot V_{in} versus V_{out}, I get the profiling something like this, right? The profile was something like this, but somewhere in the middle right here effectively both your devices are in the on state for a very short duration of time and as a result if you plot the current flowing through the both the arms you will see that this current suddenly peaks here and then falls down.

So this is the current and this is the voltage. This peak this current is referred to as a short circuit current right so this is the short circuit current which you will see. So this is the short circuit current which is there with you and this short circuit current implies that you will always have a large current at certain point of time.

(Refer Slide Time: 4:10)



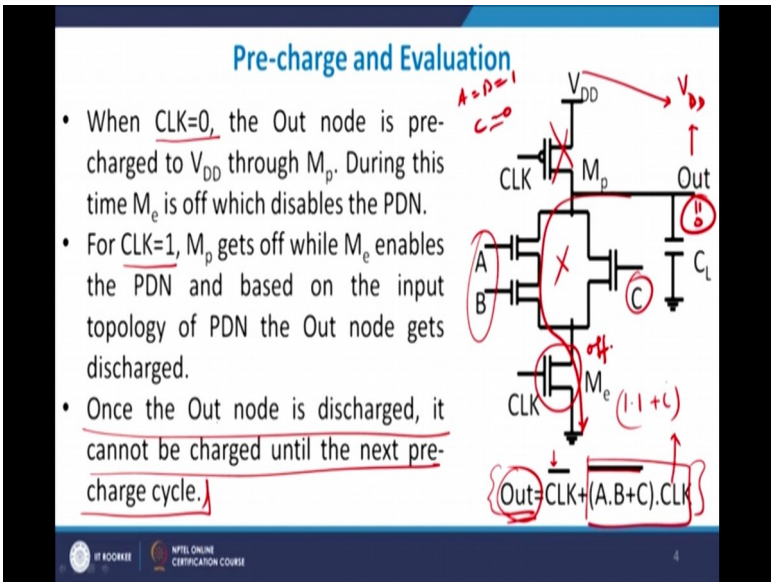
Now let us come back to dynamic logic and see how it is removed. Dynamic logic you have one single pull-up just like your CD NMOS inverter PMOS and you also have an evaluation transistor known as M_e and so this is an NMOS also referred to as an evaluation transistor M_e and this is M_p also known as a pre-charge transistor. We will explain these terms individually but we will come to that later on.

So, and this is the pull-down network which you see, this black box is basically pull-down network with n inputs I_1 to I_n here and the output is basically here with this is the load capacitance, which you see. Now it is very simple and straightforward. Whenever your CLK is equals is equal to 0 right your M_e is switched off right and this is switched on. So when this is switched off and this is switched on, output goes to V_{DD} because this is switched on but your, this transistor is not coming to picture at all because here this is been cut off. So when your CLK equals to 0 right and your this transistor switches on, your output goes to 1.

Now when your CLK goes to 1 right, then this CLK this also goes to 1, right and therefore this switches off but then depending on the value of your input vectors I1 to I n and the types of logic design which is there in the pull-down network, either the output will go to 0 or it will not go to 0. For example, if your pull-down network is something like this and then this is your M_e this is already on right? If this both inputs are 1 1 then out which was initially held to 1 will now go to 0 across these transistors, but if your input is 0 here these will hold the output equals to 1, you are getting my point?

So two things happens, one is the type of network which you are choosing in the pull down network that, and the type of input you are choosing here will determine whether the output. So you see at no point of time, V_{DD} is directly connected to the ground and as a result because you have CLK, because you have this driving these CLK transistors. As a result you will automatically have much short circuit power dissipation.

(Refer Slide Time: 6:37)

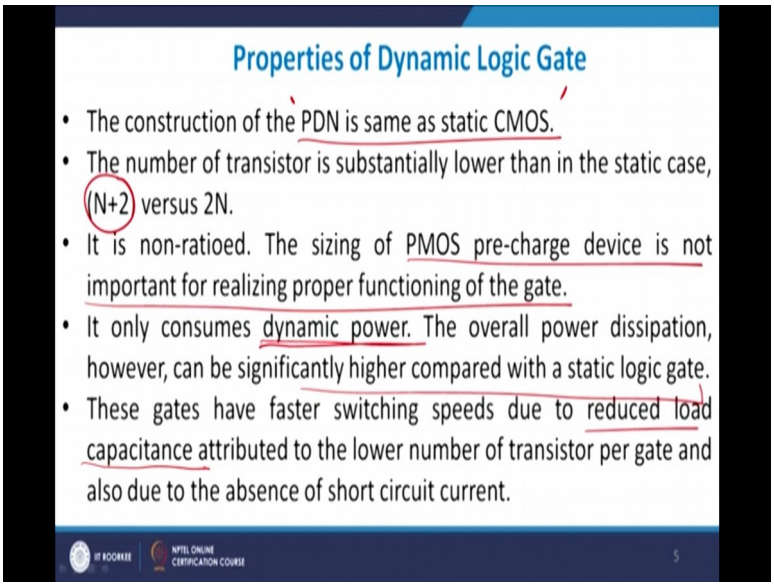


That is what is all written here and so that evaluation, for example, when CLK equals to 0 out will go to, will be pre-charged to V_{DD}. This will go to V_{DD}, the out value will go to VDD and this will be disabled or this will be switched off right? A pull down network will therefore be disabled so this will not work and therefore out will go to V_{DD}, now when CLK goes to 1, M_p switches off right and based on the values of A B and C out will either go to 0 or remain stable.

Now, once you have A B C suppose both, say A equals to B equals to 1 and C equals to 0 then out will discharge through this path and out will go to 0, clear? When out goes to 0 we get an important issue here that you will never be able to recapture or have the value equals to V_{DD} until and unless your CLK goes to 0 once again. So till your CLK goes to 0, your output will never go to back to V_{DD}. So in the sense that once out node is discharged it cannot be charged until the next pre-charge cycle.

You understand this point, and therefore out can be written as CLK bar because CLK bar when it is high then CLK will be low so this will be 0 right and therefore out will be equals to V_{DD} out is equal to 1. Similarly when CLK equals to high and CLK bar will be low so this will go to 0 this will go high and then depending upon A B and C out will be determine right and this is basically your, the complement value will be shown to you. Why? Because, for example, if I take 1 dot 1 plus 1 I should get output should be equals to 0 and that can only happen if we have a NOR function or a NAND gate.

(Refer Slide Time: 8:44)



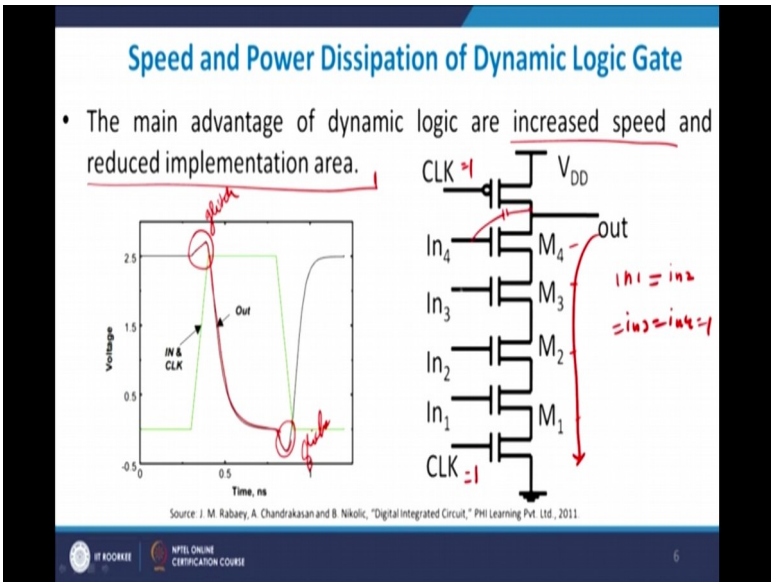
What is the property of dynamic logic? The construction of PDN is therefore exactly the same as a, the construction of the PDN is the same as your static CMOS logic. We have already done that. So PDN network is exactly the same. However, it is much lower than static the CMOS logic. You actually require N plus 2. N plus 2 why? Because N is the number of pull-down networks and plus 2 because 1 pre-charge transistor and 1 evaluation transistor. Of course, it is a

non-ratioed logic right which means the sizing of PMOS pre-charge device is not important for realizing proper functioning of the gate.

Please understand. Proper functioning means logical function of the gate is not determined by the W by L ratio of the PMOS transistor. PMOS transistor therefore W by L ratio will only help you to pre-charge your output node to V_{DD}. That is all. It does not play a role in determining the VTC, voltage transfer characteristics in anyway and therefore we define this as a non-ratioed. As I discussed with you, it only consumes dynamic power and therefore overall power dissipation can be highly compared to static logic gate because dynamic power is very high and since we are using CLK, its power can be very high.

However, these gates have much faster switching speeds because if you are reduced load capacitances because why because now the number, see in a CMOS inverter you had almost double the number of gates. Here the number of gates have drastically reduced and therefore your loading of the capacitance actually reduces and the speed of the circuitry improves so dynamic circuits are relatively faster in nature.

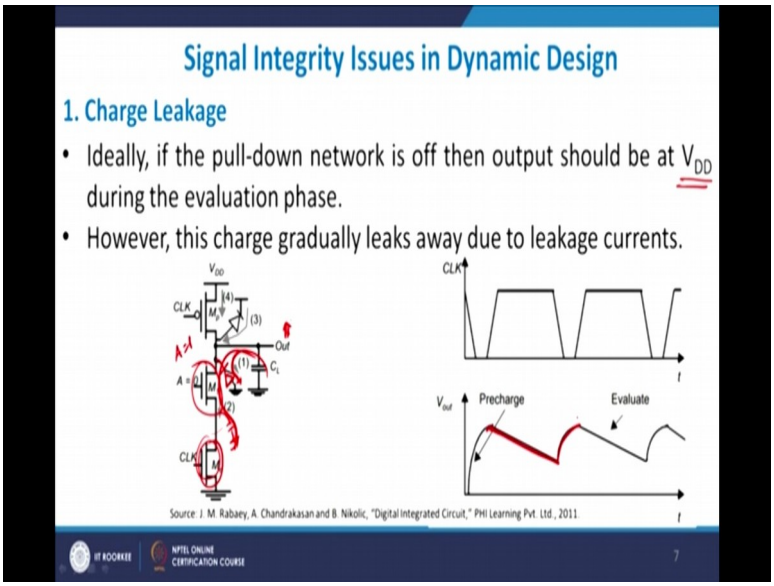
(Refer Slide Time: 10:29)



Let me get into speed and power dissipation in dynamic logic. The main advantages was, as I discussed with you, increased speed and reduced implementation area because of less number of transistors with you. However there is a small problem here that when the input suppose your input goes high and the CLK goes high, then the output should go low and it goes low also but the problem is that output going low across the M_4 M_3 so whenever my CLK goes to 1 and this goes to 1 then depending upon the value of in 1 equals to in 2 equals to in 3 equals to in 4 equals to 1 then only out will actually discharge through this path which means that the discharging path has got a large resistance being offered right?

So your delays will be typically large and therefore you see your out is basically delayed by a large quantity here right and not only that, your out is also showing a small glitch here and a glitch here so you have a glitch here and a glitch here. This is known as the glitch. This is because of a capacitive coupling we will see later on as we move forward but this is because of capacitive coupling and therefore you will see suddenly, the reason this happens is, that as the input suddenly increases there is a capacitive coupling between input here and the output here right and as a result the output shows a certain glitch in the output side and therefore that increases the capacitance.

(Refer Slide Time: 11:46)



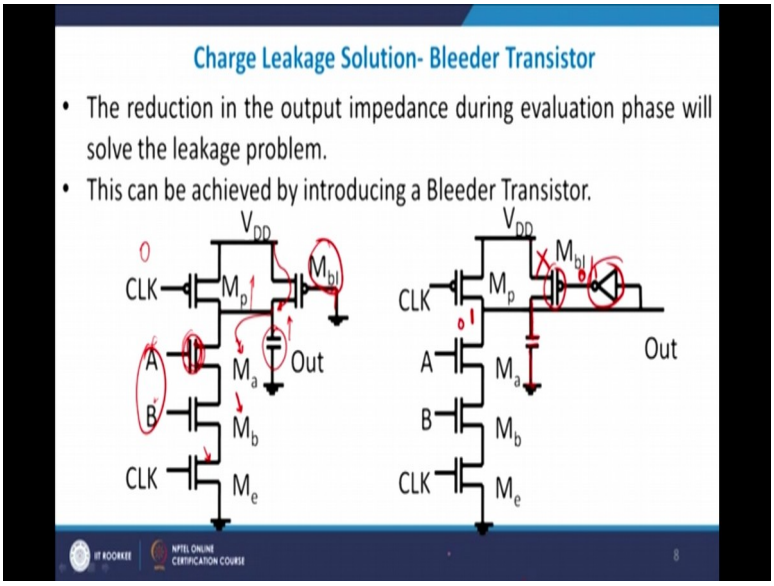
In a dynamic logic, you do have a problem of charge leakage and that is very important or that is very difficult to do that. Ideally, as I discus with you, your pull down methods is off when the output should is at V_{DD}. So when your output is at V_{DD} right since your CLK is at low voltage and so this is cut off right? However, there is a problem the problem is that there is a, so when you pre-charge it, your output goes to high value right?

It goes to high value but though your M_e is switched off you still have let us suppose A equals to 1 now and this transistor was switched on, M1 was switched on so any cap here or any reverse biased connected diode here which is basically the depletion capacitances, the charge will actually leak through these domains and therefore the pre-charge value will start to fall down until and unless the next CLK pulse comes and tries to raise the value to a high value.

So you are losing the charge because of leakage, charge leakage specially in a case when you have single integrity issues in a dynamic design. So whenever you have a dynamic design you do have a problem that your pull down network though ideally is supposedly switched off but if let us suppose one of the gates connected to the output node is switched on then the output node charge might actually go through this particular device which is a on state device and reside in its capacitances, say a reverse biased PN junction diode capacitance or the C_L load capacitances or maybe parasitic capacitances.

So what will happen is that you will lose it. Once you lose it you do not have any other option but to wait for the next pre-charge cycle to come right? And so that loss is pretty steep so you see it is actually gone down to a larger extent. So now what happens is that when you go now to the evaluation phase which is when your CLK equals to 1 and CLK equals to 1, then you start from here rather than from here so you are not able to utilize the whole swing of the design in this case. So, this is one of the problem areas which you will see.

(Refer Slide Time: 14: 24)

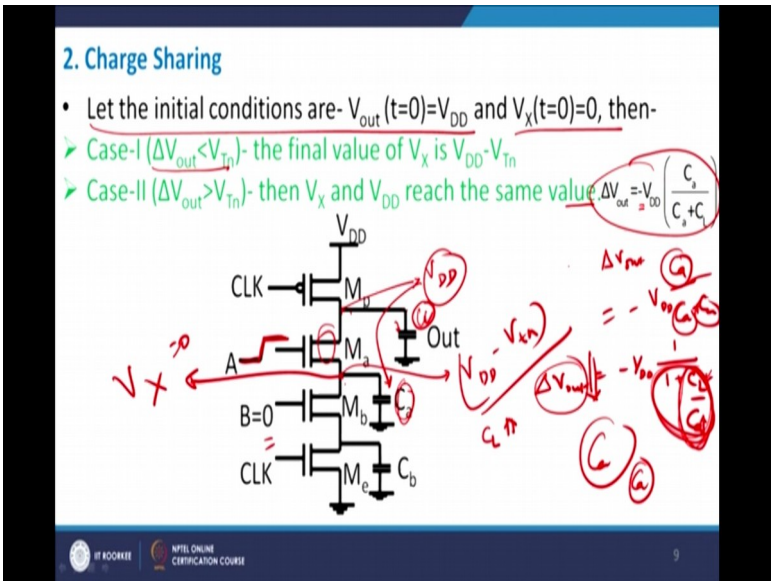


So, what people thought and people did also, they introduced what is known as a bleeder transistor. Now, let us see how it works out very simple and straight forward. What I do is I have M_a M_b so it is an AND gate. This is my evaluation transistor here and this is M_a input 1 input 2 A and B are inputs here CLK and I have put a bleeder transistor M_{bl} there right? So let us see how it works out. So let me say that CLK is basically equals to 0.

This charges up to a very high value, so this charges up to very high value this is a normally on device because PMOS is connected to ground and since this typically high value sorry this becomes a high value even if these transistors are switched on if suppose, this transistor is switched on even if some discharge takes place I still have V_{DD} connectivity here and the V_{DD} will appear and charge this node once again so this node will be again charged to a high value. So you do not lose charge because you are applying a charge from a external world.

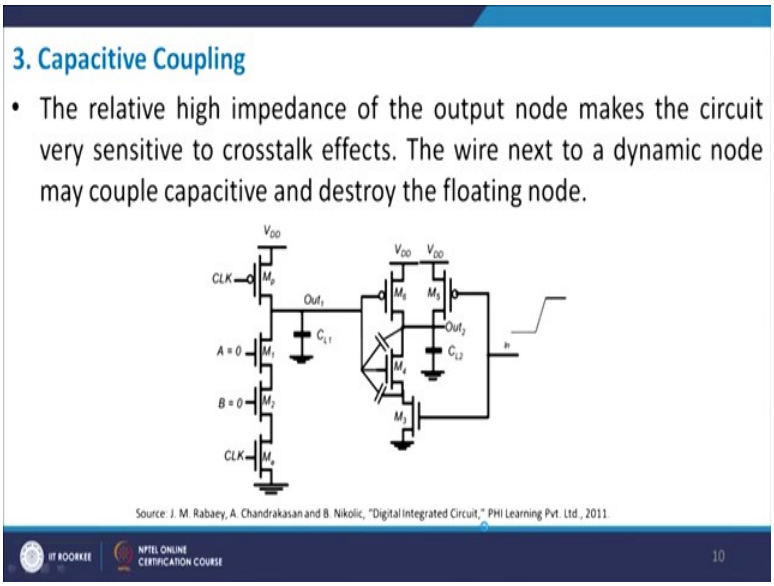
Similarly if I take a NOT gate here and if I put suppose this is for example if I take this to be as equals to 1 right, because it has charged to this value this will become 0, this will become 0 implies that M_{b1} will be on M_{b1} will be on means that this V_{DD} will be always connected to this particular capacitance and the capacitance charge will never be lost. You will have always a high capacitance value there and when my this goes to 0, when this goes to 0 this becomes equals to 1, this cuts off and you enter into the evaluation phase. So this M_{b1} is defined as my bleeder transistor, bleeder means it is basically bleeding the charge from V_{DD} on to the capacitance which you see in front of you.

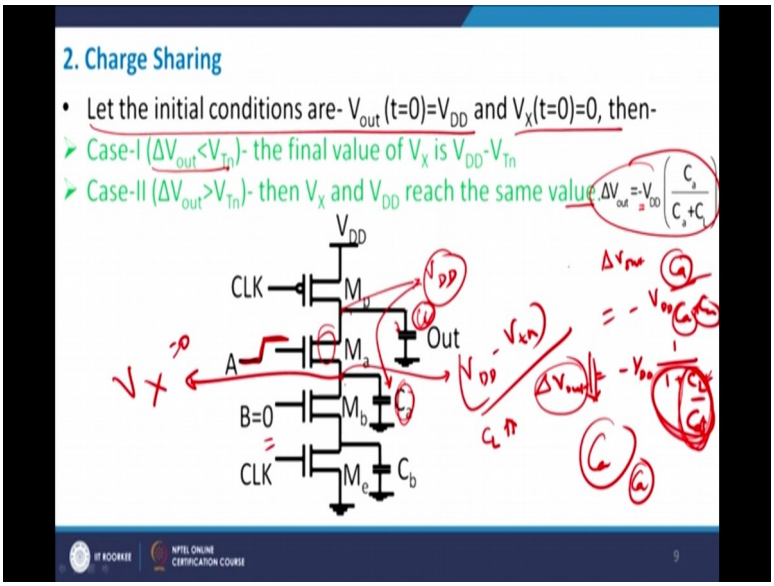
(Refer Slide Time: 15:50)



One classic example which you see, one of the classic example is basically to do with, I will just discuss with you the classic problem.

(Refer Slide Time: 16:07)





The classic problem of this thing is that when you have a capacitive coupling between the two we also have a charge sharing. What does a charge sharing mean? Charge sharing means that whenever your device switches off, the charge which is there within the device has to sit somewhere right? It has to go somewhere right? And therefore, it will, that charge will be shared between two or three devices and its voltage will go up.

I will explain to you this is worked out. Let us suppose initial conditions are my V_{out} is equals to V_{DD} and V_x equals to 0 so V_{out} is V_{DD} so I have already this is V_{DD} right? And I am already into

evaluation phase. V_x which is the voltage at the intermediate point. This is intermediate point x V_x equals to 0 because obviously you are switched on and now what I am doing is I am giving a signal A equals to 0 to 1 and B is stabilizing at 0 right?

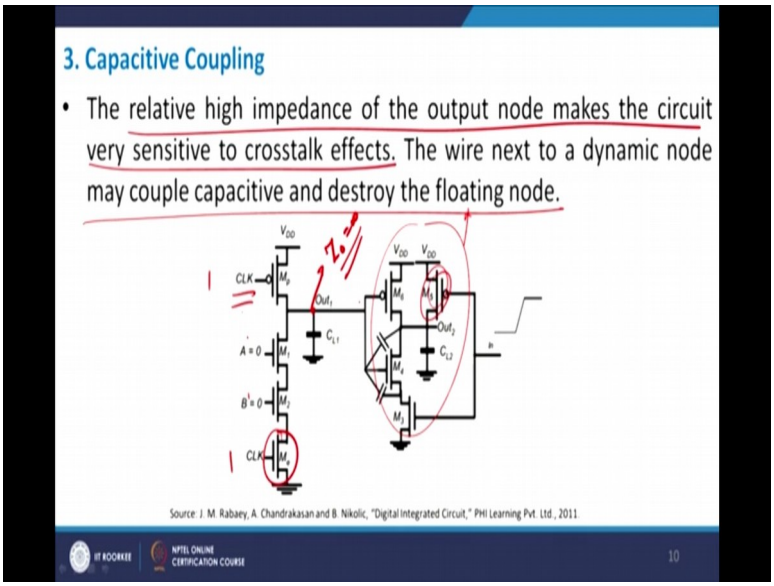
Now, if ΔV_{out} is not smaller than threshold voltage of this device right? ΔV_{out} being the change in gate voltage gate voltage is smaller, then if this is switched on this voltage will appear here. It is behaving like a past transistor logic as V_{DD} minus V_{tn} right? Now but if ΔV_{out} change in the ΔV_{out} value is very large and is much larger than the threshold voltage of this M_a then V_x and V_{DD}, these two will reach to the same value and your ΔV_{out} will be, what is the condition for ΔV_{out}, is V_{DD} upon C_a by C_a plus C_L. C_a is this one and this is C_L right?

Which means that it is basically a capacitive coupling and depending on the effective values of C_a and C_l, my V_{out} will be there. So if you look at ΔV out it is equals to minus V_{DD}. If we divide numerator and denominator by C_a I get 1 by C_L upon C_a so you see if your C_L is very very large as compared to C_a. This quantity will be very large right and therefore this quantity will be very small right and sorry yes so it will be very small and therefore ΔV_{out} will be very large.

It will be so also because if C_L is very large the most of the charges will be accumulated at C_L and the voltage change at output will be very large. Similarly if your C_a is larger then C_a is larger means then this is large which means that that this falls down and therefore, sorry I am sorry. I will just reframe my question, the understanding here, if C_L becomes large then this quantity becomes large right and therefore ΔV_{out} goes down, the reason is that with increasing value of C_L, more and more charge will be accumulated here whereas when you increase the value of C_a the more distribution will take place and your ΔV_{out} will actually become larger and larger right?

This is known as charge sharing. So whenever you switch on M_a right because a goes from 0 to 1 some charge from this V_{DD} node goes on to M_a node and therefore ΔV_{out} shows a small drop right and this drop is you see negative, you see it is negative actually and as a result you will always see a drop right and this is charge sharing phenomenon in a domino logic in a dynamic logic.

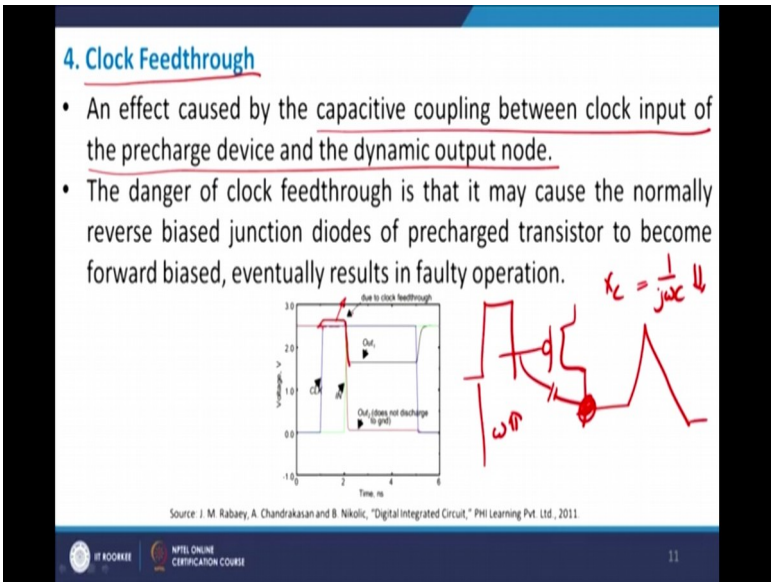
(Refer Slide Time: 19:18)



Let me discuss with you the capacitive coupling therefore. The capacitive coupling, so my output impedance is relatively high and therefore very sensitive to cross talk effects. That is the only problem area of a dynamic logic because this is quiet high Z_{out} is equals to infinity ideally right? The wire next to the dynamic node may couple capacitive and destroy the floating node right and that is your problem area which you face for a dynamic logic design.

So what people did so this is a bleeder circuit which you see in front of you and this is a bleeder transistor here which tries to make the level again go to back to V_{DD}. So even if there is a problem with your output because of charge sharing or because of leakage. This helps you to raise the value to a high value, right but the problem here is that why is it Z equals to infinity is it is behaving like a floating node because why because your CLK has actually gone to 1 CLK is equals to 1. This is switched on but let us suppose A and B are both zero then this will be acting as floating node with high output impedance right and therefore they will all be affected by crosstalk noise and electromagnetic interferences will happen here to a larger extent right? And this is therefore known as, this will result in externally signal being degraded to a larger extent.

(Refer Slide Time: 20:34)

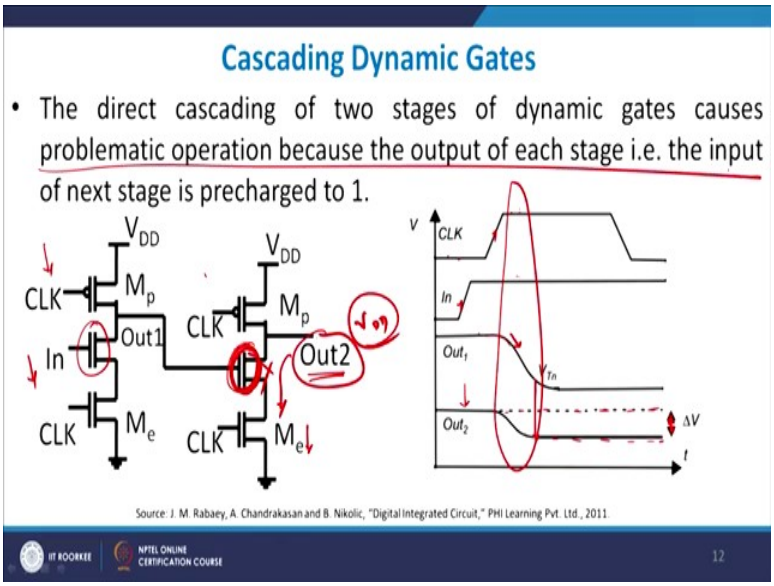


Last, let me come to the last problem area of this thing and this is what is known as a clock feed through. Clock feedthrough is basically a capacitive coupling between the clock input of the pre-charge device and the dynamic output node. So if you look back here this was clock here and this was the output here. So your clock goes high like this right? Now because of a coupling between this and this, the node voltage also goes like this.

So you see here when the clock goes right high the output should remain stable like this to V_{DD} but actually it goes beyond V_{DD} for some duration of time and then starts to fall back. This is because of the fact that for a finite duration of time because you see, clock is rising very fast which means that this ω is very very large right? So ω is large means ω is 1 by jωC is very very small Xc.

So Xc is small means it is looking almost like a transparent medium. So any small change in the clock here, high frequency change will be easily detected at the output node of my pre-charge and that is the reason you will have a voltage and as a result what happens is that the voltage rises beyond V_{DD} right and that results in what is known as a clock feedthrough and this results in a larger power dissipation and signal integrity issues so power dissipation is a problem.

(Refer Slide Time: 21:54)



Now let us look at cascading of two dynamic gates. So I have cascaded how so output is cascaded back into the input of the second gate. Now you see if my CLK goes high and my input also goes high my Out1 will start to fall down. Obviously the input goes high means this is on and the output starts to go down. It starts to go down means, this so it was initially on this was high right it was high, it was high means I should get Out2 be equals to 1 to 0 why it is 0? See initially when your CLK is low and input is low CLK is low input is also low out 1 will be high which means that this is on but then your CLK is low and input is low therefore this will be off and Out2 will be so the CLK is low means Out2 will be also latched to V_{DD}. That is what is happening here.

Now as you input those high it take some finite amount of time to output to fall down output starts to fall down as it crosses the threshold voltage of the next transistor. At this stage my this goes to off state. Which goes to off state? The next device goes to off state. As it goes to off state my out then fixes to that same value where it goes to off state. Ideally it should have been here only you understand?

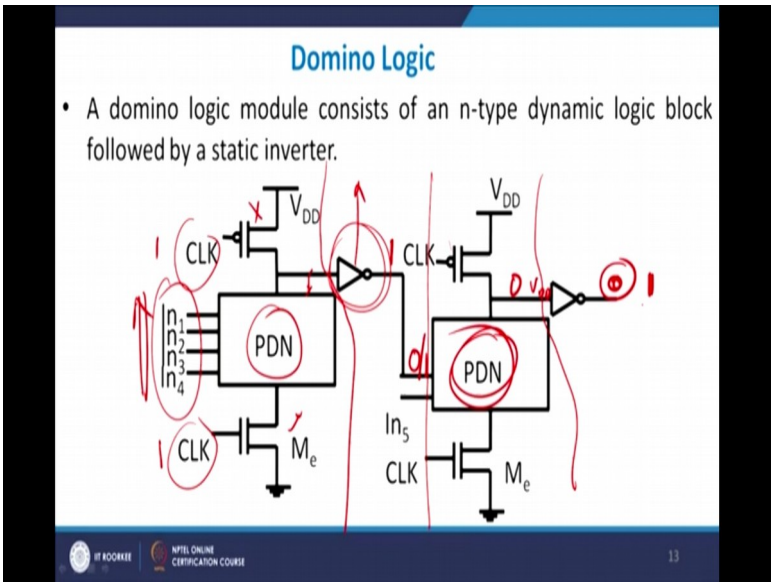
Ideally this should be here because Out1 was initially high and then starts to fall down but because of a finite delay between the two this transistor will get switched off at certain amount of time which is threshold voltage of the device and as a result what will happen is that the Out2 will be latched to a value which is not exactly equal to its initial value and therefore there will be

a ΔV change here and I cannot recover it until and unless I come back to the next pre-charge side.

So you see, Out1 has fallen down out1 is falling down so Out1 when it was initially high CLK is high and so CLK is high and input is also, so if you look at this, concentrate on this part so when CLK is high and input is high then M_e is on, right? And out should actually fall down and it is falling also but it should ideally go to a low value, it should go down if you allow this transistor to go to large value but then Out2 when it crosses the threshold voltage of the second transistor it cuts off this second transistor and this latches to a value which is a not equal to its initial value right?

And therefore you lose so when you cascade dynamic logic you end up losing that is the problematic operation because of the output of each stage okay? And that is the problem. Direct cascading is therefore not a good idea.

(Refer Slide Time: 24:27)



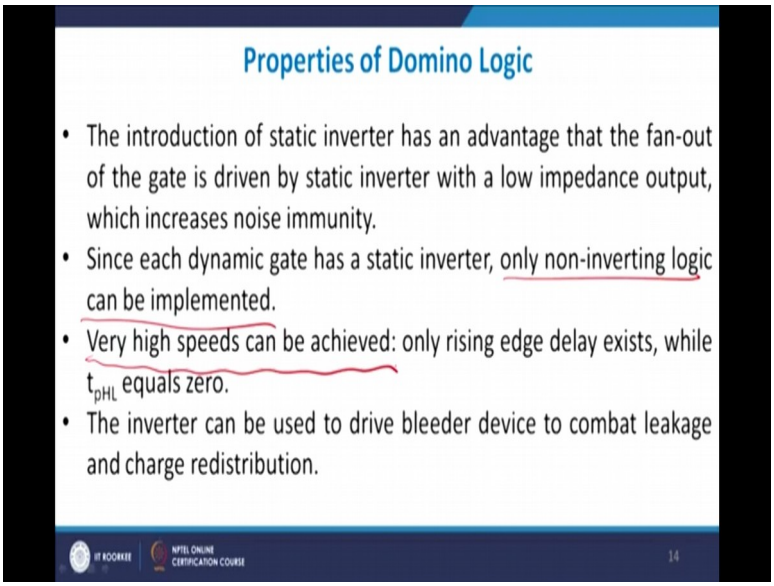
So what people thought was, that since dynamic cascade dynamic you cannot directly cascade two logics because the logic falls down and not only that you will not be able to recover that logic until the next pre-charge cycle come. We enter into what is known as a domino logic. So I have inputs here of course and I have a PDN here and a PDN here. I also have a CLK and a CLK

bar. So this, if you look at closely it is exactly the dynamic logic. Similarly this is also a dynamic logic here right? But they are cascaded by a static inverter right? And they are cascaded by a static inverter.

So you see, this static inverter will always ensure that if suppose CLK is equals to 0 then this will V_{DD} so this will be 0. This will be 0 implies that your PDN will be switched off and therefore if it is switched off and CLK equals to 0 this will be actually V_{DD} and output will be equals to 0 right? Now when this input goes all high let us suppose and it is a AND gate, CLK goes to 1 here. This switches off and this switches on and this voltage starts to fall but nothing will happen here until and unless this goes below the switching threshold of this transistor which will make this goes to 1 and this will go 1 and therefore then it will switch on my PDN.

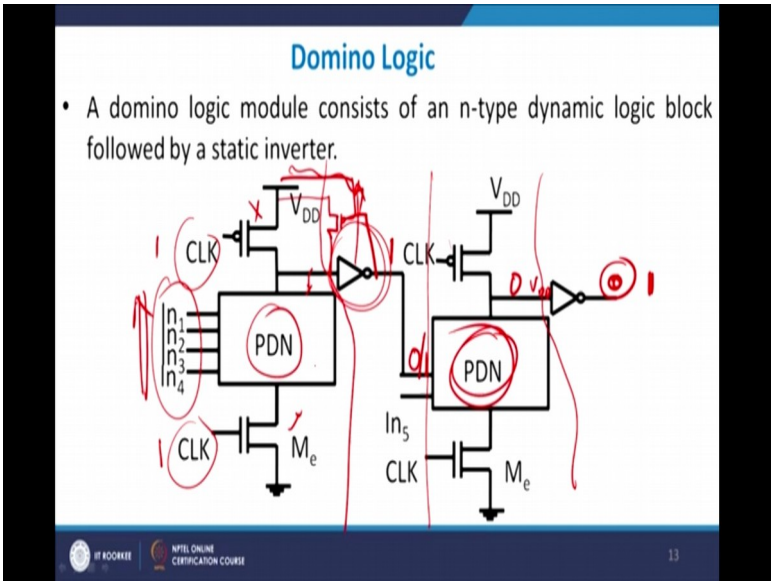
When the PDN goes high this goes to 0 and then output becomes equals to 1 right? So by just inserting a static logic here a static CMOS logic here I am able to restore the signal integrity issues in a domino logic right? So the introduction of a static inverter has an advantage where the fan out of the gate is driven by static inverter which is obviously a low impedance node and therefore it increases the noise immunity. So noise immunity problem is gone.

(Refer Slide Time: 26:11)



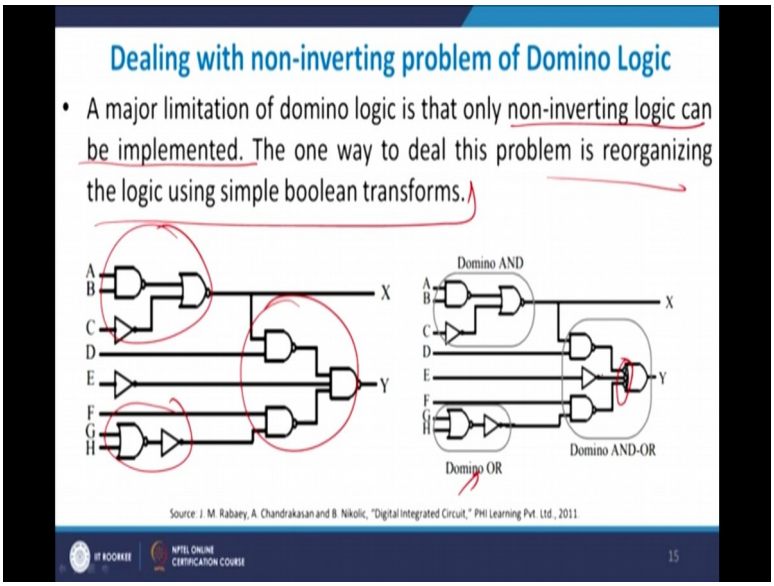
Since each dynamic gate has a static inverter only non-inverting logic can be implemented but obvious very high speeds can be achieved in this case and the reason being that t_{PHL} being approximately equals to 0. High to low will be approximately equals to 0 right? Now the inverter can be used to drive bleeder device to combat leakage and trans distribution.

(Refer Slide Time: 26:40)



How you can do that sorry how you can do that, you can add a bleeder transistor here right and this bleeder transistor will be added here and this will be V_{DD} it will be taken care of in this manner and therefore you can have a bleeder transistor directly inserted here. So charge loss will be taken care of. The charge sharing will be taken care of and the domino logic gives you a very good idea about this whole charge description.

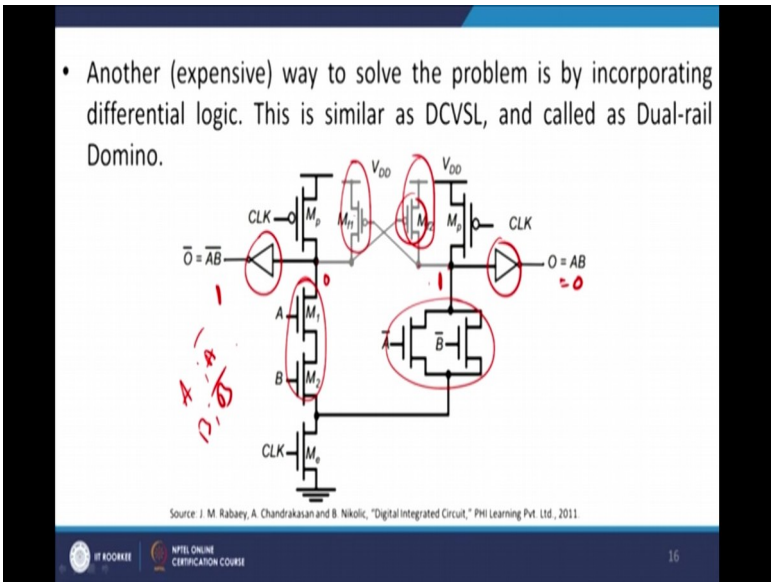
(Refer Slide Time: 27:01)



Now so as I discussed with you therefore a major limitation of domino logics is that only non - inverting logics can be implemented like non-inverting logics means those who do not invert the output. So you just need to re-organize your logic function using simple Boolean transform. For example, I can do a domino NAND, this is to be a domino NAND and this to be as a domino NOR which you can do and this is your domino NAND NOR operation by putting a bubbled OR gate right? I will not go details, will not go into the details of this one too much a large extent but simply by choosing appropriate Boolean functions we can actually remove the problem of non-inverting in logic in a domino function.

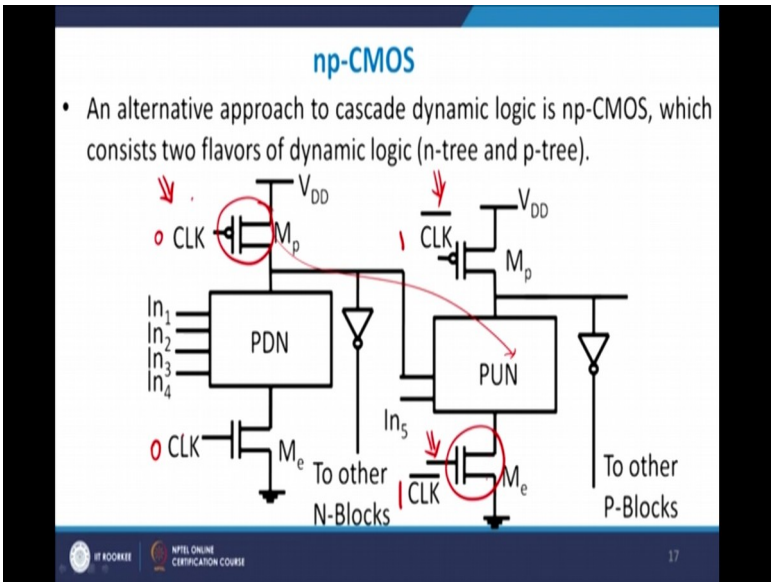
Another way to solve this problem is differential logic. It is exactly the same as DCVSL which we have already learned in our initial modules and this is also known as dual rail domino logic in which we do I have got a static inverter applied here and the static inverter applied here. I have got a feedback or a feedback resistance applied here so you have a positive feedback latch here so once this goes to 0 this switches on this device and this goes to 1 here. When this goes to 1 this goes to 0 here and this goes to 1 here so you have got 0 and 1 coming into picture.

(Refer Slide Time: 28:20)



Now this is therefore you see this is AND gate this is basically your NAND gate so you have series connections here see, so you have a parallel connection here in this place right? So once you ensure that this is 0 and 1 these PMOS transistors M_{f1} and M_{f2} help you to speed up the logic right and helps you to make this go to 0 very fast go to 1 0 in a fast manner. The advantage here is you get both inverted as well as non-inverted logic but the disadvantage here is that you require to generate both your input signal and its inverted signal. So both A A bar has to be generated B and B bar has to be generated in this case right?

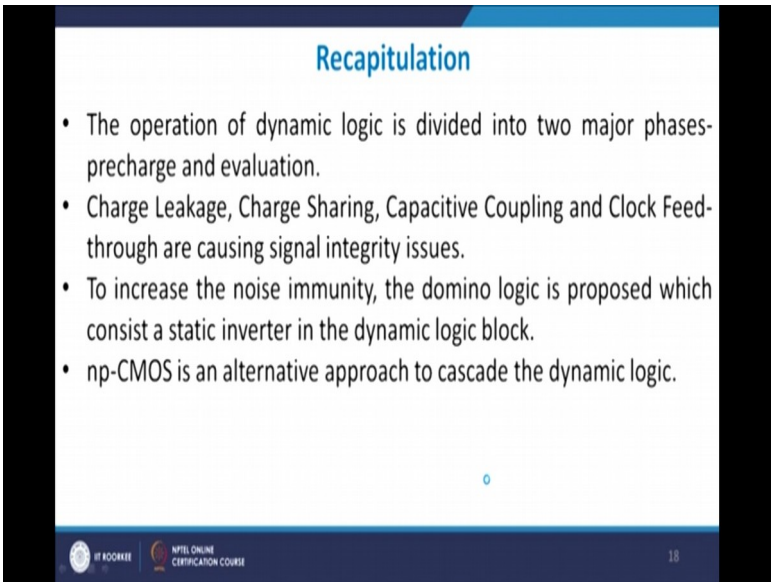
(Refer Slide Time: 29:03)



And that is the problem area for this logic taken into consideration. Another alternative approach is using NP logic. NP logic what we do is that, it is exactly the same as domino logic only thing is that we have a do is that we have a dynamic logic with CLK and CLK and then we drive it with a dynamic logic with CLK bar. So whenever your CLK is high so when CLK is suppose high or suppose CLK is low so this is low, this is low but then this is high and this is high.

So out of all these four designs right if it is 0 CLK is 0 CLK bar equals to 1 means this evaluation transistor will be on and this will be on. This both will be on together and as a result what will happen is that you will have a direct path between these two points provided Me is on provided your input five is a high value which you see right but the NP I will like you to go through it in a much more detailed manner from this book actually and it gives you a very good idea about NP-logic design.

(Refer Slide Time: 30:06)



So let me recapitulate what we did till now. We looked into the operation of dynamic logic and we saw that it can be divided into pre-charge and evaluation. We also looked into charge leakage charge sharing phenomenon of dynamic logic and we also saw that there is signal integrity issue in dynamic logic. How to remove it there are methods of doing it, using, for removing the by using static CMOS logic we have seen that and NP-CMOS is an alternative side to cascade the dynamic logic. So cascading ordinary dynamic logic is difficult task. NP logic is one of the solutions to this particular design right? With this we finish off the dynamic logic case for a combination logical blog. Thank you very much.