Microelectronics: Devices to Circuits
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Module 11
Lecture 55
Combinational Logic Design -III

Hello everybody and welcome to the next edition of NPTEL online certification course on microelectronics devices to circuits. We start today's module from the combinational Logic design III. So we have actually covered two modules of combinational logic design in which we have seen what is the meaning of combinational logic, how can you design a combinational logic from a Boolean expression, we have also seen how does a combinational logic, what are the various parameters for example power, delay, how they are related to the aspect ratio of the transistors and so on and so forth.

So we have studied two types of styles. One is the complementary style, one is the ratioed logic we have studied and we have seen that, complementary style is the most robust style but the area count is typically high. Whereas ratioed logic gives you more amount of static power dissipation and noise margins are limited. Today we will take up what is known as a pass transistor logic in applied to digital logic design.

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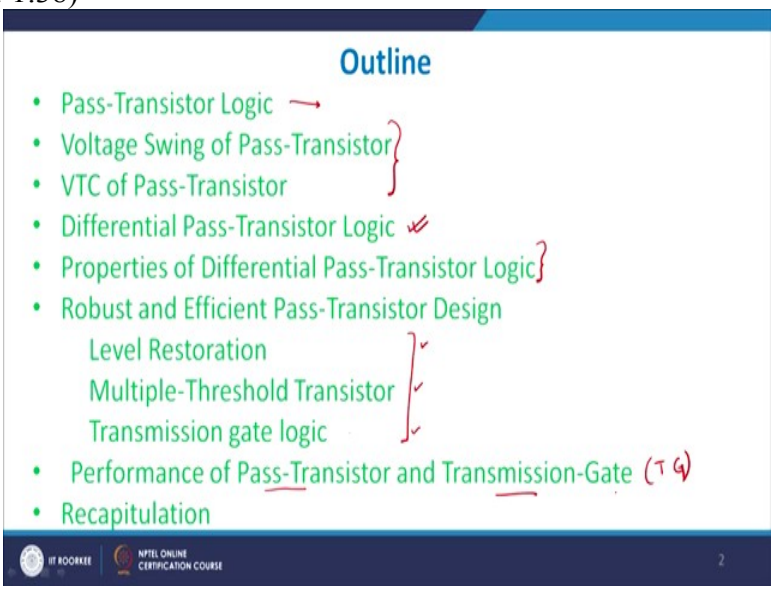

So the outline of this module is that we will first look into pass transistor logic and then look into the VTC and therefore the voltage swing of the pass transistor logic. So we will look into the fact that what is a pass transistor and therefore what is the voltage transfer characteristics. Then maybe I have a look at differential pass transistor logic. We will look into properties of differential pass transistor logic and then we will understand these three quantities here which is level restoration, multiple threshold transistor design and transmission gate logic, right?

And then we will compare pass transistor logic with TG logic which is transmission gate logic. This is also referred to as TG, right. Transmission gate. And then we will recapitulate. So this is a general outline of the module structure for this particular lecture. And we will go step-by-step and see how it works.

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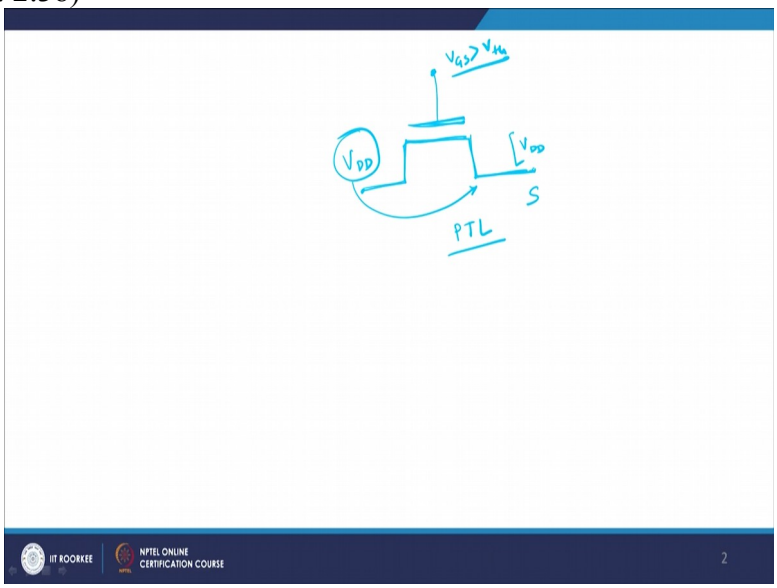

If you remember now, till now we will first now look into the transistor logic. What is a pass transistor? Let me give you a very simple idea what is a pass transistor. A pass transistor is something like this that if you have a gate, right you have a gate here and you apply a V_{DD} here, it is a drain side and this is your source side. Now, what you do is that you do not apply and signal on the gate side right? You apply the signal actually on the drain side, right.

And let us suppose you apply a gate voltage which is greater than threshold voltage, then since this is on right, this will be on, this V_{DD} will be transferred to this particular point and this will be V_{DD}. Obviously, of course there will be a threshold voltage drop. I will not discuss that point here

at this stage but the name, it is pass transistor logic, also referred to as PTL, pass transistor logic, it allows you for this V_{DD} to move forward and appear in the source side, right. So this is the basic pass transistor logic, basic idea.

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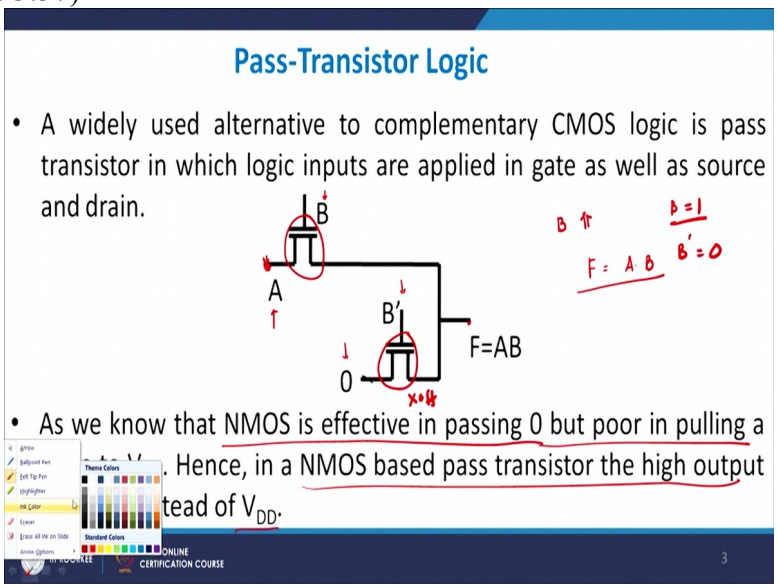

Now with this knowledge, let me give you an idea about basic AND gate using pass transistor logic. So you see here, I have got one transistor here, another transistor is here, and we apply the signal B here and we apply a complementary signal B here, we apply a 0 here and we apply the A here. So whenever my B is high right, whenever my B is high, whatever be the value of A appears outside and therefore safely I can write down F equals to A dot B. Why? Because whatever the value of A will appear at this point.

So if A is equals to 0, F will be equals to 0. If A equals to 1, F will be equals to 1 provided B equals to 1. Now whenever B is higher, B equals to 1, you ensure that your B complement is basically zero which meaning then this will be cut off. And therefore, this your output will be just latched or bar to this input A here. We have already dealt in your previous turn that if you remember the question which we asked was, why NMOS is a very good pull down network candidate whereas PMOS is a very good pull up candidate?

And we told you that or we discussed that NMOS is a very good, it is a very good, it allows you to do a very good passage of zero whereas PMOS allows you to do a very good passage of 1. So NMOS is a very good passing of but a poor in V_{DD}. Hence in NMOS-based pass transistor, the

high output is V_{DD} minus V_T instead of V_{DD}. That is what I was saying that if you have got a high input transistor in a pass transistor logic, the output will appear as V_{DD} minus V_T.

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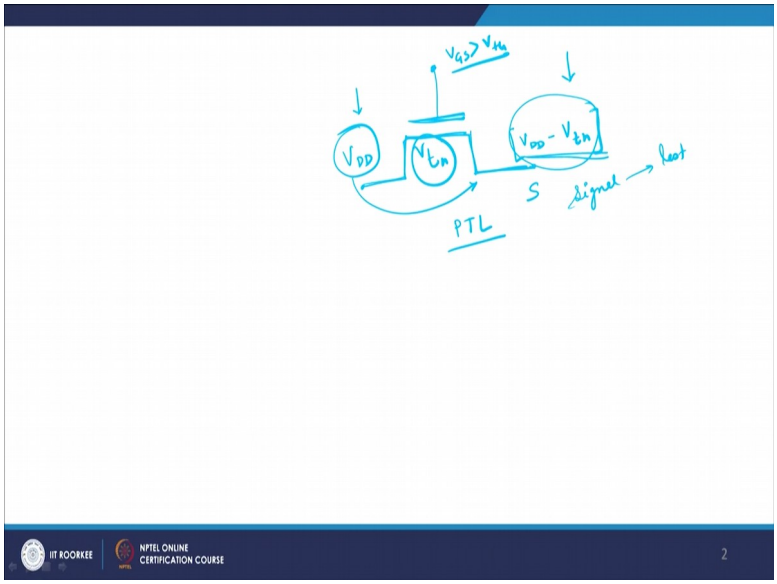

So the discussion which I was having here, you will have V_{DD} minus V_{TN} here, right where V_{TN} is basically the voltage drop here, right. So whatever the voltage here, you get a drop in this case, right. And therefore, and please understand this drop cannot be restored at any point of time, right. And therefore there will be a loss of the signal. So the signal will be lost, right. So a pass transistor logic has this problem that the signals will be lost.

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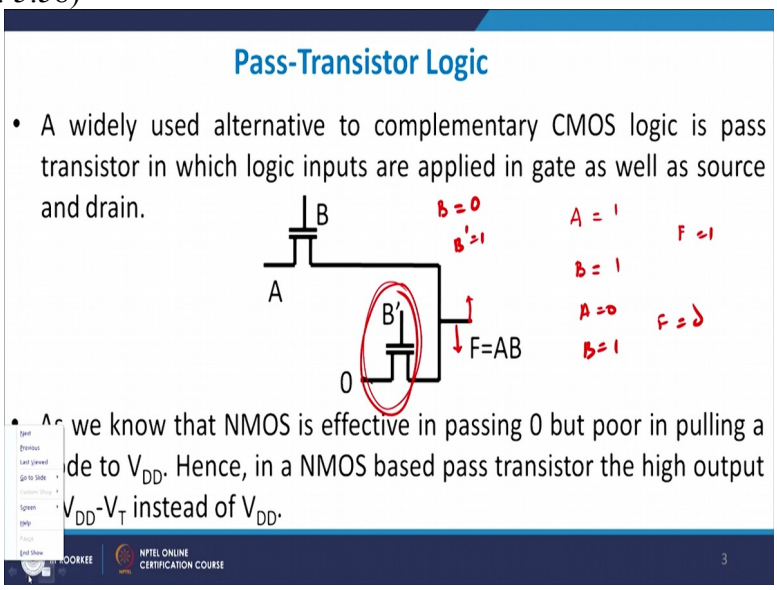

Now if you look at this, again this structure here, we have discussed this point that now you see, in this whole structure, even if you do not give this transistor this transistor, you still will have an AND application but the problem is that there will be a floating node available to you whenever my A is equals to 0 or 1. So now suppose my B equals to 1 and my A equals to 1, then output of course will be 1 and this will be at high-voltage, high. Similarly, if A equals to 0 and B equals to 1, output F will be equals to 0 and this will be at low voltage.

But then, this will not be connected to any input and therefore there will be a problem of floating node, right. And that is the reason you always have this transistor with you. I will give you an example. For example let us suppose B was 0, right. So B bar will be equals to 1. When B is zero, suppose this transistor would not have been there when B equals to 0 is there. So when B equals to 0, this will be acting as a floating node. You are getting my point?

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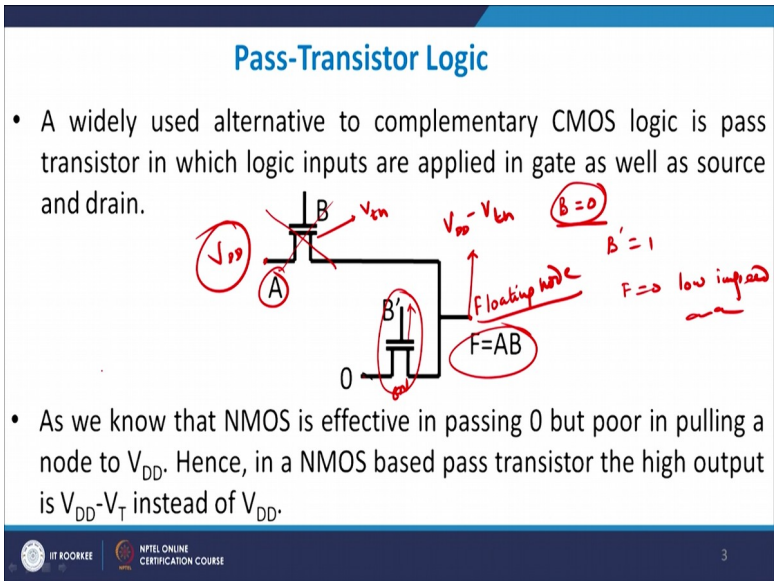

See, suppose we assume that just to give you a brief insight, say B equals to 0.B equals to 0 implies that this transistor is cut off. And suppose this transistor would not have been there in the design, then this node F would have been a floating node, right. Floating node and all sorts of voltage spikes, and everything would have been visible here. So what people thought or what researchers thought was that if you give B goes to 0, then B bar equals to 1 right, which implies that this will be on and when this is on, this is zero will, so your output node will be plugged to 0 which is a low impedance node.

So your output F will be equals to 0 which is a low impedance node. So at no point of time, this F will be a floating node and therefore you will have no problem related to high distortions. So first thing is this one, the second thing is as we discussed with you, the voltage here will be equals to V_{DD} minus V_{TN} where V_{TN} is the threshold voltage of this one and this voltage is equals to V_{DD}, fine. So this is the pass transistor, basic pass transistor logic application.

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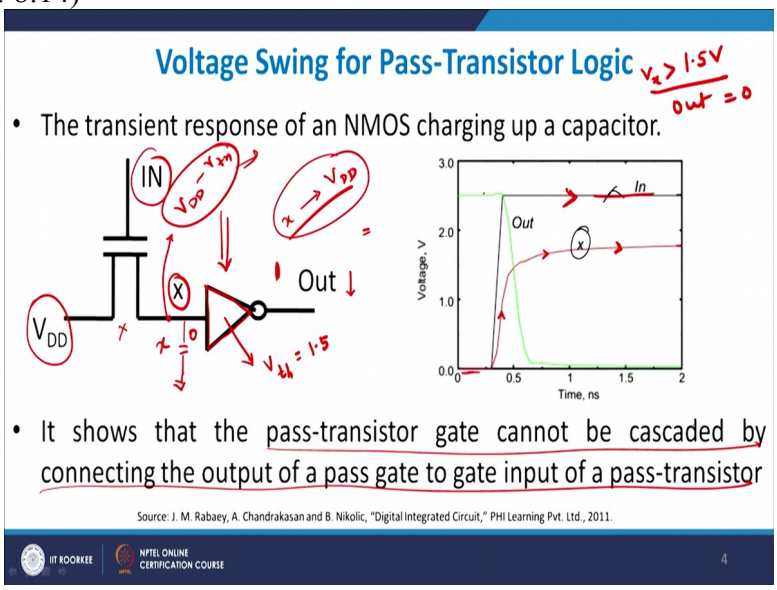

Now let us look at the property of voltage swing in a pass transistor logic, right. So we need to also look into the fact that you do have a voltage available with you and that is swinging right. It is swinging from low to high. So I have an input, so my V_{DD} is given on the drain side, let me define this point source to be point X and then of course, I have a static inverter here and I am giving an input here right and there will be a capacitance, of course there will be a capacitance here, right.

And this capacitance will be charged by virtue of the current here. Now this is the input, this black colour is my input. This black colour which you see here, is my input. Now when the input was low, right, when the input was low right, let us suppose this was low, it means this is cut off. Once this is cut off, the output goes to high. So output is high now right and now the input starts to rise. As the input starts to rise, look at this red one. Input starts to rise which means that X now starts to reach towards V_{DD}.

And that is the reason you see the red coloured graph here, it starts to V_{DD} but what happens is that, beyond a particular time limit, this X latches onto only V_{DD} minus V_{TN}. So your response is V_{DD} minus V_{TN}. So if your V_{TN} is approximately say 0.7, 0.8, you automatically have a lower value of X at this particular point. So when X is high, out will be low at this point. But it can be only low, understand, it can be only low provided the value of voltage at point X exceeds the switching threshold of the CMOS, static CMOS.

Say the switching threshold for this one, V_{TH}, switching threshold, is say 1.5 volts. Then the value of voltage at X should be larger than, so V of X should be larger than 1.5 volts for out to be equals to 0. But what has happened is that X rather than going towards V_{DD} and out therefore going to 0, your X only went up to V_{DD} minus V_{TN}. If your V_{TN} is relatively large for certain reasons or other, this output voltage will not cross the switching threshold and as result, it will be lesser than that and this inverter, static inverter will read it as zero only. And therefore output will be still latched to 1, right. And this is the problem area which you are facing. And therefore, the pass transistor gate cannot be cascaded by connecting the output of the pass gate to gate input of the pass transistor. I will explain to you what do you mean by that.

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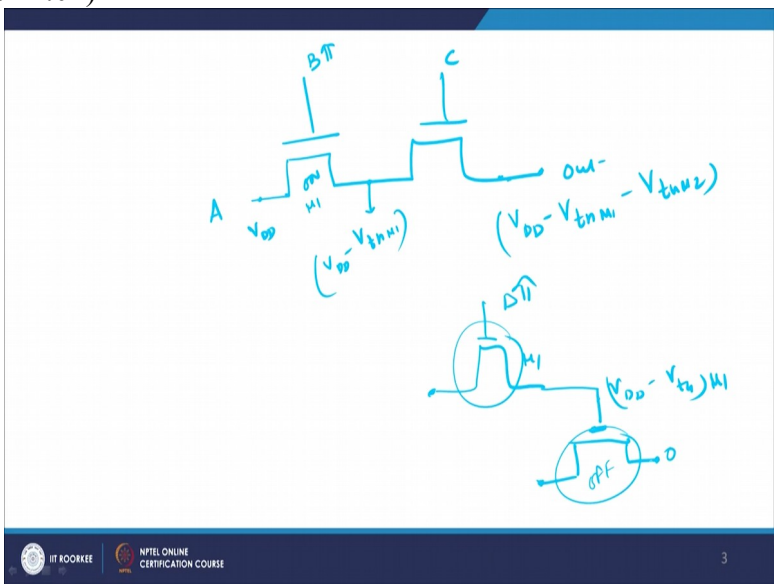

Let us suppose now let us suppose, now I have got two pass transistors connected in this manner right. Is it okay? So this is A, this is say B. This is B. This is C and this is your out, fine. So what will happen is that if this is V_{DD} here, you are given this one high, so this is on. This V_{DD} appears here as V_{DD} minus V_{TN} of say this is M_1, of M_1, right and at this point, it will appear as V_{DD} minus V_{TN} of M_1 minus V_{TN} of M_2 which means that in a pass transistor logic, if you cascade in this manner, then the signal as you move from primary input towards the output, the signal level starts to fall down by one threshold voltage as you cross one transistor.

And in no way you are able to restore it back to its original state until and unless you put a static inverter, right? And that too, I should ensure that the voltage level does not go above or below

the switching threshold, right. And therefore, this type of cascading does not work in a pass transistor logic for large logic designs. This is one problem area which people face. Another problem area is, let me show you what will happen if this is connected as the gate, something like this.

This we have already done, right? And therefore when B is going high, this V_{DD} will appear as V_{DD} minus V_{TN}. V_{TN} of what? V_{TN} of this transistor say M_1, of M_1. And that is the voltage here which is given here. Now if this voltage does not exceed the threshold voltage of this second transistor, this will be switched off and the output will be held to 0 voltage or whatever the original voltage was right. So what I wanted to point you out was that it is very difficult to cascade two pass transistor logics in a similar manner and you need to restore the signal level by simply using a static inverter in between the two transistor levels.

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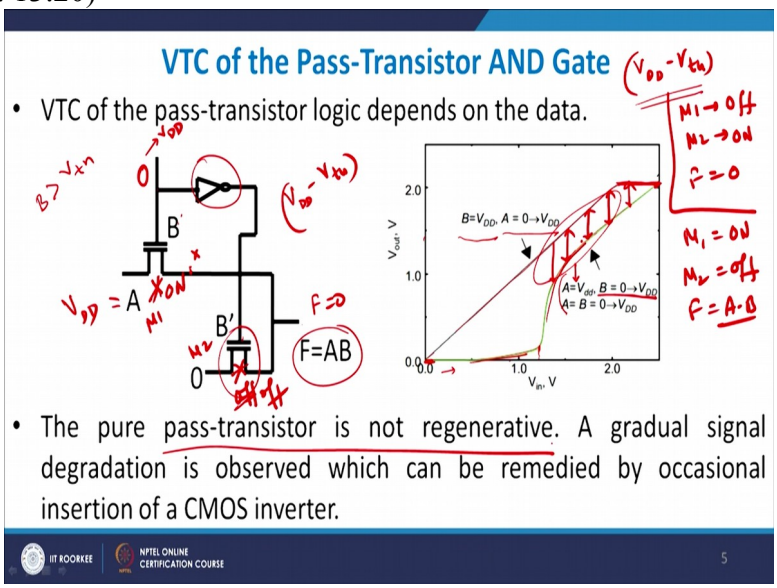

Now let me come to the voltage transfer characteristics of the pass transistor AND gate, right. So AND gate I have already discussed with you. I have got A, B Prime, B and what I am now I am adding is, I am adding this gate output or the obviously, this gate is inverted by this static inverter and I am feeding it at B prime and F equals to A into B. Now you see, suppose B equals to V_{DD} and A goes from 0 to V_{DD}, so therefore when input equals to 0 and as my input starts to increase, this goes on increasing, output goes on increasing, this output goes on increasing right.

And this is a linear, obviously rise will be to you but beyond a particular V_{in} right, how much it will be? V_{DD} minus V_{TN}. You will see that it will be almost saturated and therefore this will be a saturated case. Why is it like that? Because when B equals to V_{DD}, this is switched on. This is switched off of course, this is off right. So A will appear at point X by degrading it by one threshold of the device right, one threshold of the device. But whenever V_{DD} is much smaller as compared to V_{TN}, my V_{out} will follow V_{in} and therefore this will be a straight line path available to you till a point where you reach V_{DD} minus V_{TN}.

At such a point, this device will enter into deep saturation and the voltage will be fixed at V_{DD} minus V_{TN} right. And therefore the voltage is fixed at V_{DD} minus V_{TN}. Similarly, let us look at the fact that, suppose A was equals to V_{DD} and B was equals to going from 0 to V_{DD}, B is this one, right? So it was initially zero and now it is going from 0 to V_{DD} and A has been fixed to V_{DD}. So when initially this was zero right, this will be cut off.

So this transistor will be cut off. As this transistor is cut off, this will be fully on and the output F will be equals to 0. And that is what you are getting here. So whenever your V_{in} is very, very small, output is also small. It goes like this. Just at the point where your threshold voltage of the device is there, when B goes above the threshold voltage of the device, this switches on and then this switches off. Sorry, this switches on and this switches off, yes, off.

So it was initially on and this was, so let me assume this to be as M_1 and this to be as M_2. So initially M_1 was off and M_2 was on and F was equals to 0. Now what has happened? M_1 is going to on state, M_2 is off state and F is equals to A dot B which you see. And therefore you start following this curve in reality. So this is the curve you follow. So as your V_{in} increases, so since V_{DD} is already fixed, I get V_{DD} minus V_{TH} curve till the point I get up to this much right.

B goes from 0 to V_{DD}. So when the voltage starts, so your…this is fixed, B is varying from 0 to V_{DD}. When this B is varying from 0 to V_{DD}, this goes like this right and the reason is that this switches on, this switches off and if A dot B comes into picture here right and that is quite critical or understanding it. So you can see your V_{out} in this case is already down by V_{TN} as compared to the previous state. It is already down by quite a large quantity.

Below V_{TN}, it is already so difference is there, above V_{TN} also there is no difference but around this part, you will have V_{TN} difference between the two, threshold voltage difference is there. So this is the, so as I discussed with you therefore the pure pass transistor logic is not regenerative, means the voltage once lost is gone, you cannot regenerate it and as gradual signal degradation is observed, which can be remedied by the occasional insertion of a static CMOS inverter because inverter will either latch it to V_{DD} and zero and therefore you have to insert V_{DD} resulting in a larger power dissipation.

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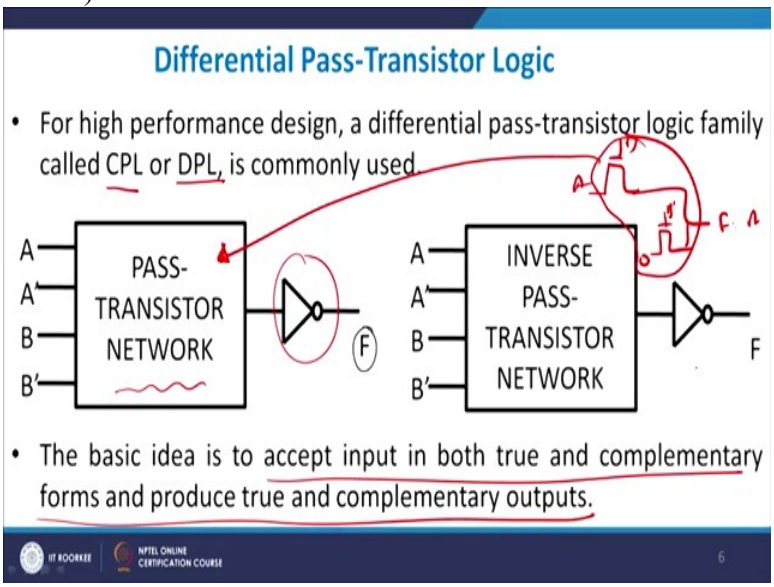

Now, typically when you do a high-performance design, we use a differential pass transistor logic in which we assume that my input and its complements are available to me. So A, A bar, B, B bar, C, C bar, are all available to me and I do a pass transistor network here and then I put a static inverter to get a full swing in the output side.

Now the basic ideas as I discussed with you accept the input in both true and complementary forms and produce a true and complementary outputs. So the output will also be a true and complementary one. Well, that is simple because you do have a static inverter here, right? This is also referred to as a differential pass logic or even a complementary pass logic here right.

Differential, most common is the differential pass transistor logic or DPL or DPTL right and it gives you quite an interesting result as far as this is concerned. So what is this pass transistor network? The same thing which we just now studied that there is you have got A, B right and

then it comes like this and then the same thing which you have done. So this is B prime, this is B, this is A and this is zero. So F equals to A into B. So this whole thing which you see is inserted in this black box, right. And I will term this as a differential pass transistor logic.

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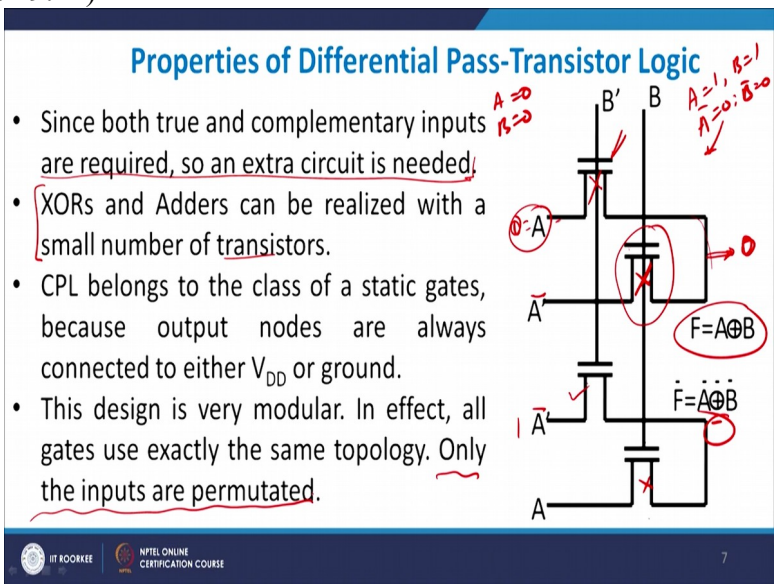

With this knowledge or with this idea, let me come to the next one that let me take up the properties of differential pass transistor logic and let us see how it works out. So since both true and complementary inputs are required, so extra circuitry is needed just to complement the signal. So I require an extra static inverter to complement the signals. Of course, XORs and Adders can be realized using small transistors, one example is given here where XOR and XNOR are designed.

So you can see here, when A, I have got A, A bar, A bar, A right? So and this is, so if your A equals to 1 and B equals to 1, then what will happen is that when A equals to 1, this is 1. So your A bar will be equals to 0 and B bar will be equals to 0. So this will be zero means this will be cut off right and B equals to 1 meaning this will be on and therefore A bar will appear in the output side here, A bar. And therefore that is nothing but zero, right.

Which means that when A and B are both equals to 1, I get a zero. When both are 0 0, sorry when equals to 0 and B equals to 0, so A equals to 0 and B equals to 0 implies that this is cut off now, this one is cut off. So with B equals to 0. With A equals to 0, what will happen is that, with

A equals to 0 sorry. So with A equals to 0, what will happen is that this will be 0, of course 0 and B prime will be 1. So this will be switched on. So I will have 0 coming into picture here and when B prime equals to 0, this will be cut off.

So B prime will be 1, this will be switched on. And B will be equals to 0, this will be cut off and A bar will appear here, so 1 will be appearing here, right? So if I want to find out XNOR, XOR I will get this. If I want to find XNOR, I will get this into consideration. So I can have an XOR bar here, right. And so we just need to permutate the inputs in the proper manner so that I get the proper output here, right.

However, as I discussed with you, there will be always a problem of signal degradation between the pass transistor logic input and output and therefore cascading this across a large number of logic is a futile exercise because everywhere you will get one V_{TN} drop and if that exceeds the switching threshold of the static inverter, I will actually read 0 as 1 or 1 as 0 and that is quite a important problem area which you will see.

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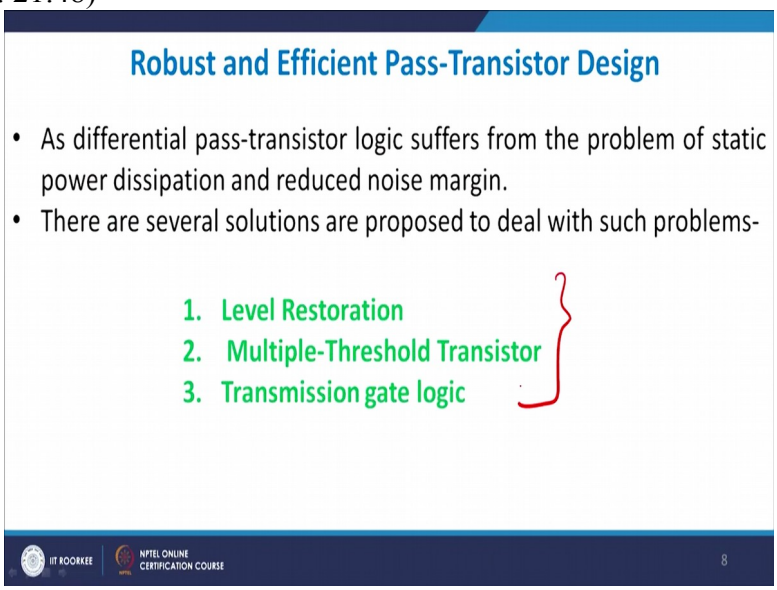

Now as I discussed with you, differential pass transistor logic suffers from the problem of static power dissipation. Why power dissipation? Because now you are directly allowing the output to see the input right and therefore there will be a large current and therefore this will result in a larger power dissipation. So there are certain solutions which is level restoration, multiple

threshold and transmission gate. We will take each one of them and explain to you how it works out.

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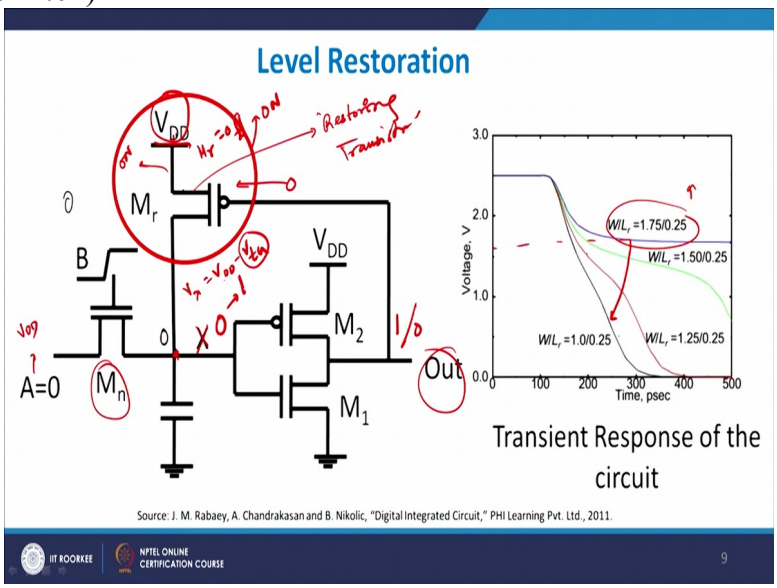

Say for example, I have a level restorer. Means I want to restore the level at the inputs. So this is my static inverter here. Just like an AND gate, I have A and I have B here and I have this is M_n and X is the point, this particular point and this is the output here. Now you see, when this is equals to 0 right, when this is 0, this will be 1 and therefore M_r will be equals to off. When this is off, this will be again 0 because you are connected to the ground through this capacitance.

Now when X equals to 1, sorry X equals to yes, 1, this will be 0. This will be 0 means this will be switched on. When this will be switched on, this V_{DD} will appear at this particular point and try to pull the value of voltage here above V_{TN} because if you see, this is A equals to 1 means A equals to V_{DD}. Then my V_X will be equals to V_{DD} minus V_{TN}. V_{TN} is the threshold voltage of M_n. Now this will switch on my transistor and as a result, this will be zero. When this is zero, this will switch on my M_R and this V_{DD} will be connected to ground and the loss which you get through V_{TN} will be made up by this V_{DD}.

But please understand the loss V will give you is that at that particular instant of time, when your MR is on, you have a direct connection between V_{DD} and ground. And therefore your short-circuit power dissipation will be larger in such a case, right. And that is, this is known as level

restoration at the cost of a slightly higher power dissipation. You see, therefore as the W by L ratio of the, this is known as restoring transistor. This is referred to as a restoring transistor.

So as the aspect ratio is increased, which means the W of the restoring transistor is increased, the voltage level at this particular point is not allowed to fall drastically. So when you reduce your W, it goes down to almost 0 but as you increase the value of W from 1 to 1.75 with L fixed as 0.25, the voltage is actually latched to a value approximately 1.75 or approximately 1.60 or something like this. So you got the principle correct that, so why is it like that?

Go back to my previous module to appreciate this point that when your aspect ratio is large, you have made the device stronger, higher current is flowing through the device and therefore the output voltage which this was trying to go to the ground is now pulled back, is pulled up by the M_r, restoration transistor and therefore you see this is what do you get, the profile which you get right. And therefore, you are not able to get the peak to peak swing so at the cost of that you are able to restore the internal level at node X.

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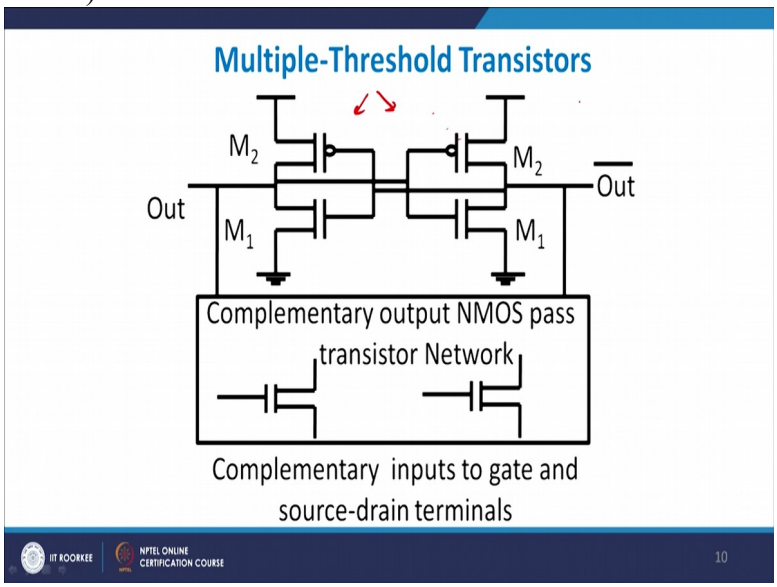

Let me come to multi-threshold voltages. What we do here is that we have a, so this is basically your two cross coupled inverters connected back-to-back right and I will get out and out bar and then this is complementary output NMOS pass transistor logic, right. So what we do is that we try to make the threshold voltages of this one slightly larger as compared to the threshold voltage of the devices kept inside the complementary NMOS pass transistor logic.

Once you initiate that or once you have that into consideration, you automatically are able to correlate or able to do some amount of correlation between the output at this stage and output at this stage, right; so basically what we do is that we try to keep the complementary output module threshold voltages much lower and we try to keep the threshold voltages of the cross coupled inverter much higher right.

And what it does therefore is that report if it is much higher, they are more strong and therefore the voltage of out and out bar are actually latched to its value and these cross coupled inverters try to stick to these values in a proper manner, right. So this is the advantage of having a multiple threshold transistors.

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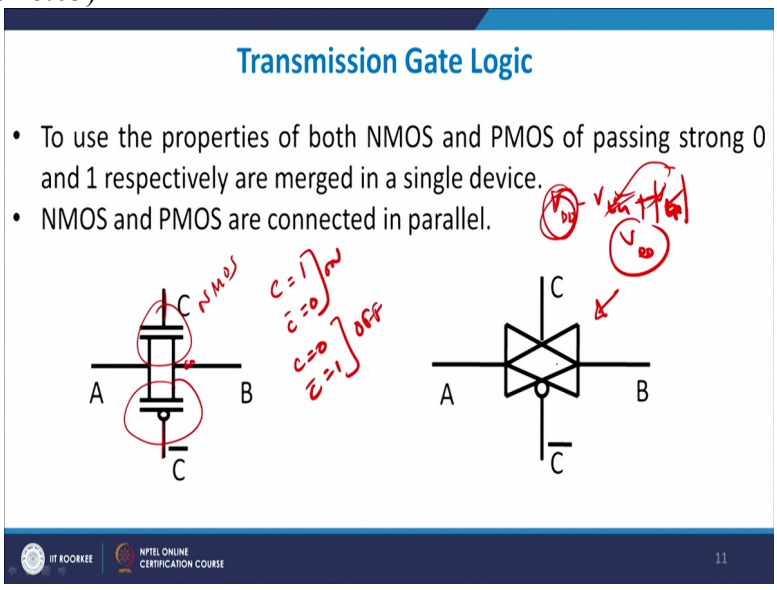

Now let me come to the last part of the or sort of, this is transmission gate and transmission gate is very simple straightforward. You do have an NMOS here, right? You have an NMOS here. For AND, a PMOS in connected back-to-back. This is driven by C and this is driven by C bar. So whenever my C equals to 1 and my C bar therefore equals to 0, I ensure that this is on right, on. And whenever C equals to 0 and C bar equals to 1, I will assume it to be off or it will be off also in a sense because you see when C equals to 1, this NMOS on and C bar equals to 0 means this PMOS is on.

So both the transistors are on and you have a direct connection between A and B. When C equals to 0, C bar equals to 1, this is cut off and therefore there is a high resistance between source and drain of this transistor and therefore A and B are disconnected with respect to each other right. And therefore they are connected in parallel and they are driven by one clock or one data input, C and its C bar, it's complementary.

This is the schematic which you see here. Remember why do we do a TG is very simple. You remember that NMOS was a good puller of 0 and PMOS was a good puller of 1. We have already seen that point. Now therefore if you combine the two together, two transistors together, then both of them cancel each other's domain assuming the threshold voltages are exactly equal and the whole transistor is able to pull the input node right till V_{DD}, right.

So what you will get in the output side is something like this. You will get V_{DD} minus V_{TN} right and then you will subtract V_{TN}. So you will add V_{TN} here and this cancels up and you get V_{DD} in the output side. So we add mod of V_{TP}. Now assuming that mod of V_{TP} equals to mod of V_{TN}, these two gets cancelled off and I get again V_{DD} in the output side. Right and that is a standard way of looking at a transmission gate.

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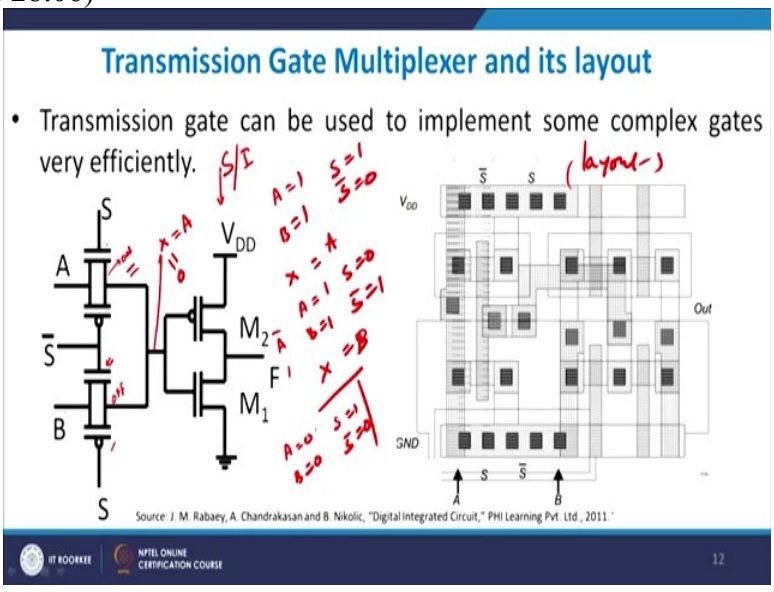

I will show you how I can implement this logic gate and let us see how it works out. I have this, this is basically a static inverter. This part is static inverter. Let us suppose A equals to 1 and B equals to 1 and let us suppose S is also equals to 1, then S bar equals to 0. So when S equals to 1,

S bar equals to 0, right, my this point let us suppose this is X, X will be equals to, so when S equals to 1 and S bar equals to 0, this is on right and this is off. If this is on, then A will appear in the X. Fine.

Similarly, if A equals to 1 and B equals to 1 and S equals to 0 and S bar equals to 1, what will happen? S equals to 0 and S bar equals to 1 primarily again means that this will be on, right S bar equals to 1 and S equals to 0 means B will be on. And X will be equals to B. Fine. And X will be equals to B. Is this conceptually clear? Right and there will be no drop in the voltage. In fact, there will be no switching of the voltage from V_{DD} to V_{DD} minus V_{TN}. It was still remain the same.

Similarly, if A equals to 0, B equals to 0 let us suppose and S equals to 1 and S bar equals to 0, in that case what will happen? If S equals to 1 and S bar equals to 0, means this condition will be there and A and B are both equals to 0 implies that this will be switched on and therefore X will be equal to 0, right. And therefore I can get all sorts of logic principles here. Now 0 will be obviously will be made equals to 1. When you have A, you have got A bar consider here. So I can implement certain logic gates in this case.

Just tell me what this logic gate will be all about right. You need to find out. You yourself do it and need to find out. This is the layout. On the right-hand side is basically the layout of this logic gate. It is quite complex in nature because you are using multiple gates with multiple clock loading. And that makes life difficult for us.

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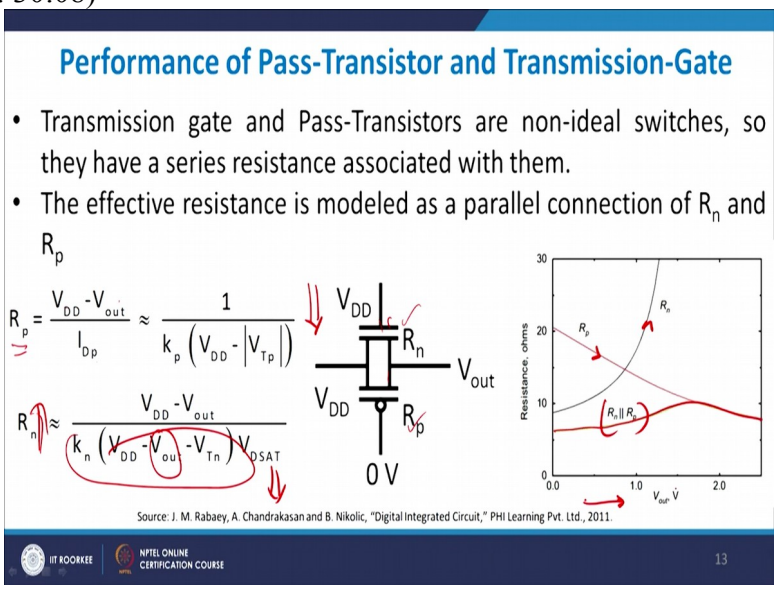

Let me come to the performance of the transmission gate. So remember, transmission gate is made up of NMOS and PMOS. This is NMOS and PMOS. So you see, R_P which is the resistance of PMOS will be V_{DD} minus V out by I_{DP}, where I_{DP} is the current flowing through the device which is approximately equals to 1 by $K_P V_{DD}$ minus mod of V_{TP}. And similarly, R_n is V_{DD} minus V_{out} upon K_n minus V_{DD} minus V_{out} minus V_{TN} into V_D sat, assuming that both are in the saturation region.

So you see, therefore as the input or the output voltage goes on increasing right, the NMOS resistance goes on increasing. The NMOS resistance goes on increasing. And the reason is that this value of voltage goes on increasing means this whole thing starts to decrease. As a result, RN goes on increasing, whereas RP actually starts to decrease with V_{out} going high and high. And that is see here, red curve.

So the overall curvature of R_n parallel to R_P because these two are parallel in dimension, is something like this in the green curve almost independent of the value of V_{out} and that is one of the major advantages of a transmission gate that the transmission gate output or the effective resistance offered by a transmission gate is almost independent of the value of the signal which you give, right.

Whereas for all other cases, it happens to be a strong function of the signal, right and that makes my life easier as far as performance of the pass transistor logic is concerned. So we have

understood the pass transistor logic, we have also understood the complementary logic, we have also understood the PTC which is pass transistor logic as well as transmission gate logic. So for reduction in the transistor account, we use pass transistor.

For example, an AND gate would require 4 transistors assuming the complement is also to be taken out for one of the signals. Whereas when you use a AND gate for your CMOS transistor, it takes six transistors into consideration. In a differential pass transistor, I will assume both true and its complementary inputs and both types of output, true and its complementary output is formed. Typically as I discussed with you, when you do a pass transistor, there will be a fall in the voltage.

To remove that, we use a level restoration circuit. We can also use a multiple threshold circuit or we can use a transmission gate, either of the three. The problems with these logic designs are that they might replace CMOS but they are not as robust as your CMOS is. So they are not too much preferred in your logic domain or in design domain, right. In some cases, we do use transmission gate based but then you are actually increasing the number of transistors in that case, right and your clock load also starts to increase.

With these words, we have therefore understood the basic difference between PTL, pass transistor logic and transmission gate, we have also understood what is a pass transistor logic and how is it depending on the value of threshold voltage, what is the meaning of cascading of logics and how can I remove the problem of a loss of signal using level restoration circuits, right. With this, we finish this module and we will come back in the next module with other explanations. Thank you.