Microelectronics: Devices to Circuits
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Lecture 52: Large Signal Operation of Op-amp and Second Order Effects

Hello and welcome to the next edition of NPTEL online course on Microelectronics, devices to circuits. We will start today's module on last signal operation of operational amplifiers and second order effects. The reason for doing this module was that typically as of now we are assuming that the input to the signal or input signal to the operational amplifier's peak to peak values are relatively small and therefore even when you multiplied that with the open loop gain of the operational amplifier, it never crosses the values of plus V_{cc} and minus V_{ee}.

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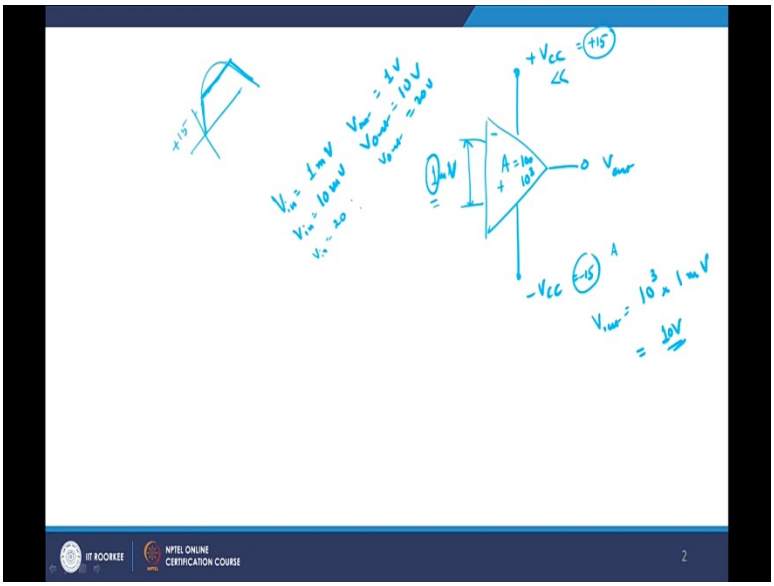

Remember in my previous discussion which we had during the starting of the module on Operational amplifiers, you will understand or you will notice that whenever you are dealing with Op Amps, your op amps are primarily having a negative and a positive terminal and you also had plus V_{cc} and minus V_{cc} or minus V_{ee} and you had one output terminal here. Now if you multiply typically A, say suppose this is equals to plus 15 and this is equals to minus 15 and if the difference between the two signals is say 1 milli amp, 1 milli volt let us suppose and A is equals to 100 or maybe even 10 to the power 3, so I get output V_{out} to be equals to 10 to the

power 3 into 1 milli volt. So that becomes equals to 1 volt, now 1 volt is much smaller as compared to V_{cc}, right.

Similarly, if this now comes out to be 10 milli volt then I get 10 volt as the output, so if this is, so V_{in} is 1 milli volt, I get V_{out} to be equals to 1 volt. If V_{in} equals to 10 milli volt, I get V_{out} to be equals to 10 volt and so on and so forth. Now therefore if this Vin is let us suppose say 20 then my V_{out} should be equal to 20 volts but that exceeds this value here and here which means that my output waveform which I will get will be much larger than plus 15 which is being said by the power supply.

So I am basically allowing the device to trip and therefore there will be the output waveform will be clipped at plus 15. Now what we will be studying in this module is that thing only that given a possibility that you do not, you let the whole system to saturate and you allow the voltage to go beyond the permissible values then how does the operational amplifier behaves. So that will be the major goal of this study.

Before that let me give you a small problem and you might try to solve it, the methodology I can give it to you. Say I have an input, this is regarding an integrator right. So I have an integrator in which the input waveform, this is t is equals to 0 and this is t equals to 1 millisecond and this is equals to 1 volt. So in an integrator I am giving a square wave, just like as input waveform whose peak value is 1 volt and whose width, pulse width is 1 millisecond and you need to calculate how it looks like, so how it looks like we need to calculate.

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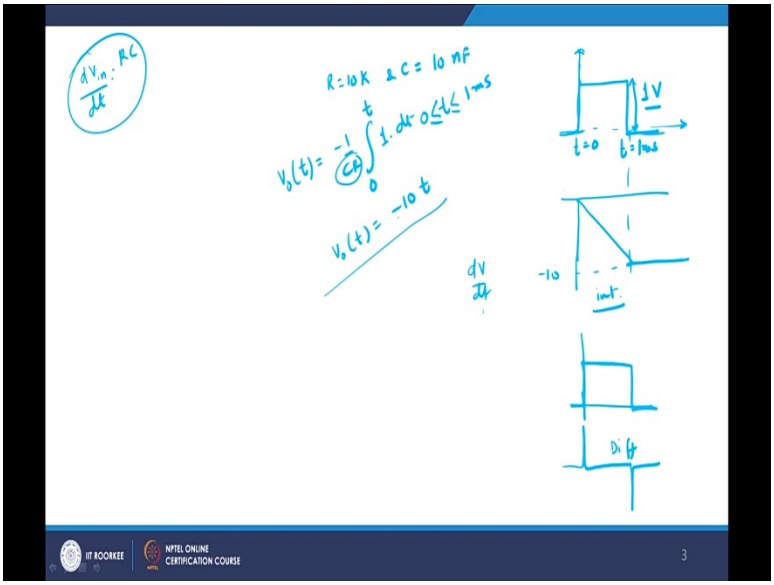

Let me draw for you, so before that if the resistance is given to be as 10K and C is given to be as 10 nano farads. So I get V0(t), right is equal to 1 by CR integral 0 to t 1 dt where t is between 1 millisecond and 0. So if I solve it I get V0(t) to e equals to minus 10 t by putting the values of C and R. So if you look very carefully this is basically a negative sign with a 10, so it will be a ramp so and the voltage goes like this, this will be typically a ramp here, ramp till how much, minus 10 volts and after this it will be a straight line once again right, there will be 0, sorry it will go to, it will go to 0 here.

Why it will go to 0 here because see here you are integrating, you are integrating it right? You are integrating it, so when the, so this is what you get as far as integration is concerned. This is how it looks like right, so integration of a constant value will give you a constant output and that is the reason we will get it, whereas if you look at the differentiator for example, differentiator is basically dVin/dt into RC, well that is how you look into the differentiator which means that in a differentiator if you get a constant. For example, the same profile if I ever got, this is the input then the rising edge right, rising edge my dV/dt would have been very large, so I would have got a spike here, but when my voltage goes to constant, then constant differential is always 0 and therefore this will, I will just see a spike here and then I will since it is coming down I will see a spike here.

So a differentiator looks something like this and integrator looks something like this. So this is a pretty wonderful method, differentiators are pretty wonderful methods for generating spikes out of given waveforms but differentiators are very seldom used because they influence large amount, they insert large amount of noise because of electromagnetic interference and so on and so forth whereas integrators do not do that. So just for information's sake this is in consonance or in continuation of my earlier discussion as far as this course was, as far as this course was concerned.

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Let me come to therefore the next part here and let me come to the large signal operation and let us go step by step what we will be doing here. So we will be looking into large signal operation of op-amp, we understand what is a slew rate, why is it important as far as designing is concerned, in operational amplifier design is concerned. We will also look into one important point that we are assuming till now that your loop, your gain is infinitely large and your bandwidths are also large but in reality your bandwidths are always restricted bandwidths right, and gains are also restricted. And therefore under such a scenario how will your open loop gain change and how will your input impedance and your output impedance change.

We will also look into Frequency Response, Gain Bandwidth Product, the concept of Offset Voltage and the concept of Offset Compensation Voltage and then a Bias Current, right. We will

take one of them individually and understand, try to understand the basic features of these individual voltages or understand the basic concept, right.

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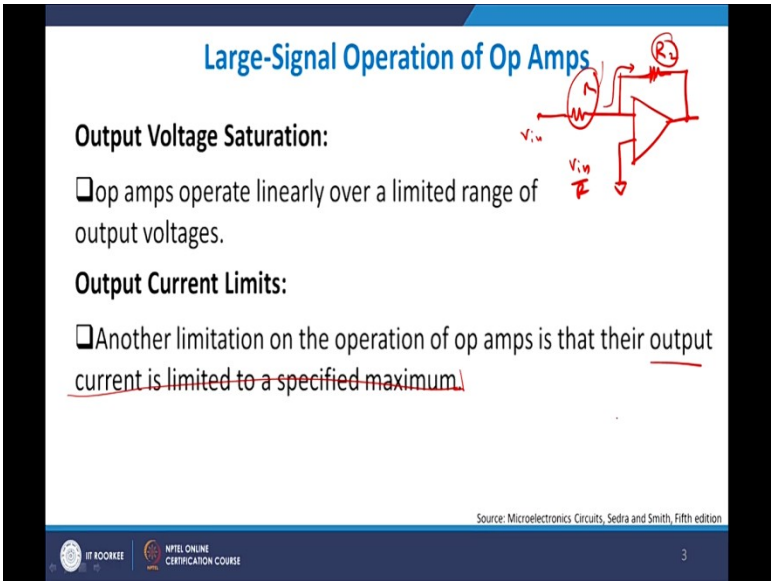

You see we had just now discussed that an operational amplifier if you give an input voltage, my output voltage will be as I discussed with you, difference of the two voltage multiplied by a which means that if the difference remains the same right, that my output voltage will be independent on the both the voltages. I hope you understand this point, because A into V_2 minus V_1. As long as V_2 minus V_1 is held constant and I do not mind and my V_0 is constant, output voltage is constant.

This is basically sort of a linear property of the device which primarily means that in such a scenario your amplification is independent of the input voltages but then operational amplifiers remain linear for a limited range of output voltages right and what happens is that as you reach towards plus V_{cc} and minus V_{cc} in the output side, you try to drive or or the signal tries to drive the operational amplifier into saturation, right. As it enters into saturation, there is a problem and the problem is non-linearity comes into picture to a larger extent.

Now another limitation of the operation of operational amplifier is that the output current is limited by the maximum specified value which means what, an operational amplifier remember, output current is given by even if you take an integrator or a differentiator. So if you see it will be resistance here and the capacitance here right, or maybe the inverting one will be much easier

to understand so I have got R_2 and R_1 here, as I discussed with you suppose this is V_{in} then V_{in} by R is the current flowing through this resistor but since this is a virtual ground I would expect to see all the current to move to this R and therefore R_2 will also have the same current here, the same current will reach at the output of the current.

But please understand the total output current is limited by power dissipation of operational amplifier right, so operational amplifiers are designed to operate at optimal power dissipations. Now if the current is very high right, it might trouble the operation of an operational amplifier and therefore you always have a limit on the total amount of current flowing through the operational amplifier in the output loop factor. So this is one problem area which people face.

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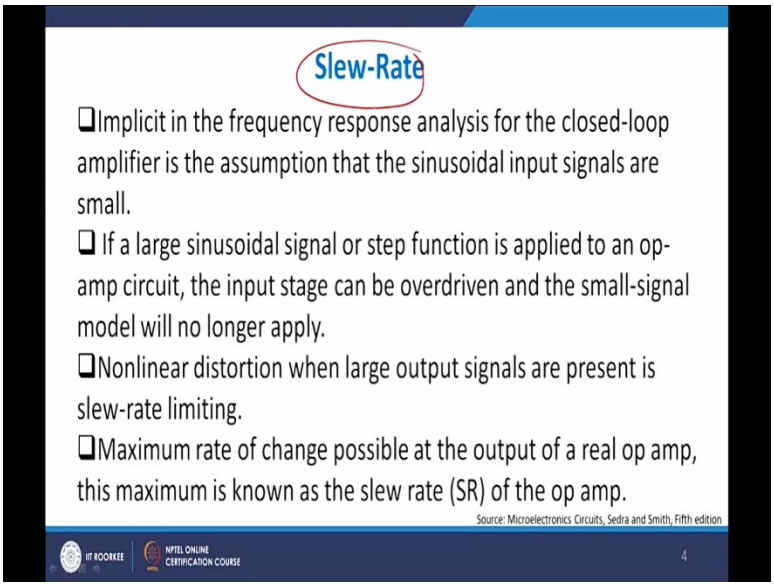

The third problem area is of the slew-rate, you would not be as far as designing is considered in most of the cases if it is a small signal you would not be having these problems coming in the picture but whenever you have a large-signal model for operational amplifier you might have these problems. Slew-rate is primarily if you look very closely, look at the second point will give you a give you an idea. If a large sinusoidal signal or a step function is applied to an operational amplifier circuit the input stage can be overdriven and the small-signal model will no longer apply, as I was saying to you.

Now if there is a heavy non-linear distortion when there is a large distortion signal, then we define it to be the slew-rate limited signal. So how do you define slew-rate, the maximum rate of change at the output.

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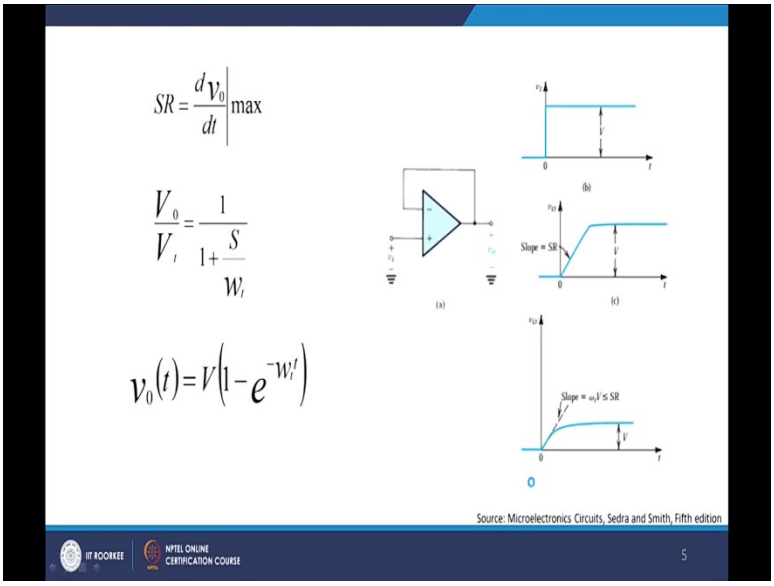

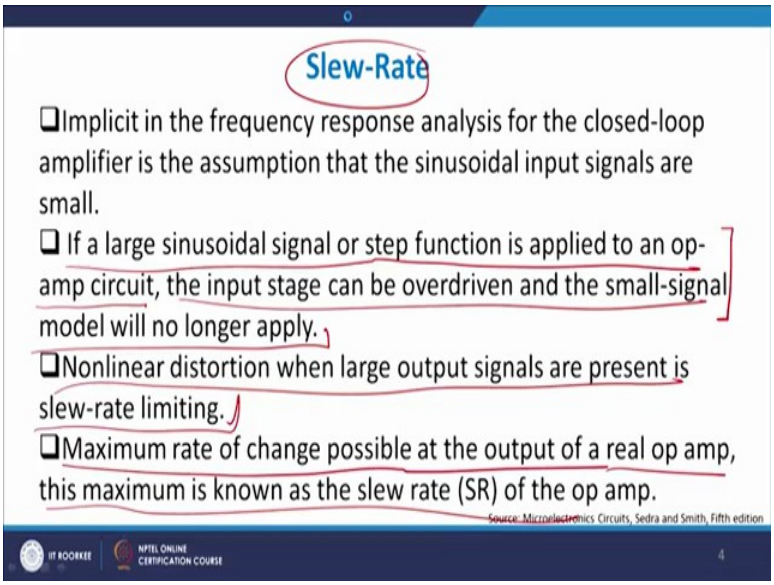

The maximum rate of change possible at the output of a real op-amp is known as the slew-rate which means that let me just show you then we will come back here. This is my definition dV_0/dt means the rate of change of output voltage with respect to time, the maximum it can sustain and why I am saying the maximum it can sustain is there is certain specific reasons for that.

The maximum, the reason for that is that the variation of the voltage with respect to time may may, let it be at input or output is always governed by the RC time constant of that particular point or that particular node, so you cannot expect that if I give an input which is suddenly rising like a step voltage, you would not expect that the same performance will be at the output of your operational amplifier, it will be always delayed and there will be always a RC time constant available to you at the output side right, so we define slew-rate as the maximum rate of change of output voltage with respect to time which the operational amplifier can safely sustain. You make it slightly larger than that output variation and you would not get any change in the output cycle right or it would not be or will be actually slew-rate limited output supply.

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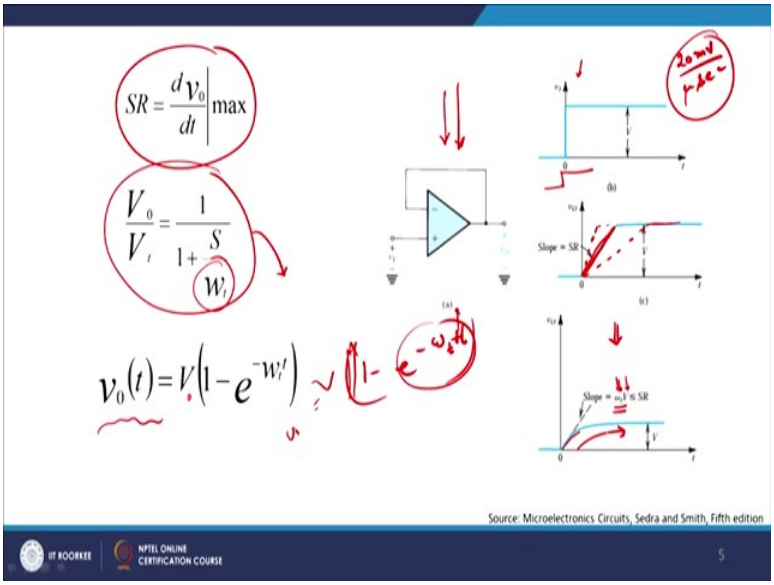

So as I was discussing with you let us suppose I have a voltage follower right, I discussed this point or I discussed this circuit in your previous turn as well and let us suppose I have a voltage follower. In this voltage follower I give a step input which is given as V_I, what I am seeing is that because of the step input ideally I would have seen the output to follow the input because it is given to the positive terminal, non-inverting terminal and therefore output should ideally follow like this but because op-amp has got a problem, therefore output will always be a like this which means that it will flow or it will rise at the maximum pace.

So if the slew-rates are large it will be like this, if the slew-rates are small, it will be something like this, you got my point. Therefore, these are known as slew-rate limited operational amplifiers right. So they will tell you that it is basically 20 milli volts per second or per microsecond which means that for every one microsecond change in the output I would expect to see a 20 milli volt change in the output voltage that is the maximum that the op-amp can sustain. Anything larger than that it cannot be sustained with operational amplifiers, right? So this is the basic concept here which you see.

Now as I discussed with you, therefore, if you look at the curve which is the last one here then this slope which you see that means it will be slew-rate limited then this slope gives you the value which is the ω_T into, ω_T is the unity gain bandwidth frequency multiplied by voltage must be less than equals to slew-rate. So so this we will discuss later on if time permits. But ω_T into,

ω_T into V is the input voltage given is basically the rate of change of my output voltage and that should be always less than the slew-rate, then you will get such type curve in reality, right.

So I get V_0 by V_t, V_0 is the output voltage by V_t which is the input voltage is 1 by 1 plus s by ω_T where ω_T is basically the 3 db bandwidth frequency, so if you do transform, Laplace transform of this one you get V_0, inverse Laplace transform sorry, you get $V_0(t)$ equals to V_0 into 1 minus e to the power minus ω_T. So 1 minus e to the power minus ω_T into t into V_0 is equals to V_0, so you see as the time increases this quantity will drop down this quantity will increase and that is what is happening, fine. So this is Slew-rate dependent phenomena which you see.

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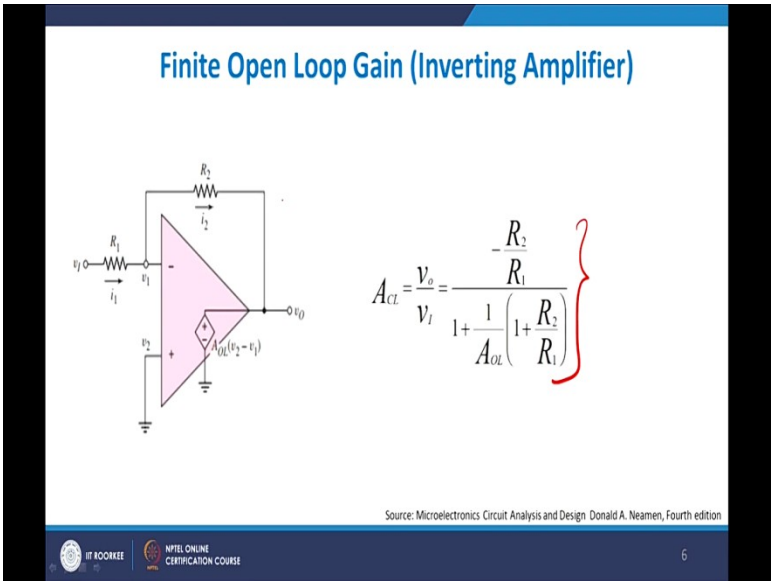

Now if you, what we were discussing in the previous turn was that if you have an inverting amplifier, I mean inverting amplifier, then the output will be 180 degree phase shifted with respect to input and therefore you put a negative sign in your closed loop gain. So I get A_{CL} equals to minus R_2 by R_1, remember? Now what has happened is that my loop gain or my gain was considered to be very high right and therefore my, but if it is not high and it is restricted by a certain value, for example A_{OL} which is the open loop gain, then the closed loop gain is related to the open loop gain by this this factor, right? And this is what I get; this is what I get as the difference in the open loop gain and the closed loop gain.

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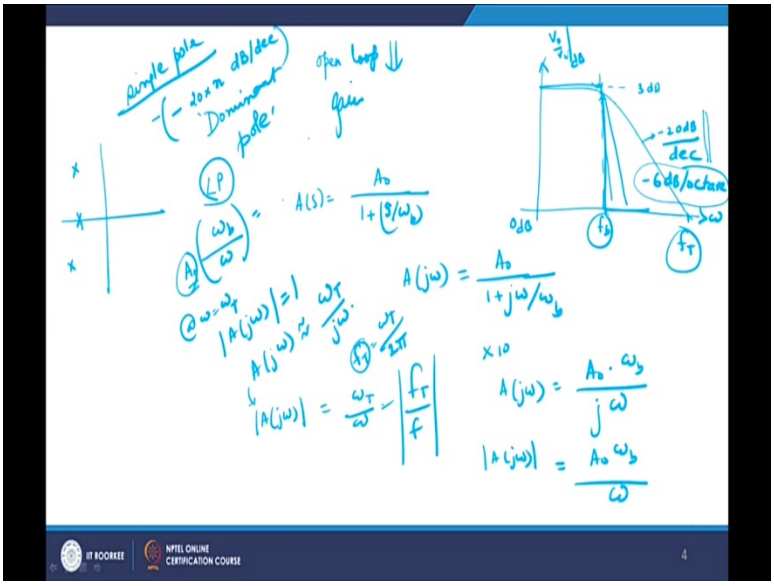

So just to show you this basic concept as far as effect of finite loop gain is considered. Let me just show it you what I am talking about and let me show you how it works out that, let us suppose I have a filter whose output characteristics look something like this so I have, this is basically your, this is your 3 dB bandwidth or 3 dB point and the voltage is defined as f_b let us suppose where it cuts is defined as f_T unity gain because it is 0 dB, this is my gain V_0 by V_i in dB and this is my ω in terms of frequency we will get some value.

Now so what I am trying to tell you is that open loop gain, open loop gain, let us suppose it drops down or it falls then how does it influence my in this thing. So I have a low pass filter let us suppose and transfer function is given by A(S) equals to A0 upon 1 plus s by ω_b, where ω_b is basically my this frequency here. So in terms of jω I get, I just replace S by jω I get A_0 upon 1 plus jω by ω_b, right?

So, so what I am trying to tell you is that let us suppose now you assume that your frequency is increased by 10 times as compared to ω_b, so I am somewhere here right, then I get A of jω equals to A_0 into ω_b by ω, got the point, jω, why because if ω is very very large as compared to ω_b this quantity will be very large as compared to 1 and I get A_0 into ω_b by ω s equals to A of jω right? So if I take the mod value of a of jω then I get this to be equals to A_0 ω_b by ω.

So I get the gain to be equals to A_0 multiplied by ω_b by ω. A_0 is fixed because that is open loop gain multiplied by ω_b by ω. This is my sort of a closed loop gain and a finite loop gain which you see, right. So this gives you a value, now at ω equals to ω_T where you have got a unity gain bandwidth product I will automatically have this equals to 1 and therefore a of $j\omega$ will be approximately given as ω_T by $j\omega$ because this is 1 ω_b will convert to ω_T and ω_T by $j\omega$ I get where f_T will be given as ω_T by 2π, right?

So this is your unity gain unity gain bandwidth frequency right? And therefore if you want to find out this, if you want to find out the this the magnitude of A of $j\omega$ from this case right, I get this to be equals to ω_T by ω, this is nothing but f_T by f. So it is the ratio of the unity gain frequency divided by the frequency at which you are trying to find out the gain, the ratio of that will be equals to your gain right at that particular frequency. Now that is with the consideration that your finite loop gain is already available to you.

Now generally if this is a single pole dominated transfer function, single, if there is a single pole on the left half plain, then you will automatically this will be around minus 20 dB per decade or minus 6 dB per octave. So please try to find out why it is 6 dB per octave, I leave it as an exercise to you but you can ask questions later on through the discussion forum but try to find out why it can be also referred to as minus 6 dB per octave or minus 20 dB per decade provided you have a single pole on the S plain.

So if you have a single pole here then we define that to be as a this thing, if there are multiple poles, for example this complex conjugate poles here so there are two poles, so it will be 20 times n dB per decade. I will not derive it here, so this is minus 20 times n dB. So you multiply 20 with the number of poles, so if there are two poles, 40 dB per decade. So you would expect to see a steeper fall. So larger the number of poles right, more steeper will be your fall in the low-pass filter and better will be your characteristics, you will be reaching to the much.

So the ideal characteristic is something like this right, for a low pass filter. So now you will get much more better because this fall will be very fast here, so which means higher number of poles means higher order of your filter, you automatically get a larger and larger value of your input profile and that is what is known as a dominant pole approximation. This is known as a dominant

dominant pole, right? So this is as far as understanding the dominant pole approximation is concerned.

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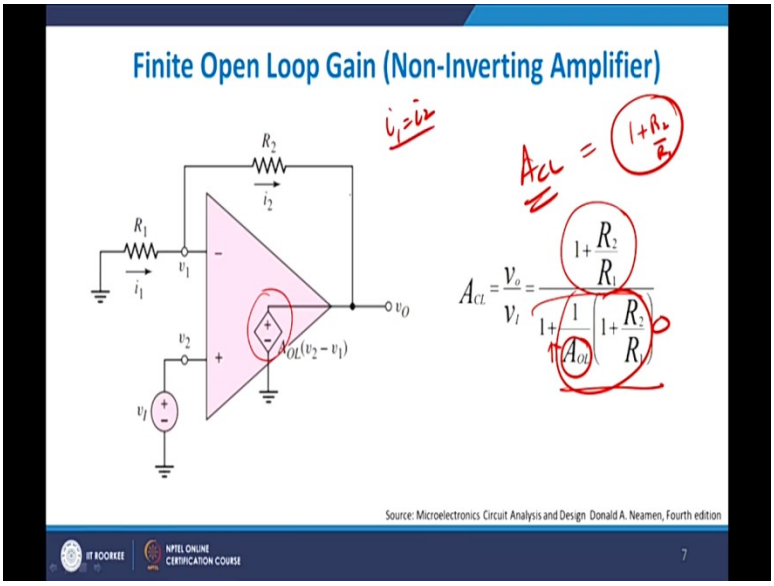

Now if I take a closed loop control or a closed loop consideration I get R_2 by R_1 into 1 plus 1 by A_{OL} 1 plus R_2 by R_1. I am not deriving it in the class but this is what you get out of it. Now you see if your open loop gain A_{OL} is extremely high or infinitely high then this quantity, this quantity goes to 0 and I get again R_2 by R_1 which is basically my initial inverting mode, remember, inverting mode operational amplifier. Got the point?

So when your open loop gain is very very high 10 to the power 7 in the ideal cases, you get a closed loop gain almost near to R_2 by R_1 but if your A_{OL} is not very high it is 10 or 20 or 30 or 40 whatever, then these also lower your overall closed loop gain right and that is the inverting amplifier case.

Let us look at the non-inverting amplifier case, exactly the same only thing the numerator is replaced by 1 plus R_2 by R_1 and you have denominator given as this similarly if A_{OL} goes to a very high value, this quantity this quantity goes to 0 and therefore I get 1 plus R_2 by R_1 as the value of your A_{CL} closed loop gain, right? And as you can see that for the small signal model this has been replaced by a voltage source of a value A_{OL} into V_2 minus V_1, fine.

And this is the current source so I am assuming that so I will be assuming that I_1 equals to I_2, well assuming or it is true in a sense true also because this is basically high impedance node available here, right? So I have a finite open-loop gain that gives me a non-inverting amplifier here.

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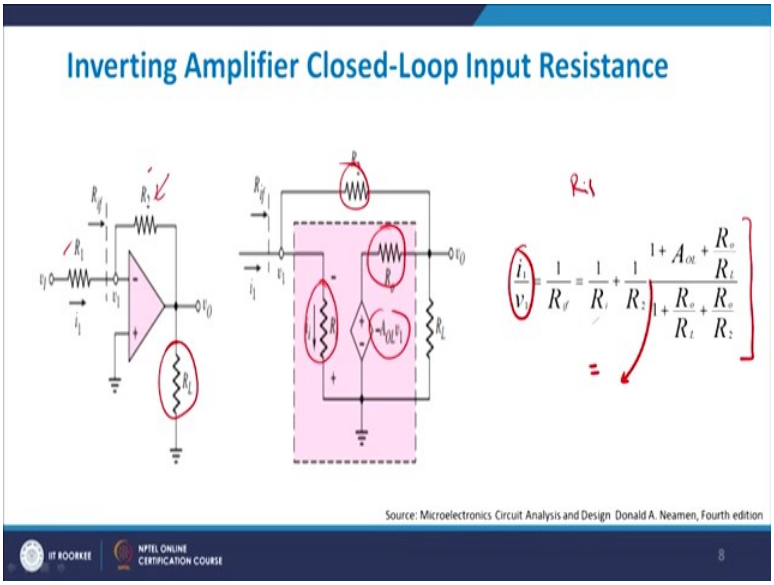

Now if I want to find out the inverting amplifier closed loop input resistance then I have to find out R_{if} which is I_1 by V_1. Now if you look at this this thing here, so I have got R_1, R_2 and let us suppose I have a load resistance R_L. This can be made to equivalent small-signal models, so this is my input impedance R_i, this is my R_2 which is the feedback resistance here and I have got output resistance R_0 and minus A_{OL} into V_1 because you are inserting your signal into the inverting terminal and therefore minus A_{OL} into V_1, why V_1, because V_2 is grounded. So I get minus A_{OL} into V_1 into R_L is the external node.

If you solve it by doing simple simple derivations I get this the overall picture as the input resistances, so sorry so I get this plus sorry this will be equal to, so this will be here equal to right and I get, 1 over that will give you the value of your R_{if} input impedance for the closed loop gain.

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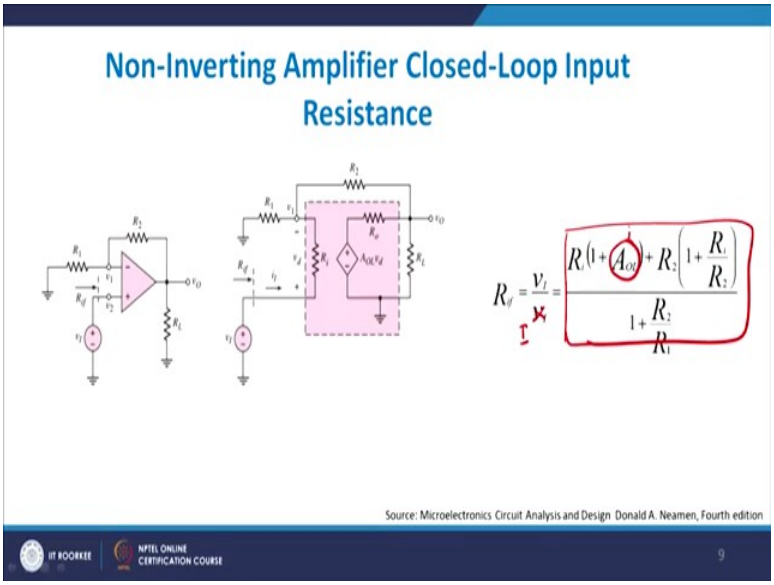

If I do a non-inverting exactly the same happens, non-inverting case R_{if} case comes out to be equal to this one right and this is sorry this is actually V_I by I_I, right, input current and this is the input resistance 1 plus A_{OL} plus R_2.

So as you can see if this goes to very high value right, your R_{if} also goes to a very high value right and this is true also if a open loop gain is very very high of an operational amplifier your input impedances will also be very high right and you can get this value here. So is it a R_1, R_2, R_L is exactly the same as the pervious case and we get this into consideration here with V_d is the voltage difference between R_1 and R_2 between this point and this point, right.

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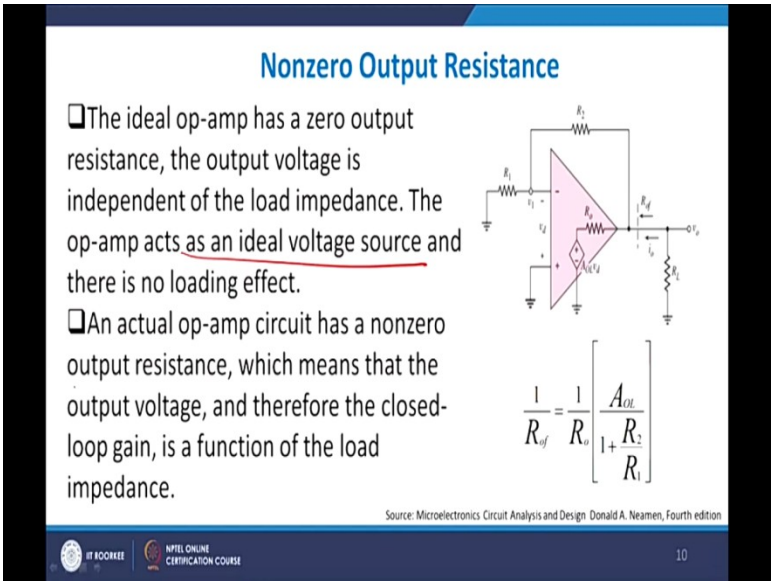

We come to the non-zero output resistance; typically the ideal op-amp has a zero output resistance. We have already seen that but and the output voltage therefore is independent of the resistances seen at the output load and that is therefore op-amp starts to act like an ideal, what is an ideal voltage source? Ideal voltage source is a source which gives you, wherein you can draw any large current but the voltage across the that source will always remain constant right and that was the ideal voltage source which means that there is no loading, in reality not true that the output the ideal op-amps will have some non zero in resistance in the output side.

As I discussed with you therefore the actual op-amp circuit will have a non-zero output resistance which means that that output voltage and therefore the closed loop gain is as function of the load impedance, right. Why? Because see if let us suppose, let us suppose that output voltage is independent of load impedances right, so whatever your load impedance is 10 kilo ohm, 5 kilo ohm, 100 ohm or 40 ohm or shortage, the voltage level at the particular point will remain fixed and so when your impedance levels are say 100 kilo ohm, you will be drawing a smaller current but if voltage remains fixed right.

So when you want to make your voltage independent of load impedances then you assume that op-amp is behaving like an ideal voltage source, in reality not true as I discussed with you and therefore your output voltage will start to become a function of your output impedance, right? And therefore when you output impedance changes, your voltage will also change.

It is given by this formula here1 by R_{of} to be equals to 1 by R_o, R_o is the, 1 by R_o is basically my output impedance under ideal conditions right, but with this you get A_{OL} coming into picture. So if you just make it, if you just do the reciprocal of this one I get R_{of} to be equals to R_o right and then you reciprocate this 1 plus R_2 by R_1 right, divide it by A_{OL}. As you can see make open-loop gain infinitely large and R_{of} goes to 0. So ideal output output voltage always be close to 0.

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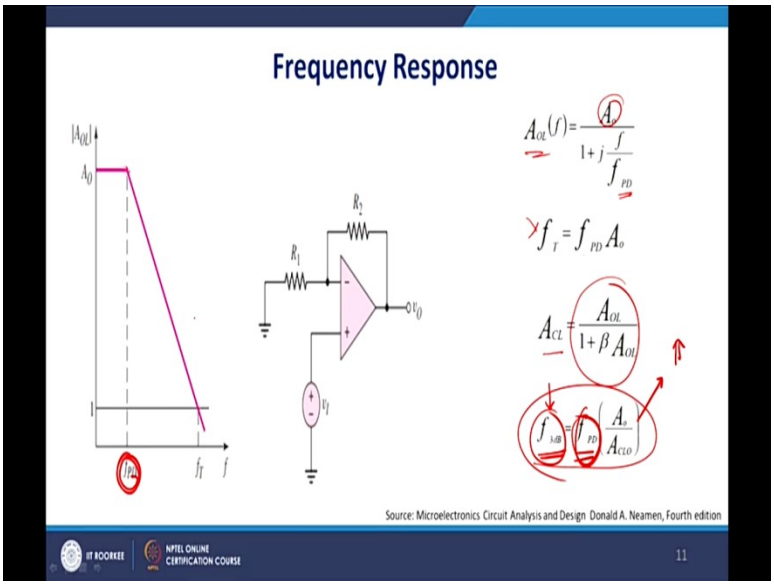

Look at the frequency response, as I discussed with you frequency response for any other cases will be just like a low-pass filter and A_{OL}, open loop gain is given as A_o upon 1 plus j by f_{PD}, PD is basically your 3 dB point, so f_T which is the unity gain frequency is given by f_{PD} into A_o and therefore the closed loop gain is given by A_{OL} upon 1 plus β times A_{OL}, right? And therefore you get f 3dB equals to f $_{Pd}$ into A_{OL} upon A_{CLO}, which means that 3 dB frequency depends upon your f_{PD} and also depends upon the ratio of your open loop gain on the closed loop gain, right.

So if you know, if this quantity is high which generally it is then your 3dB bandwidth is higher than f_{PD}, right? And that is what you get here f_{PD} is basically my 3dB, 3dB bandwidth and f $_{PD}$ is my, f_{PD} is this point where it starts to go down and this f_{3dB} is the bandwidth at which you have a 3dB gain here. So we will again come back to this frequency response later, all in a detailed manner. At this stage you can understand it is almost behave like an integrator and low-pass integrator.

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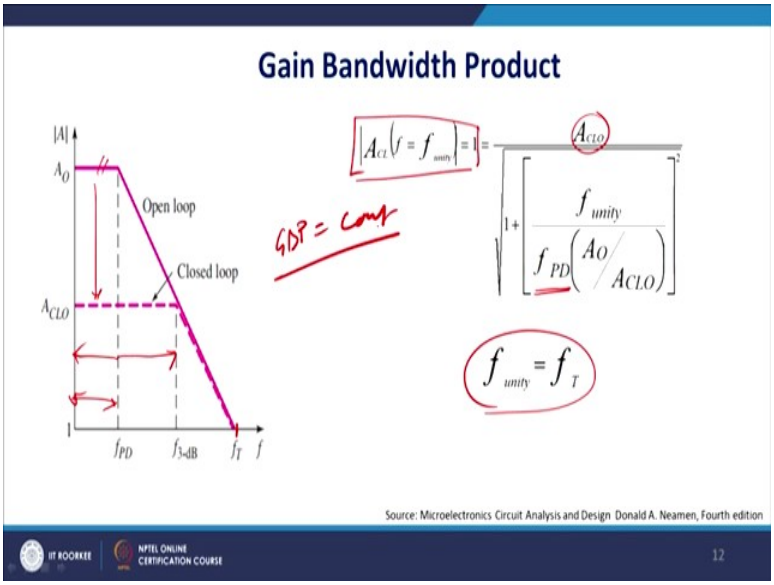

Now gain bandwidth product is given by closed loop gain if you look very carefully, unity f_T, f_T is unity gain bandwidth is given by CLO which means that the closed loop circuitry 1 plus f unity; f unity is f_T divided by f_{PD}, f_{PD} is basically my 3dB into A_{OL} by A_{CLO}. And therefore I get f_T equals to, so f unity is equals to f_T, provided I get A_0 by A_{CLO} very high, right.

So what happens is that when you open-loop your gain is higher, when your closed loop your gain falls down but your 3dB bandwidth increases so your initial 3dB was this much right and now your 3dB has improved by this much, so your 3dB bandwidth is an and that is the reason your GBP, Gain Bandwidth Product is always constant. So the first case without when you are in an open loop conditions, you automatically have your gain very very high, in the closed loop conditions your gains falls off drastically, right. Okay

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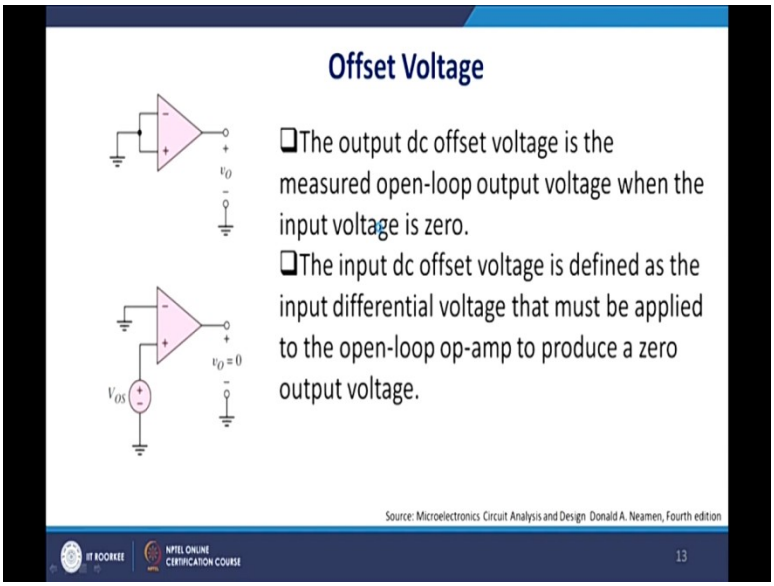

We come to another important issue of an operational amplifier and that is known as an Offset Voltage. Now ideally if you remember if I short the input of my operational amplifier, the inverting and the non-inverting input, then for this, then I will get 0 output available to me because V_2 minus V_1 is 0. In reality not true, there is some amount of DC voltage available to me in the output side. So I can see here the output DC offset voltage is measured open-loop output voltage when the input voltage is zero, right. The input DC offset voltage is defined as the input differential voltage that must be applied to the open-loop op-amp to produce a zero output voltage. You got the point?

So you see when you do not apply anything you get some voltage right? Now if we apply a voltage in the reverse direction, then this high value will go down to zero. So this amount of voltage is, input side voltage is defined as my input differential offset voltage right or input offset voltage. I can have an output offset voltage also I can have an input offset voltage. What is an input offset voltage, at the input side the amount of voltage you need to give differential between two voltage sources so that the output goes to zero is my defined as my input differential voltage.

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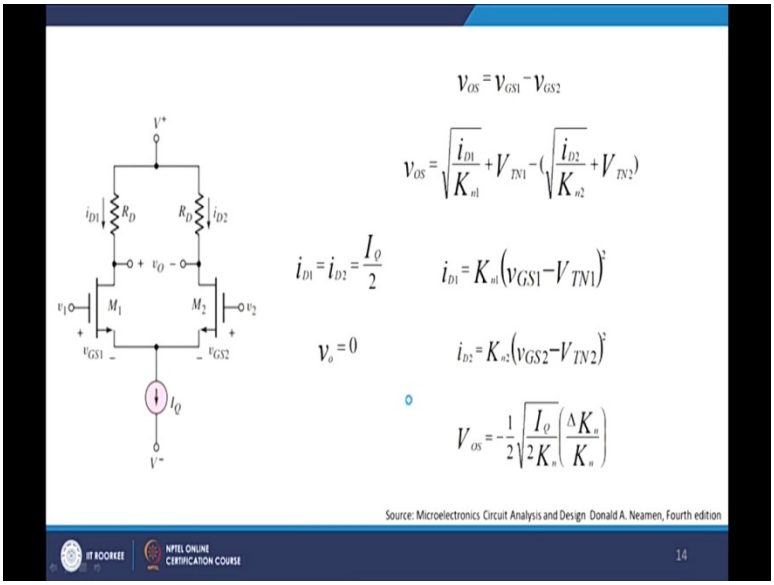

I will not go into the details of the derivations here but typically if you look very carefully assuming that, I have a differential pair here right and it is driven by this, by this ideal current source here. And so this is the V_{GS1} is the drive voltage, V_{GS2} and I am trying to do the voltage difference between V_0 and V_1. So offset voltage will be given as V_{GS1} minus V_{GS2} right, remember because these are the two inputs I am giving to the operational amplifier. Now I am assuming that these voltages are not equal, so I am trying to find out the difference between the two voltages, right.

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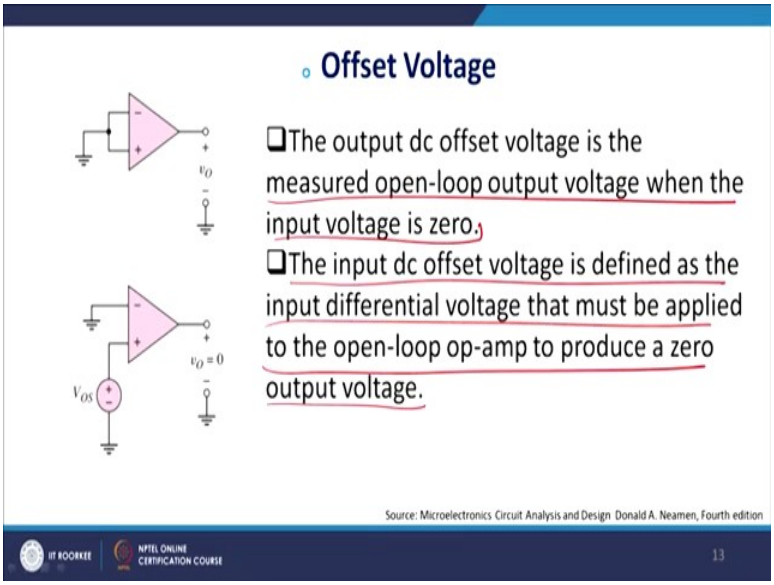

So in reality if you look very carefully, in the previous slide if you, if you go back to the previous slide see this is the V_{OS} I am giving here and I have grounded this I am giving V_{OS}, so that this goes to 0.

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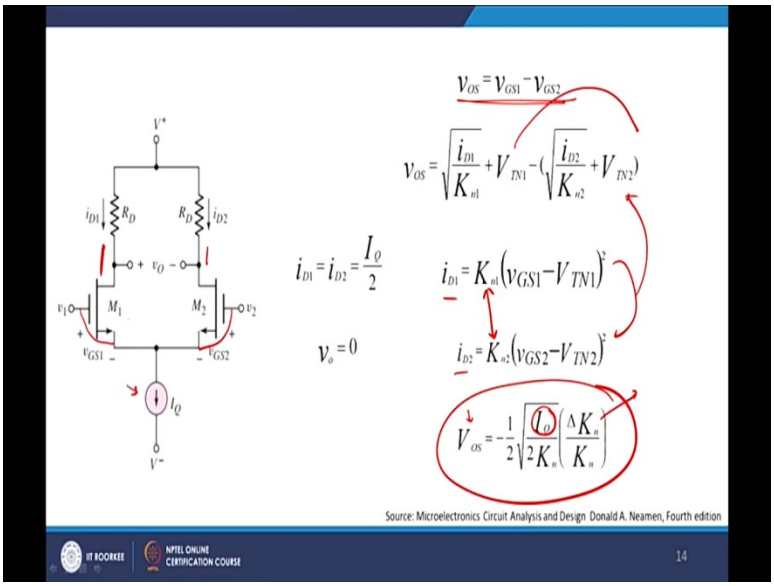

So with this concept I have applied V_{OS} as V_{GS1} minus V_{GS2} right. This is from assuming that there is saturation I get root of I_{D1} upon K_{n1} where K_{n1} is μ_{n1} C_{ox} (W/L) by l plus V_{TN1} threshold voltage of N-MOS minus this whole quantity where I_{D1} is given by this I_{D2} is given by this. I_{D1} is the current flowing through this arm and I_{D2} is the current flowing through these two arm. If you

put all these values back into this equation, do a small solution assuming that V_{TN1} equals to V_{TN2}, so they cancel out. I get this output voltage the value here, right, where, just let me see, yes.

So I will get this output voltage where I_Q is the sum of the two currents which you see and delta K_n is basically the difference in the value of your, these two values, right. Difference of these two values and K_n is basically the one of the, K_n is the process transconductance parameter of the differential pair. As you can see here higher the current more will be offset in a negative sense right, because it is the inverting terminal which I am giving to you. Okay.

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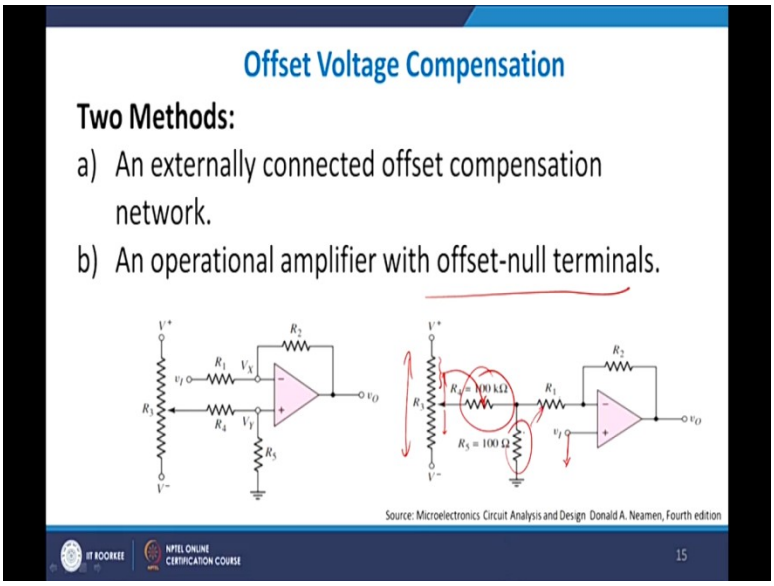

We come to the offset compensation voltage compensation, so there are two methods by which you can compensate the offset voltages and these two compensations are externally compensation, externally connected of set compensation network and with the null offset terminals. So we would not go into the details but I will give you an idea how it works out in a very simple manner. So you see I have V_i here which I am giving. I also have a 100 ohm R_1 and 100 kilo ohm here.

I have a potential divider at R_3, so If I move this up or down right, some amount of resistance will be in series 200 kilo ohm and that will be in parallel to 100 ohm here and this will be feeding the voltage to R_1, you getting my point? So by simply choosing the potential divider network up or down I can actually make the resistance value in a potential divider network change right and make it exactly equal to the offset voltage.

So what I do, what I initially experimentally how how I do it, I go on shifting this potential divider network up or down and check out that when V_0 equals to 0. So when V_0 is equals to 0, I stop and that is basically my input offset voltage, right. So this is one of the methodologies people adopt across the current.

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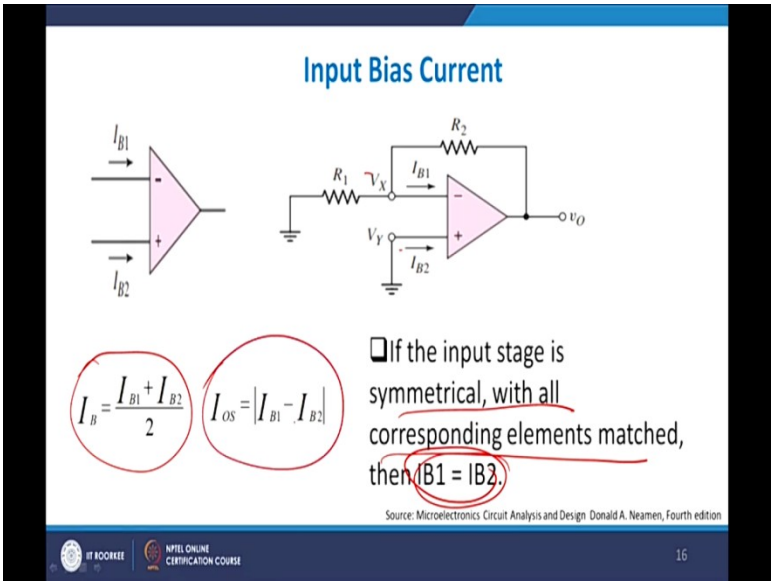

Then you also have an Input Bias Current, well this is very simple. They will be generally symmetrical if everything is matched for the top and bottom. If the input stage is symmetrical with all the corresponding elements match, I_{B1} will has to be equal to I_{B2}. So I define I_B equals to I_{B1} plus I_{B2} the average current and offset current is defined as difference between I_{B1} and I_{B2}. In reality, I_{B1} and I_{B2} must be equal but they are not and therefore there will be difference. Okay.

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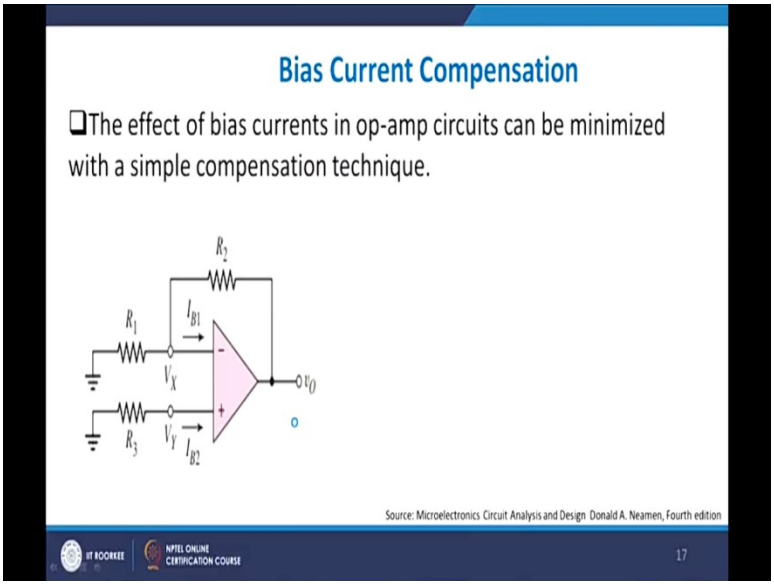

I come to Bias Current Compensation, so I was doing voltage compensation there. Now I do a bias compensation and this bias compensation is given by this manner by that which we have got V_X and V_Y here and simply by choosing appropriate value of R_3, I can choose I_{B1} equal to I_{B2}, right. I will not go into further details of this one, because this is slightly higher than what you are supposed to know at this stage and therefore you need not worry about from where I am getting this bias compensation.

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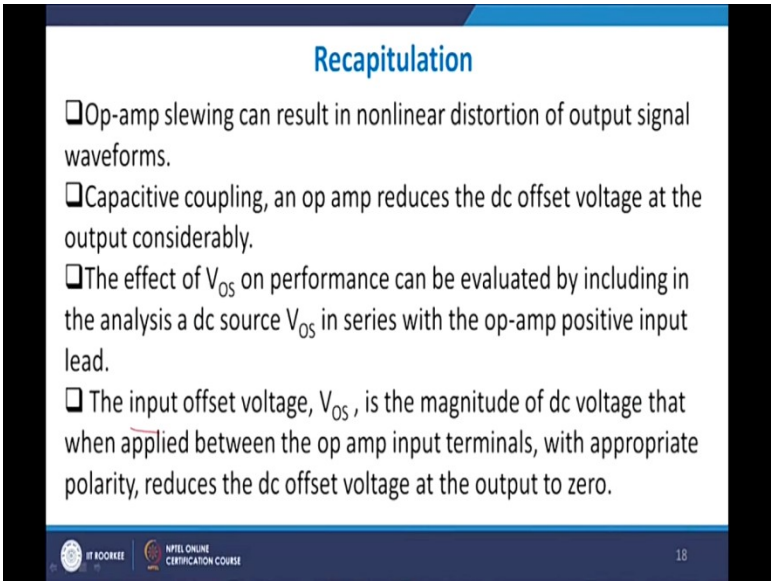

So let me recapitulate what we did, we were actually looking into an op-amp slewing action. What is the meaning of slew right and what is slew rate, slew rate limited operation? What is a DC offset voltage right and how do you define DC offset voltages? What is the meaning of saturation, operational amplifier saturation? What is the meaning of input offset voltage V_{OS}?

And how can we determine the input offset voltage, similarly what is the input offset current and how can you remove it. So this we have learned in this module and this takes care of approximately our whole understanding of the analog part of the syllabus. So from next turn onwards, we will start with the combinational logic which is a digital part, right? And for the next ten five to six hours of our lecture which is left we will be actually doing a lot of differential a lot of digital logic design.

So this is where we stop our mixed signal or analog block out of the circuits, so if you look at the whole structure of the course it is first devices which is the first few weeks, one or two weeks. Then subsequently from three to lecture week number seven it is primarily a analog flow and then we have a digital flow at the last places. So next time onwards we will start the digital flow. Thank you very much.