Microelectronics: Devices to Circuits
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Lecture 44: Frequency Response of the Differential Amplifier

Hello everybody and welcome to the next edition of NPTEL Online certification course on Microelectronics Devices to Circuits. Today we will be taking up frequency response of the differential amplifiers. We have already seen in our previous discussions and modules that a differential amplifier gives you a relatively larger gain as compared to a single stage amplifier. The second advantage is that it is a very good rejecter of common signals to both the inputs of the differential amplifier which means that any noise will be heavily rejected.

And therefore, signal to noise ratios for differential amplifiers are relatively very high as compared to single stage amplifier. However, the price we pay for it is it has got a much larger power dissipation because now you have to drive 2 transistors in 2 loads. Not only that there is also a problem of mismatch between the 2 arms of the differential pair, right? So, if this is small difference in terms of let us say load resistance or transconductance that reflects your common mode gain also.

So, in reality you common made common mode gain should be close to 0, ideally it should be 0 which means that any common mode signal will not be at all amplified. And all differential mode signals would be highly amplified. So, A_{DM} upon A_{CM} should be very large quantity but due to these problem areas your A_{CM} also becomes large and therefore, CMRR which is adm by A_{CM} also does not go to a very high value.

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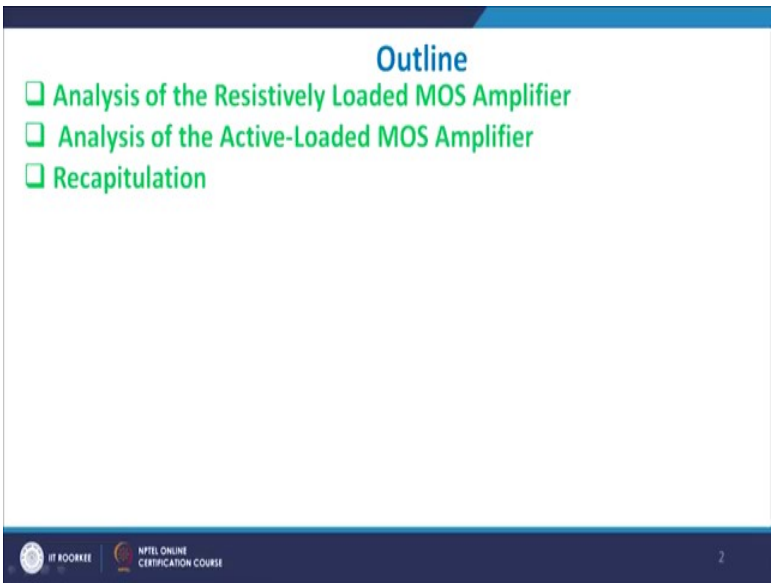

So, we will look into this frequency response of a differential amplifier and the outline of this talk will be analysis of resistively loaded MOS amplifiers. We will take up that first of all and then actively loaded MOS amplifier we will take. So, one is the resistive loading which basically means that you are loading at the pull up stages basically by r_d. This was a resistance and your actively loaded MOS amplifier will be that you do have a current mirror based MOS device or loaded device and, of course, then we will recapitulate, right? And then we will go for cascoded stage amplifier designed in our subsequent talk.

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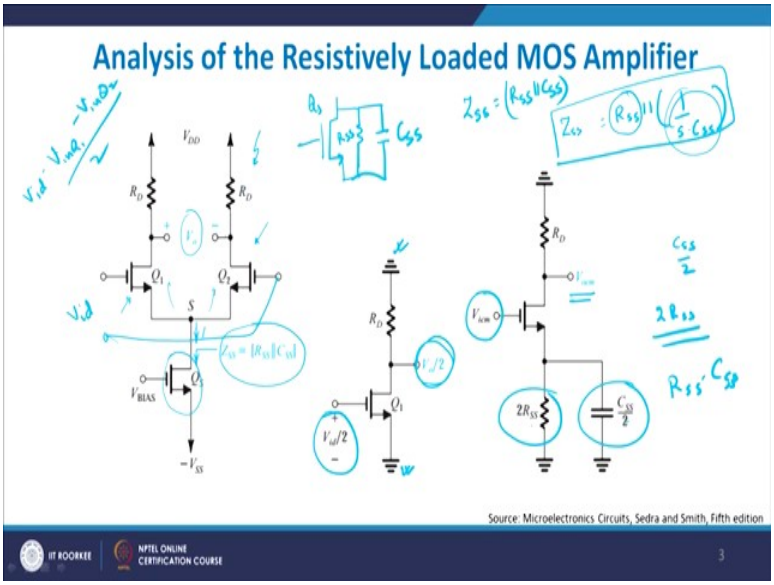

Let me show you how a resistively loaded MOS amplifier looks like. You see the left hand side if you look here is basically you have got 2 input devices q1 and q2, right? And these are all active devices and these are basically MOS devices. You also have a qs which is basically the current source which is giving current to both the arms q1 and q2 here, right? Then we have got RD the resistance here and the output is taken between the 2 nodes here which is referred to as v not. As you can see therefore, that there effective value of impedance seen from node S towards S from the ground is basically R_{SS} is parallel to C_{SS}.

What is R_{SS}? If you look very carefully R_{SS} is nothing but if you if you plot qs here, right; this is qs. The R_{SS} is nothing but this, right? And C_{SS} is nothing but the capacitances in parallel to it. So, this is your C_{SS} and this is your R_{SS}, right? And the parallel combination of that gives you ZSS are also referred to as the impedance seen from the from the from the source end of the input transistor. Now, if you remember C_{SS} can also be written as 1 over S of C_{SS}, right; j omega C_{SS}. This is Z_{SS}, right?

So, whenever we talk about so basically it is a parallel combination and therefore, overall resistance and impedance will be less than the least or will be least of course. Now, what happens is that very high frequencies of operation, relatively high frequencies of operation. This 1 by S of C_{SS} goes low and therefore, it is capacitively dominated and relatively low values of

capacitances or frequencies R_{SS} which is the DC resistance offered by this transistor qs comes into picture, right?

But, nonetheless you will always have a Z_{SS} value which is basically a parallel combination of both comes into picture. Now, to do a single stage, so to understand this we have already seen our previous discussion that we all short our dc biases so V_{DD} is shorted and my ground is also grounded here. And we apply a signal which is V_{ID} by 2, right; half the difference signal between the2. So, remember basically what w do is that if this my input here then I apply my V_{ID}. V_{ID} is nothing but v in q1 minus V_{in} q2.

So, V_{ID} by 2 will be this much. So, this much amount of voltage is applied here and we try to get the value of V_{02}, V_0 by 2 here the output voltage here; which is nothing but the voltage visible at this particular point. Now, as I discussed with you earlier that q1 and q2 need to be initially biased by a dc supply which is basically a common mode supply which will result in these two q1 and q2 working in the saturation region and therefore, this is the V_{icm} which is the common mode signal.

And this is my V_{OCM} which is coming out of it. If you see very carefully the capacitance is half because, the capacitance is half the resistance is double because 2 R_{SS} comes into picture because there are if you look very carefully if this is single device it can be broken into two compound devices and whose capacitances will be in parallel will be in series. And therefore, I get C_{SS} by 2 as the effective capacitance.

However, since they are in they are in series to each other we get 2 R_{SS} as the overall resistance seen from the particular arm. So, if you multiply 2 into see if you see the time constant which you get as R_{SS} into C_{SS} because if you multiply this 2 gets cancelled off and you get R_{SS} into C_{SS}, right? So, this is the typical structure of any MOS device which you see.

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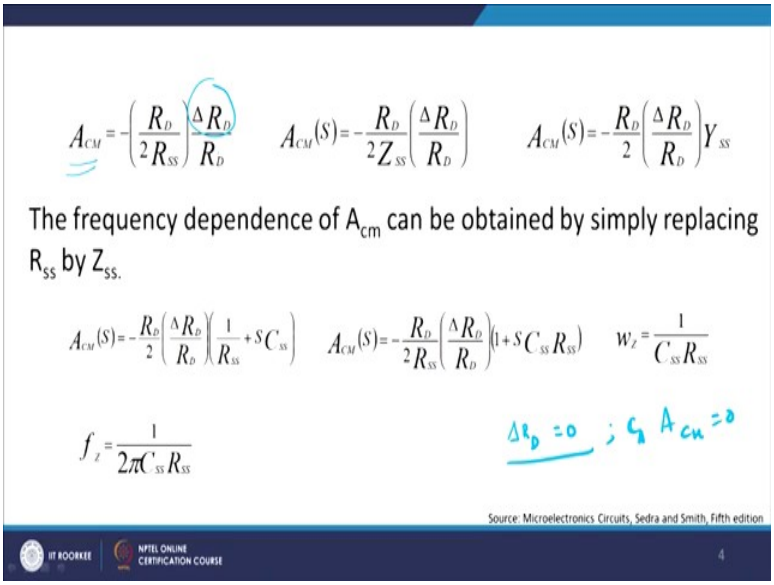

Now, let us suppose you have mismatch of the drain resistance, right? If there is a mismatch of drain resistance whose value is equal to del R_D then I get A_{CM} the common mode signal equals to R_D upon 2 R_{SS} into del R_D by r_d. I am not deriving it here but this is what the value is which you will get.

The reason ideally if you look very carefully if you have no mismatches then this del R_D will be equals to 0 and therefore, my A_{CM} shall be equals to, A_{CM} should be equals to 0, right? But if there is some mismatch between the 2 I get this into consideration and so best methodology is you can see is to improve your A_{CM} almost to 0 value a low value is to keep your R_{SS} also very high which effectively means that.

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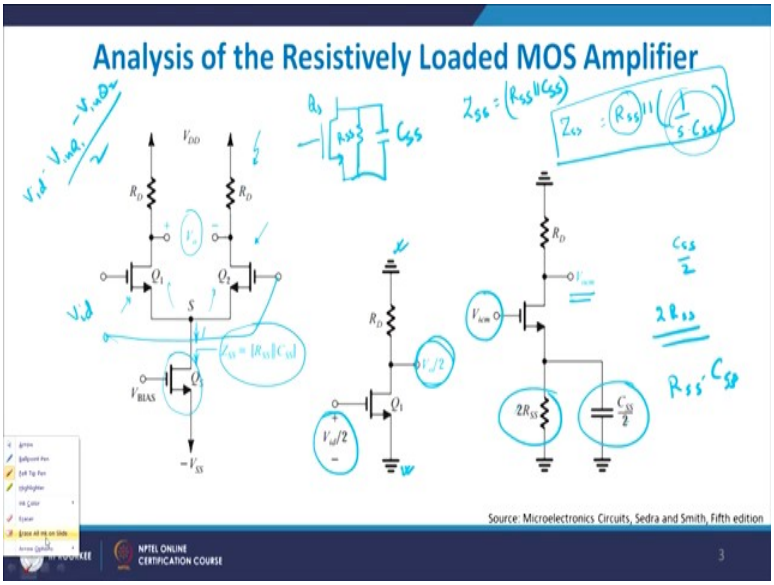

If you go back to this slide again and then let me rub all these things, then this transistor qs has actually to behave like an ideal current source. If it behaves like an ideal current source then resistance offered output impedance offered by it is relatively very high.

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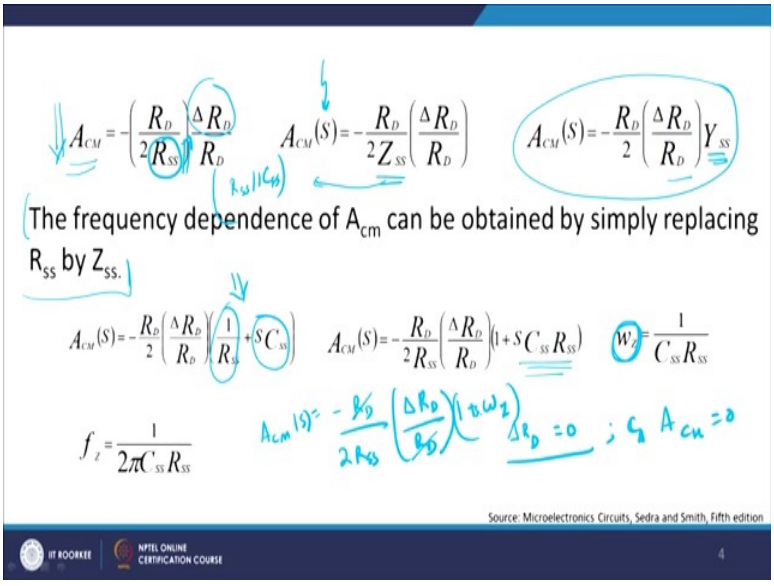

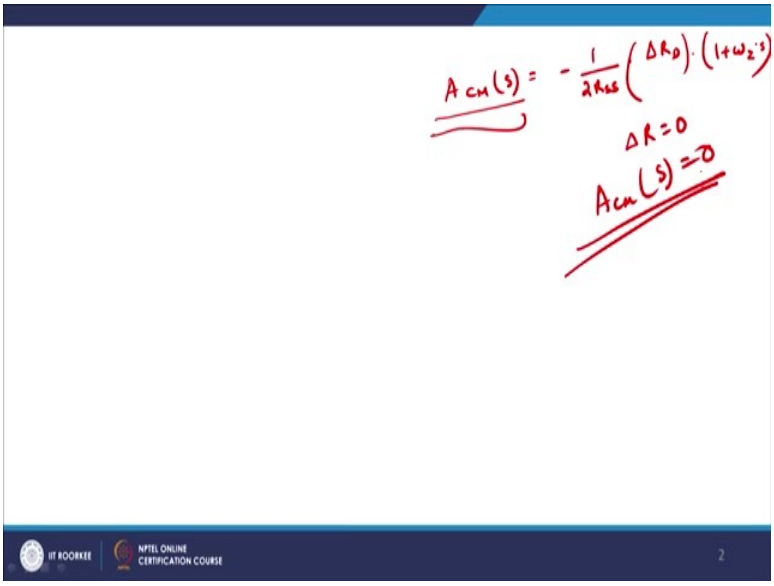

So, RSS is relatively very high and as a result what you will see is A_{CM} is very low in that case. So, when I go in frequency domain I replace R_{SS} by Z_{SS} and Z_{SS} is given by RSS parallel to C_{SS}, right? And we get R_D upon this thing into consideration. Now, 1 upon Z_{SS} is nothing but Y_{SS} and therefore, I get A_{CM} to be equals to minus R_D by 2 into del R_D by R_D into Y_{SS}, right?

As I discussed with you therefore the frequency dependence of ACM can be obtained by simply replacing RSS by ZSS. That is what we have done strictly in this case. Therefore, in S domain I can just simply simply write down this this quantity R_D basically it is R_D by R_{SS} R_D by 2 into del R_D by R_D into Y_{SS}. So, Y_{SS} I can simply write down as equals to 1 by R_{SS} plus S of Scc, right? Because Y is nothing but 1 by Z so, if you remember Z is equal to v by I I by v, right?

So, I by v is nothing but 1 by r 1 by r. so, this is what you get from here. And since they are parallel to each other we simply add those 2 together. Similarly, if I do a small manipulation here it will be S times RSS here, right? And this RSS will come in the output side and I will get R_D by 2 RSS into del R_D by R_D into R_{SS}. Now, you refer to it as omega Z omega Z and therefore, I can write down A_{CM} in S domain to be equals to minus R_D by 2 R_{SS}, right? Into del R_D by R_D into 1 plus swz, right?

So, now you see that R_D also gets cancelled out and you are left with the fact that your your A_{CM} of S is equals to minus 1 by 1 by 2 RSS right multiplied by del R_D del R_D into 1 plus omega into omega Z into S. so, this is your common mode differential signal which you see. So, in this case

as you can see del R_D equals to 0 I get A_{CMs} equals also equals to 0, right? And that is quite an interesting idea which you see. This is basically omega Z is basically my 1 by C_{SS} or f_z is equals to because omega Z will be 1 by 2 pi r. So, 1 by 2 pi comes here and I get the frequency to be 1 by 2 pi C_{SS} R_{SS}, right? Right!

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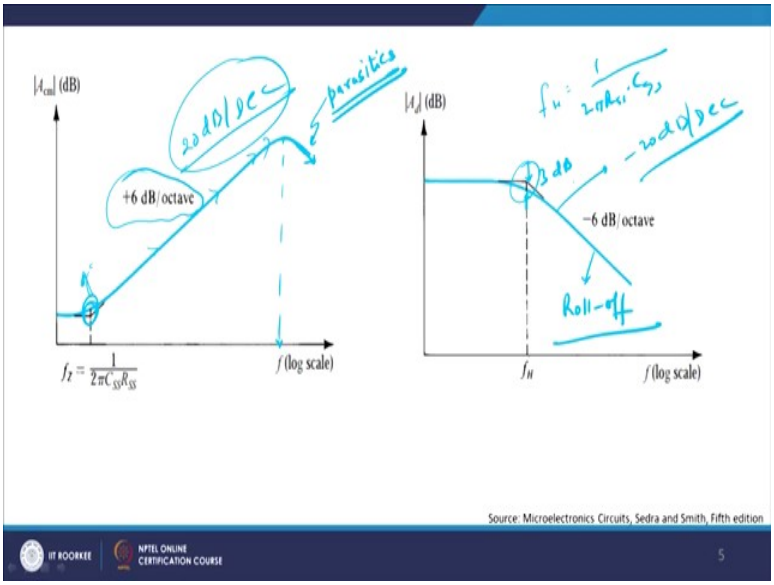

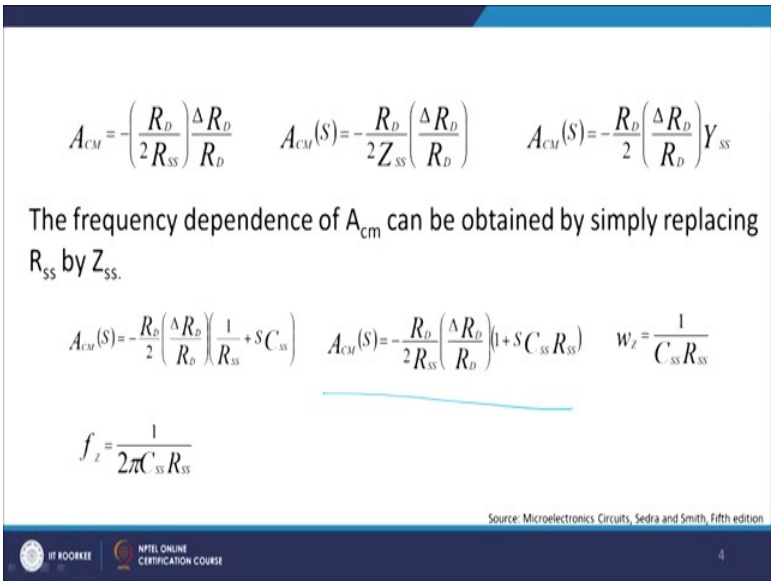

Now, with this knowledge let me plot for you the differential gain versus frequency here. And as you can see at very-very low frequencies at typically very low frequencies if you if you just see the sorry, if you look at the point then the gain is differential gain is almost constant independent

of frequency. But as the frequency goes on increasing somewhere near f_h is nothing but approximately 1 by 2 pi R_{SS} into C_{SS}.

Somewhere, at this point you get a 3 db drop here. This is minus 3 db gain or a drop here. And after this you get minus 20 db per decade drop in terms of differential voltage gain. So, this is this is defined as a roll of which you see. This is known as a roll of, right? So, I have got a roll of available at this particular point. This is your low frequency gain behaving like a low pass amplifier low pass filter actually where your low frequency gain is relatively high and at high frequency the gain starts to fall off.

Whereas if you look at the common mode signal, right; and go back to the previous slide then then you will see that the common mode signal is given by this formula. The gain at least is given by this formula, right; in S domain. So, when S equals to 0 or it is very-very small, your value is very small, right? And that is what you get here. So, what do you get when S is very small this is also very small. Beyond a particular point given by 1 by 2 pi C_{SS} R_{SS} as the S value goes on increasing, A_{CM} value also goes on increasing, right?

And the increase is basically 20 db per decade or plus 6 db per decade octave increase. We will stick to this single formula 20 db per decade enhancement is there. It has been seen that beyond a particular point your actually the A_{CM} value the common mode gain starts to fall down or again there is a roll of point which you see beyond which the frequency it falls off. And this is primarily because of parasitics. So, this is primarily because of parasitics which you get which makes your output capacitance getting loaded.

So, apart from C_{SS} and R_{SS} you will also have an output capacitance which will be in series to overall picture. And as a result overall capacitance will increase and your gain will start to fall down beyond a particular limit. But this is sort of 3 db drop here this is 3 db gain here and the 3 db drop here for the differential amplifier design.

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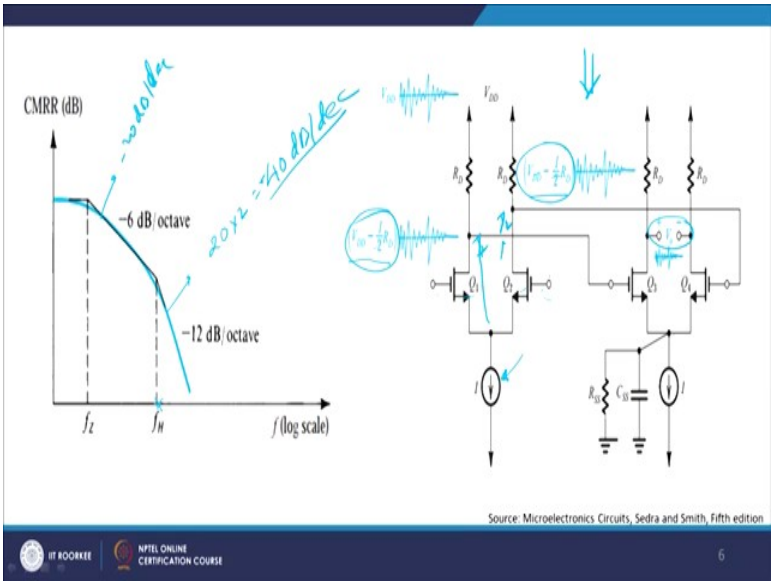

So, if you look at CMRR as I discussed with you we define f_h be equals to position where you will have 1 by 2 pi R_{SS} C_{SS} beyond which you will get actually a 20 into 2 which is basically 40 db per decade drop, right with a negative sign. So, I will get initially 0 and then I will get a minus 20 db per decade, right? And then I get 40 db per decade drop here and this roll off is very high at higher frequency.

Now, if you look at this slide this slide last part here q1 and q2 are basically the transistors which you have given and I have a current source which is the tail current source you give. Depending upon the input value of voltage I get V_{DD} by 2 into R_D which means that half the current flows here and half the current flows here I get V_{DD} minus 2 R_D as the output voltage here and V_{DD} minus I by 2 R_D as output voltage here.

The same voltage are fed into q3 and q4 the second stage of the differential amplifier and as a result you will get a v out value depending on these 2 values here, right? So, as the current goes on increasing I goes on increasing this quantity goes on decreasing this goes on decreasing right? So, how does current goes on increasing by simply make both these transistors switch on at higher values of threshold voltages. And more current will be drawn from I. Its maximum value is I by 2.

You cannot have currents greater than I by 2 but it will be if current is less than I by 2 then you will automatically have voltages here slightly larger, right? And, therefore, forcing q3 and q4 in saturation. As a result we will get an output which is depending on the value of q3 and q4 here which state the q3 and q4 devices are run. Similarly, I have just blocked the current source through R_{SS} and C_{SS} in this case.

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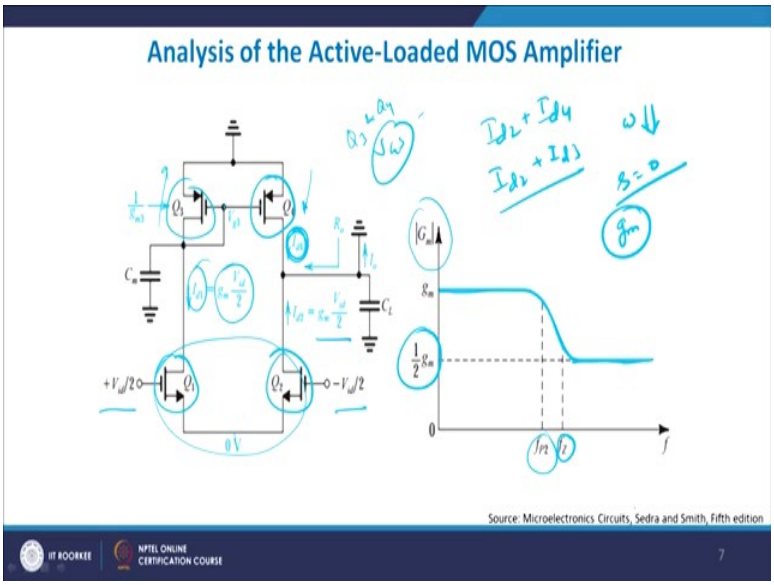

So, now what I do is I replace so till now what we were doing is we were concentrating on the fact that you will have a resistance in the pull up transistor which is rd. But now what I do is I replace RD by q3 and q4 which is basically pMOS loaded actively loaded pMOS and which it is basically current mirror source and the gate. Sorry the drain and the gate of q3 are shorted with respect to each other. Once you short it, it starts to behave like a resistive element and therefore, the current flowing through q3 is replicated in q4, right? Because this gate voltage here and the gate voltage at this particular point is exactly the same. So, gate to source voltage of both the transistors q3 and q4 VGS is exactly the same, right?

If I assume that q3 and q4 are the same transistors with same threshold voltage the current flowing through m which is mu nc oxide w by l V_{GS} minus V_{TH} whole square will also be same and as a result same current will be flowing through q4, right? So, I will have obviously a current flowing through q3 and there will be a same current flowing through q4. So, if I assume that

there is no change here but the current source is ideal current source. So, I have removed it because its output impedance infinitely high.

I have given V_{ID} by 2 V_{ID} by 2 here. Once you have given V_{ID} by 2 I get a current which is basically gm times v_g. So, g_m into V_{ID} by 2 is 1 which you see. This id1 will come here and i_{d2} will be flowing which is g_{m2} into V_{ID} by 2. I will get id4 which is primarily the current flowing through q4 because of q3 and current mirroring action here. And therefore, the total current will be equals to i_{d2} plus i_{d4}. Now, i_{d4} is also equals to i_{d3}. So, i_{d2} plus i_{d3} I can also write down as the total current flowing through the device, right?

And that much amount of is across the load capacitance, right? So, if you plot capital g_m which is basically the transconductance of q1 and q2 taken together then you will see that till a particular frequency the trans conductance is almost independent of frequency. It is almost a straight line beyond which you will see a certain drop here and then it again remains constant approximately given by g_m.

So, I will see initially first gm and then it goes to half g_m in essence, and the reason can be found out from this picture only because very low frequencies of operation when the frequency is relatively low and you do not have any other frequency issues at this particular point, then what happens is that when frequency is relatively low omega is low your S is also approximately equals to 0 in dc case.

Then this capacitance transistors q1 and q2 work in pure active region, right? And they there biased points do not move about. There biased points are fixed. So, they are overall trans conductance is nothing but g_m. Once, I increase my frequency and I goes to a value of f_z 1 by 2 pi R_{SS} into C_{SS} then at a particular point the gm starts to drop down, the gain starts to drop down. And the reason being now because you have larger parasitic into picture and the overall capacitance becomes half g_m and therefore gain also drops down at a particular point. That is the reason a differential amplifier your gain at a high frequency starts to drop down, right?

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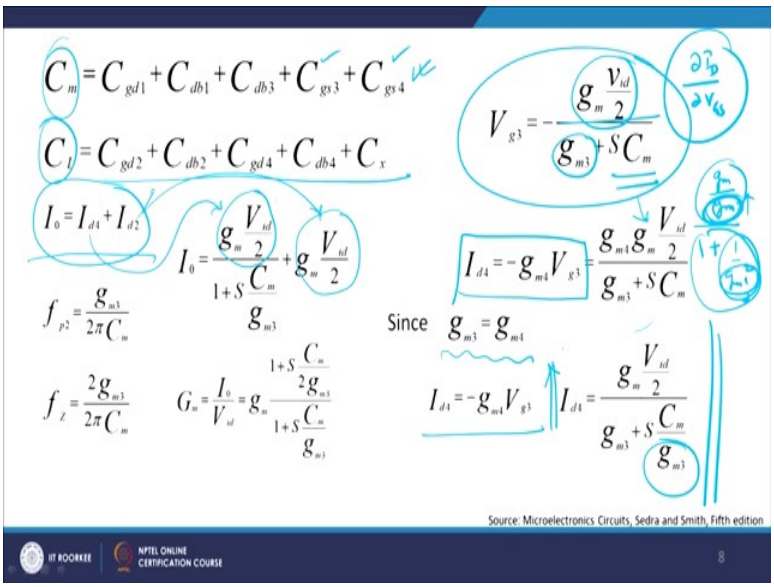

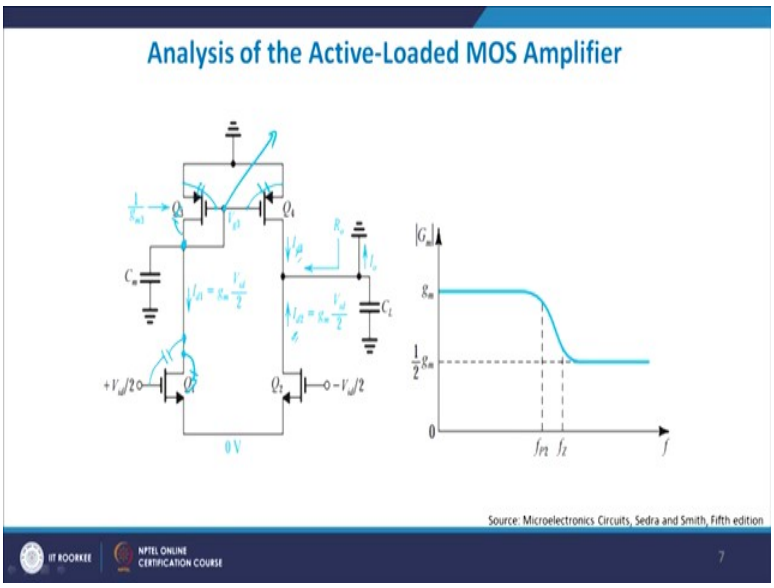

Let me show to you therefore id. So, total current which is flowing through the device is nothing but i_{d4} plus i_{d2}. What is i_{d4} and i_{d2}? I_{d4} and i_{d2} is nothing but this is i_{d4} this is i_{d2} and this is i_{d4}. So, if you look at i_{d4}, this is the total current which flows through a device. This can also be written as gm into V_{ID} by 2, right because that is the current which is flowing through the arm.

This divided by 1 plus S c by g_{m3} sc by g_{m3} because capacitance by transconductance will give you a value which is fundamentally resistance. As a result what you will get is voltage by

resistance will give you a current flow here. And that is must be equal to $g_m i_d$ by 2 which is which is coming from i_{d2}. So, this is your i_{d4} and this is your i_{d2}, right? And you simply add those 2 together in in reality.

And so what I get from here is I get v_{g3} right? V_{g3} is the gate voltage of 3 transistors is equal to gate voltage of number 3 transistors is this is if you remember del I is, del id del VGS right? So, that is what you get. Del id is nothing but gm times V_{ID} by 2, right? Because half of the half of the voltages applied here divided by you get gm3 transconductance of the device plus S times cm which is basically the total capacitance seen by at node 3 which will include of drain to drain to bulk drain to bulk of 3 gate to source of 3 and gate to source of 4.

So, gate to source of 4, gate to source of 3 and gate to drain of 1. I hope you understand this point, right? As you can see here this is gate to source of 4, right? It is gate to so I have a capacitance here I have a capacitance here, right? You also have gate to source of 3, 4 gate to drain of 1. Gate to drain of 1 basically means that gate to drain of 1. So, this one, right because this is connected to this particular point. So, this particular point is connected to this point. So, this point this point and this point are in parallel to each other.

And that is the reason you add it, right? And then you have got cdb1 and c_{db3}. What is cdb1? Drain to bulk of 1, drain to bulk of 1, right? And then drain to bulk of 3. Now, as you can see here all connected through this node, right? So, this node is a parallel node which is to all of them. So, you just have to simply add those capacitances and what do you get is basically my cm. similarly, I get cl to be equals to this whole quantity here, right?

And you need to simply place these capacitances here to get the value total value. So, I get i_{d4} to be equals to g_{m4} into V_{g3}. Now, why V_{g3}? Because V_{g3} is equals to V_{g4} so, simply you have to multiply the trans conductance of 4 th transistor multiplied by V_{g3} and you get this. So, I can write down gm4 into V_{g3} can be just this 1 can be replaced here and I get this into consideration. As you mean that g_{m3} is equal to gm4 because that is obviously because same w by l ratios same voltages which you see.

I get i_{d4} equals to g_{m4} into V_{g3} which is equals to g_m V_{ID} by 2 g_m V_{ID} by 2 divided by g_{m3} plus S of gm by g_{m3}. So, I get g_{m3} into consideration here as i_{d4}, right? So, I get i_{d4} to be this value. So, as you can see here as you make your g_{m3} if you if you divide by g_{m3} in the numerator and

denominator what you get is basically g_m upon g_{m3} here, right, divided by 1 plus if you divide it again by 1 by g_{m3} square 3 square. So, if you make your g_m go on increasing this quantity will increase and therefore this quantity will decrease.

This will also increase and this will decrease and therefore overall decrease will be there. And therefore, this i_{d4} will go on increasing as g_{m3} goes on increasing, right? And that is what we have seen also. The g_{m3} goes on increasing I would expect to see more and more of drain current flowing through the device structure.

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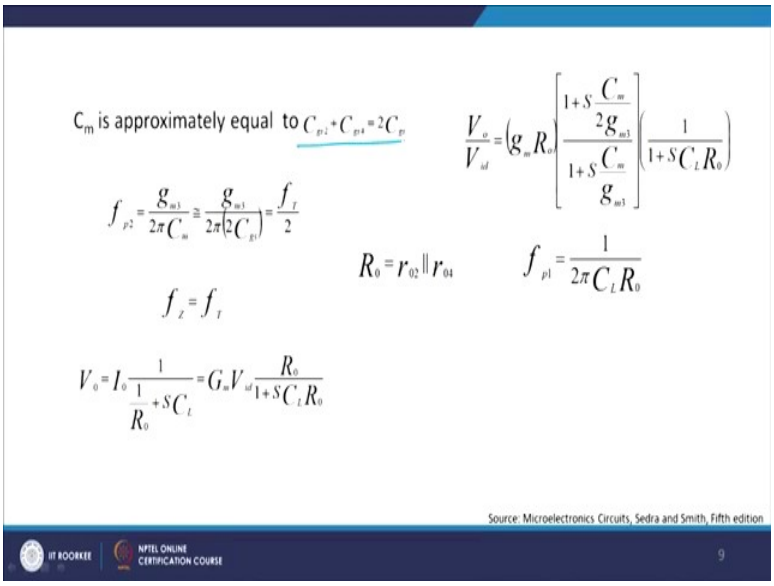

Therefore, as I discussed with you that cm will be approximately equals to the C_{GS2} and gate to source 4. So, 2 and 4 would be added, right? Let me show you why.

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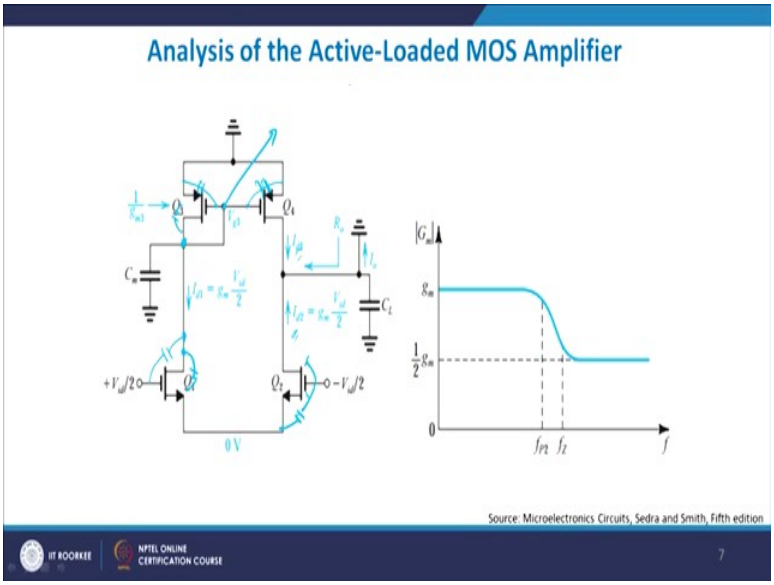

2 and 4 is basically C_{GS2} and C_{GS4}. C_{gs2} is gate to source of gate to source of 2 plus gate to source of 4, $C_{GS\,4}$. These 2 will be again parallel.

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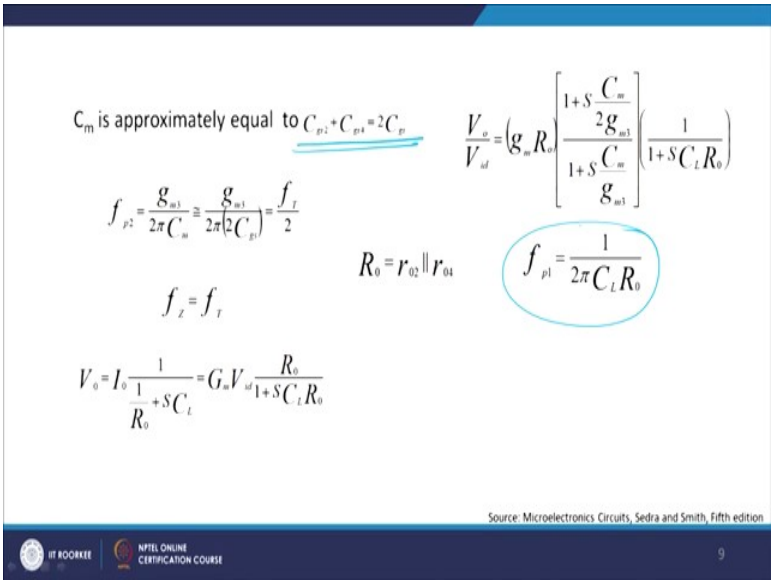

They will almost be equal to each other and as a result I will get C_{GS2} equal to 2 C_{GS}. If you solve again the whole transistor I get finally the value of pole first 4 frequencies 1 by 2 pi C_L times r_0

and that is effective value of frequency which is visible to you as far as finding out the values is available.

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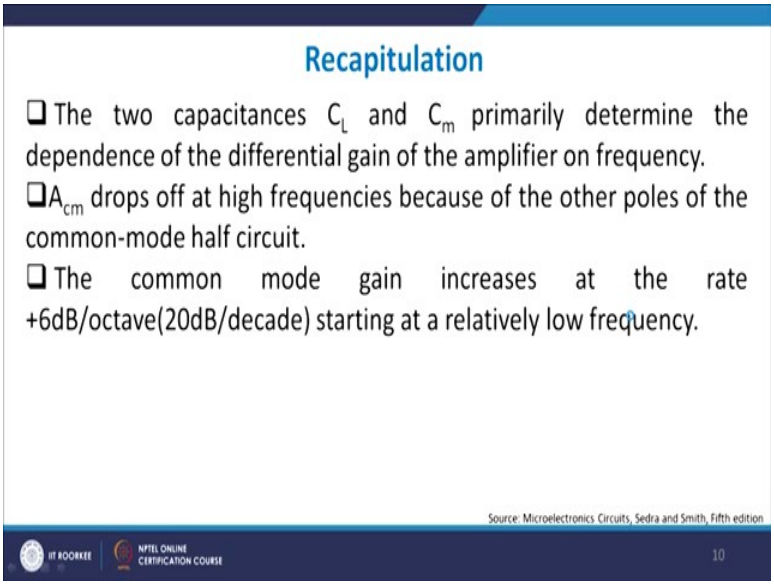

So, therefore, let me recapitulate what we have learnt till now for the for the high frequency domain analysis of this structure. The 2 capacitances are cl and cm. What is C_L? C_L and cm are basically the sum of the gate to source and the drain to bulk capacitances of all the 4 transistors which determine the cut off frequency of the differential amplifier, right? So, if you make them high, of course, your bandwidths will be limited and your cut off frequencies will be reduced. A_{CM} very-very important point drops off at a very high it increases at as the frequency increases but then at very high frequencies it starts to drop down, right?

Because there are other issues apart from that you have large amount of parasitic capacitances as well as due to formation of poles for the for the for the common mode half circuit here. The common mode gain increases at the rate of approximately 20 db per decades starting at relatively low frequencies. This we have already seen. The differential gain the differential amplifier gain starts to fall beyond the cut off frequency by approximately 20 db per decade whereas the CMRR, sorry A_V, A_{CM} actually is very low at low values of frequencies.

As the frequency increases the common mode gain increases but beyond a particular frequency the gain again starts to fall down and that makes my life difficult as far as this is concerned or

this idea is concerned. Okay! So, that takes care of our understanding of the basic concepts which you see here or the basic idea which you see here.

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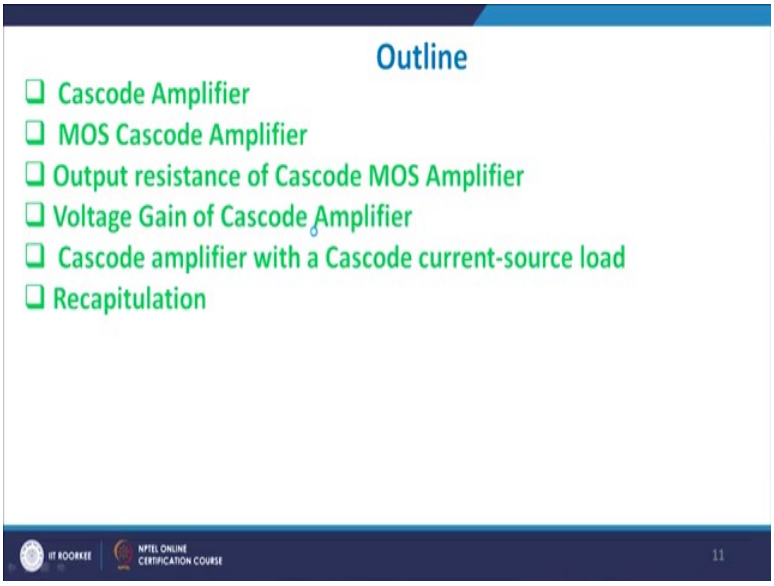

Let me now come to the last part of our amplifier design portion or the major portion of the amplifier and we start with first of all cascode and we take up MOS, cascode amplifier and cascode amplifier with cascode current source, right? So, we will be doing that.

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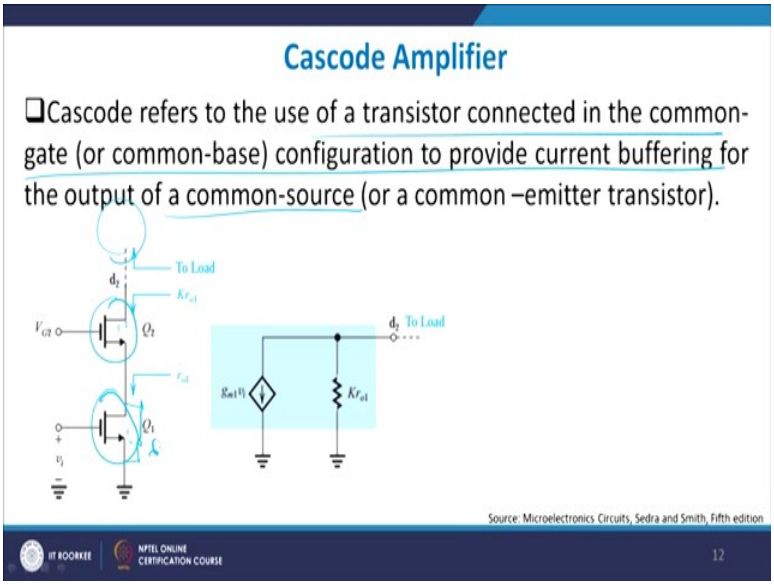

So cascoded amplifier is refers to the transistor in which a common gate is connected to a to a common source. So, common gate is connected to common source. So, you see this 1 is cascoded. This is my common source, right? And q2 is cascoded with respect to q1, right? And if you look very carefully this is so you have a load here and you are driving V_{g2} and we are giving an input voltage here and you are looking at the output somewhere here at this particular point.

And therefore, I can replace these transistors q1 by g_{m1} V_{i1} where V_{i1} is the input voltage. It is behaving like a current source. Parallel to this you will have a resistances which is effectively the resistances at this 1. So, this is r_{01} which you see, right? And this is the cascode amplifier general design which you see.

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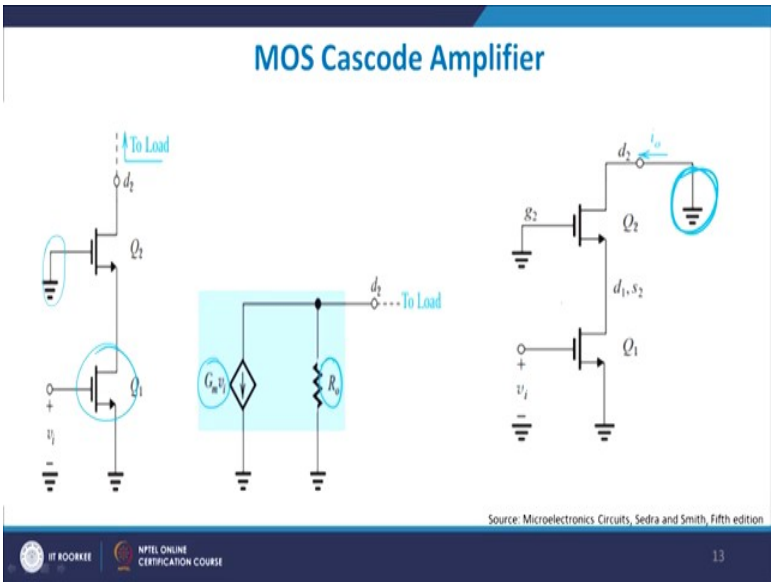

If you look at the MOS cascode amplifier therefore, as I discussed with you can actually you can actually short your gate and to the ground and then in that case it is capital g_m V_i which is basically the trans conductance of q1 into r_0 which is the output impedance as you can see from the load. So, as I discussed with you earlier also therefore, that if you short your modelling signal analysis if you short your output dc by here and then try to find the total current flowing through q1 and q 2 which will depend upon the value of V_i which you have inserted into the cascode amplifier.

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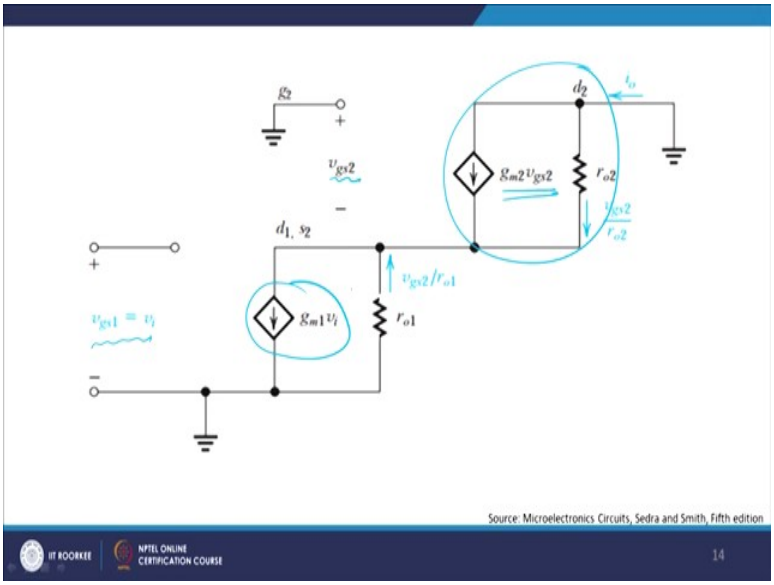

If you look very carefully therefore, this is your cascode amplifier which is given by g_{m2} V_{gs2} is the current source and g_{m1} V_i is the q1 which you see and r_{01} and r_{02} are respectively the drain to source resistances offered by these devices. And as you can see here, V_{GS1} is nothing but V_i and V_{GS2} is nothing but shorting it. So, basically V_{GS2} is that which you see in front of you. I am shorting it, right?

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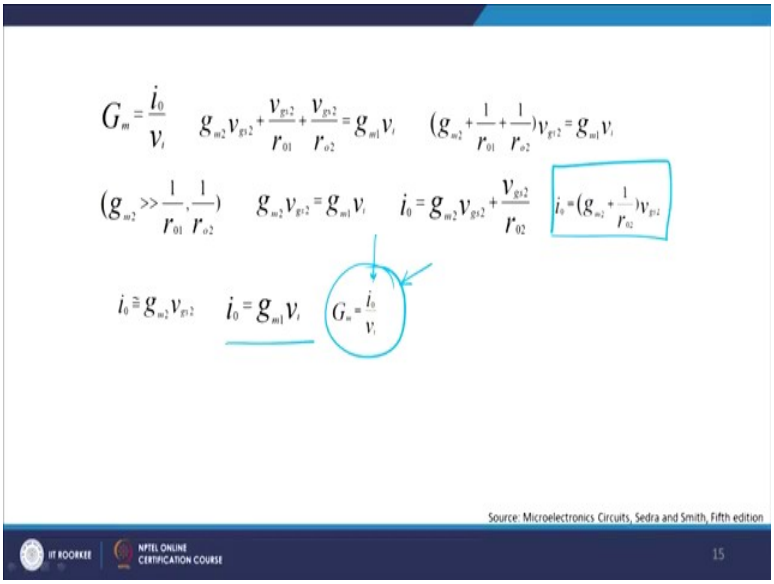

So, if you solve it and do small amount of manipulation which I did here in this in this slide you can see that the total current is basically given by g_{m2} plus 1 by r_{02} into V_{gs2}, right? And that gives you the value of output current and therefore, your i_0 is equals to gm1 into vi and your capital gm is equals to i_0 by V_i, right? And this is what you get finally at the end of the day that the capital gm which is the net trans conductance of both the devices in cascoded is given by the total current flowing through the device divided by the input voltage given to the common source stage MOS amplifier.

Now, if you want to find out the output impedance or the output resistance of a cascoded MOS amplifier the methodology adopted is that we generally short the input and we apply a unit voltage at the output and then see how much current is flowing through them. So, the voltage by current in the output side will give you the output impedance.

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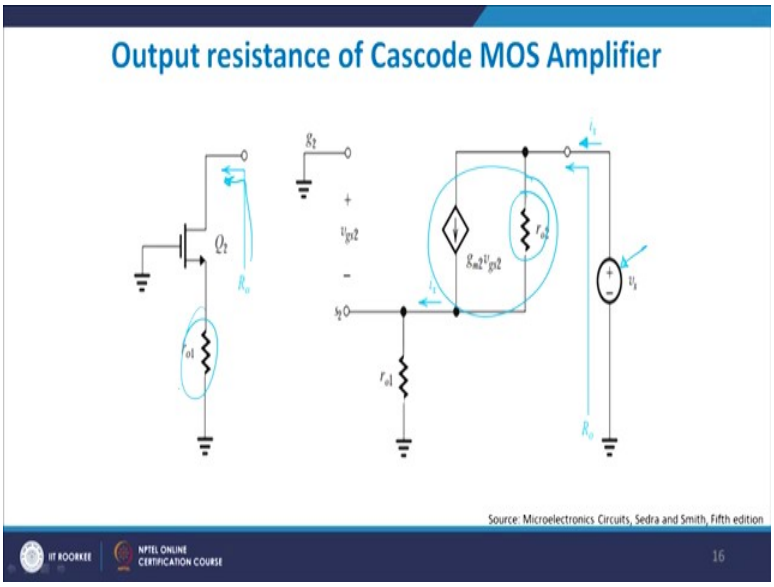

And therefore, you see this is basically your g_{m2} v_{gs2} which you see with r_{02} as the output impedance offered by the device and you have a current source here i_x here and you have applied a V_x voltage here, right? And therefore, looking from this side you have r_0 which is defined. Now, as you can see you do not have q1 coming into picture. Q1 is actually been going because you have already moved q1 and replaced it by r_{01} in this case.

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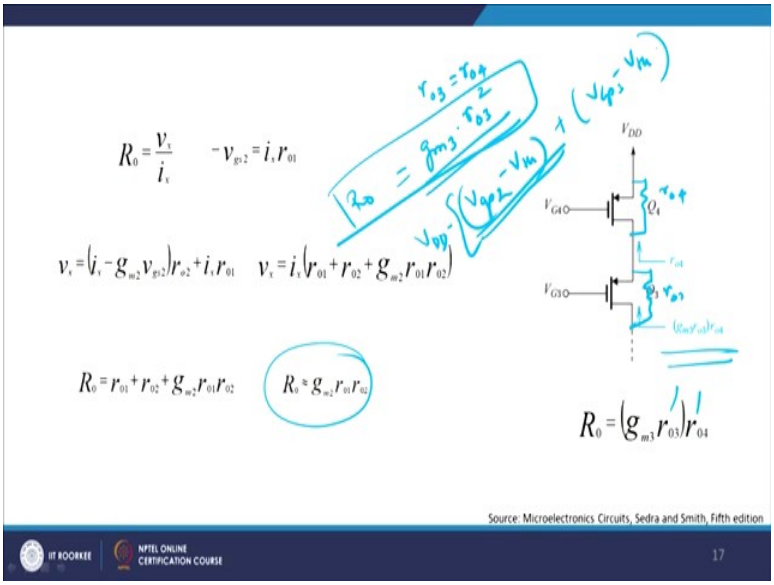

So, if you solve it the effective impedance comes out to be equal to g_{m2} into r_{01} into r_{02} and therefore, that is quite interesting that that the overall impedance seen from the output side is basically the product of r_{02} and r_{03} which is basically the resistances at these 2 particular points. So, I have got r_{04} and I have got here r_{03}. And therefore, they are sum they are product. So, basically multiplication of the 2. So, if r_0 if I assume that r_{03} is equal to r_{04} then I can safely write down as g_{m3} r_{03} whole square, right?

And that happens to be your capital r_0. So, you see if I do a single cascode I get this much if I do a double cascode my output impedance will be further high and therefore I will be able to achieve a larger gain. But the cost I pay for it is very simple that more I cascode the device more head rooms are meeting in the output because for every device to be in saturation, this much amount of overdrive is lost, right?

And as a result from V_{DD} you have to subtract this much amount of overdrives for the cascoded device. This is V_{gs2} this is V_{gs3} even if it is threshold you need to subtract it. So, you see if these are relatively large then this quantity will be relatively small and head rooms you will see and your signal integrity will be a big issue for a cascoded device.

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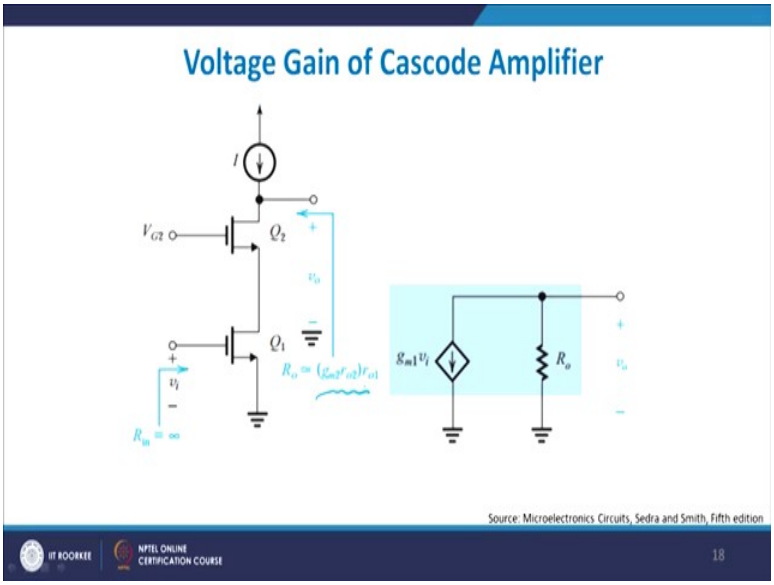

If you look at the voltage gain is very simple you just have to the input impedance will obviously be infinity because you are looking from the gate side. From the gate side obviously your resistances will be infinitely large but from the drain side if you look gm2 by r02 into r01 as I discussed with you.

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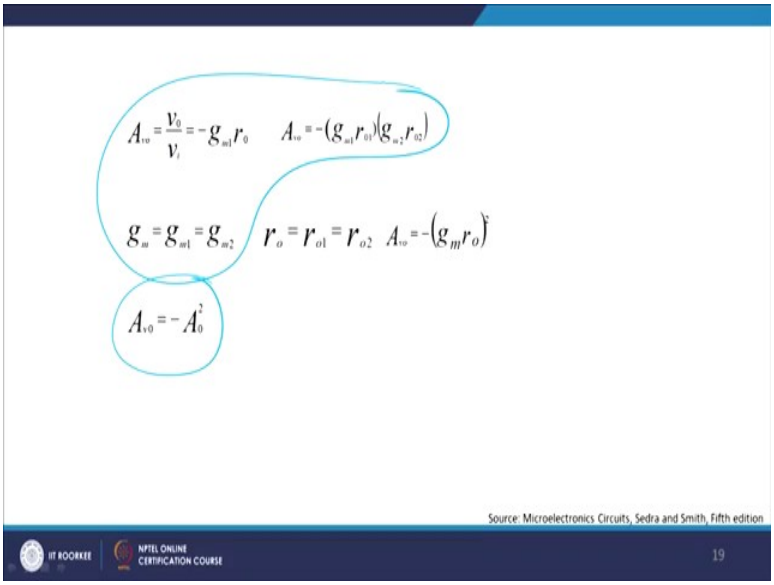

And therefore, I can safely write down the voltage gain to be equals to A_{v0} equals to minus a_0 square. So, what we have seen is that our overall gain, right; will be nothing but the square of each stage gain which means that you have 2 transistors i_b c_s and c_g then multiplication of the each stage gain will give you the value of A_{v0} with a phase change of 180 degree and therefore, you have a minus sign here. I am not doing derivation well documented in all the books and you can find it in all the text. But primarily this is what the important result and therefore, as I cascode device here, I end up having a higher gain not only that I also end up having larger r_0 which we have already discussed now.

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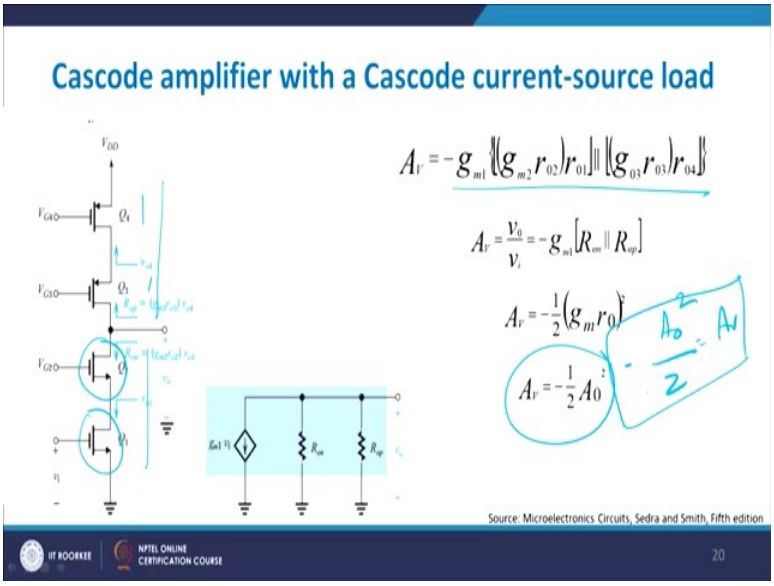

If you look at the cascoded current source which is being basically a current source which you see. So, this this is my input device q1 this is my cascoded device and these q3 and q4 are basically my load, right? And these loads will give you a value of voltage gain which is equals to a_0 square by 2. This will be with a minus sign and you will get A_v, right?

The derivation again is very simple and straightforward because looking from this side this will be in parallel to this. This is what I have done here, right? So, these 2 are in parallel. Do some small manipulations and I get overall gain to be equals to a square. So, so when you have a cascoded current source load this is a cascoded current source load q3 and q4 then your overall gain falls to half square root of 2. So, that is what you get from here 1 by 2 what you get.

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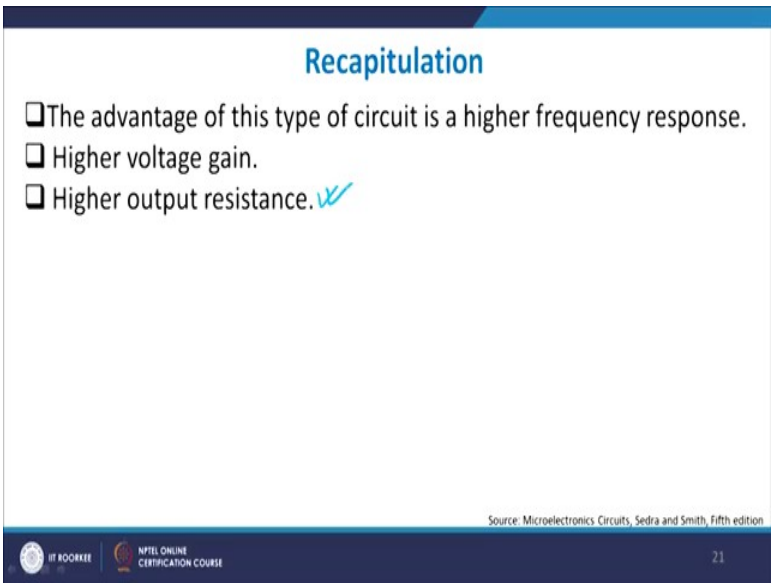

So, let me recapitulate what we did in this in this case? We saw that if I do a cascoded amplifier in place of a differential amplifier, the gain will be relatively high at the cost of voltage head rooms; my gain will be also very high, right? That is what we have seen here. So, that is what you see here that they have got higher output impedances and they have got a higher voltage gain. So, cascoded transistor means CS and CG in series with respect to each other we define them.

Cascade will be when the output of the first transistor is to the gate of the second transistor. Then we define it to be as a cascade. Cascode means when CS and CG connected to source and drain valuable to the cascade, right? So, higher the stacking or higher the number of cascode structures more will be the voltage gain and more will be the output impedance, fine? So, this is 1 of the techniques by which we can simply improve the voltage gain of a single stage amplifier. So, this is not differential single stage amplifier and you can improve it drastically, right? So, with this we finish off this module and thank you for your patient hearing. Okay!