Microelectronics: Devices to Circuits
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Lecture-43
Frequency Response of CC and SF Amplifier

Hello everybody and welcome to the NPTEL online course on Microelectronics: Devices and Circuits. We start today's module, which is named as frequency response of common collector and source follower. So, 2 configurations we will be taking up today, as far as this module is concerned. In our previous model we have looked into the common emitter configuration design as well as common source design when we do CMOS configuration. And we try to find out the high-frequency plots from that using Bode plot.

And we also saw that at high-frequency there is a degradation in the characteristics and that is because of the coupling capacitance. We also saw that there is a limit or there is a sort of a marker and that is basically a 3 dB crossover point where the gain falls by 3 dB. And at that particular point you will have a crossover between mid-frequency and high-frequency range.

After that we do have a 20 dB per decade drop in your gain and that is what we have learnt through our understanding. In our previous section we also have seen the concept of Miller capacitances being used quite often. So, today I will take up a bit of understanding of what is Miller capacitances and then we will follow the frequency response of common collector and source follower technique.

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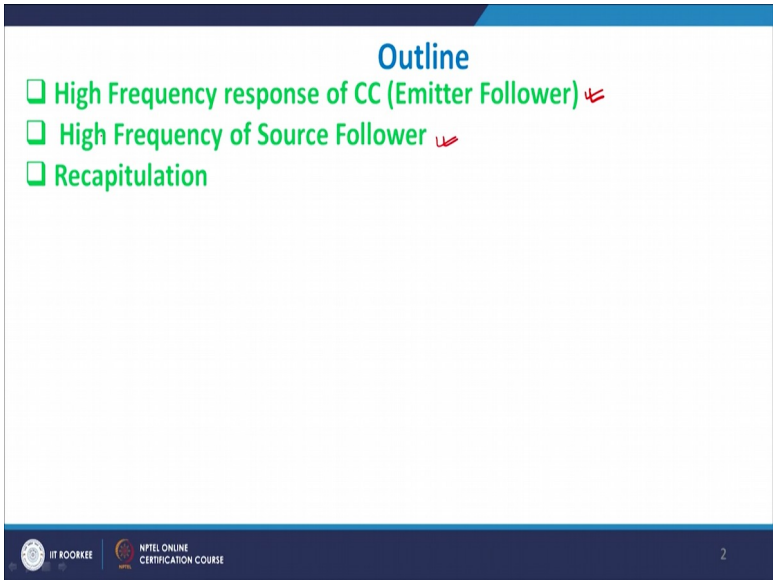

So, the outline of this module is that we will do an emitter follower and then we will do a source follower, both in high-frequency region. So, we already know what these amplifiers are, for example source follower we know has got a gain of 1 and typically you take the output from the source of the amplifier and you give input to the Gate side.

And typically, the source follows the source output follows the Gate output. And therefore, it is also referred to as source follower, that is the reason is also referred to as a source follower and then we will recapitulate. But before we move to this portion of the talk where we talk of high-frequency response of common collector.

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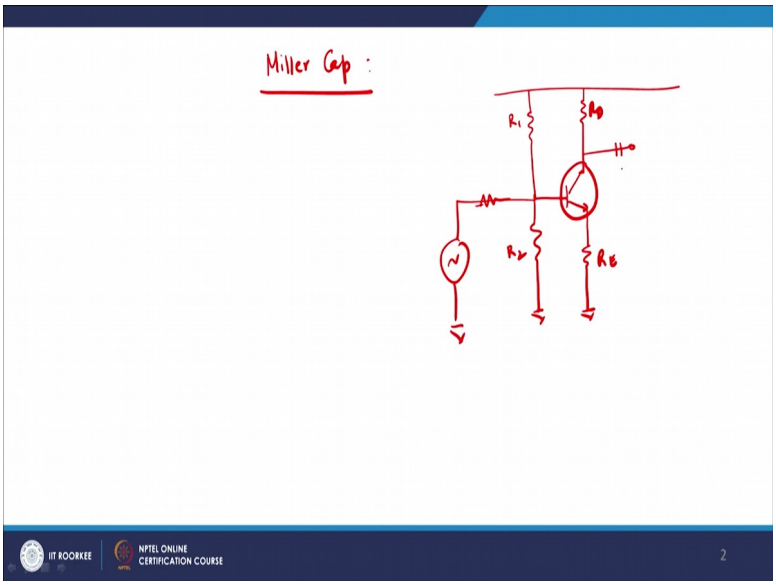

Let me explain to you as I had promised earlier the concept of Miller capacitances, because it is quite an important issue which we will be facing time and again when we will be doing analog design and Miller capacitances is one of the most important capacitances which comes into picture because of open loop gain of the system. Now, the problem is that the Miller capacitance has got a problem in the sense that if you want to increase the gain, open loop gain of the system, you end up having also a larger Miller capacitances. So, optimisation is a very important fact. So, we will take up Miller capacitances from the point of view of, let us suppose common emitter based BJT in voltage divider technique or voltage divider networks.

So, if I plot the graph of voltage divider, it looks something like this and then, common emitter if we take up, then we come to this and then we have this, right and this is R_1, R_2 and let us suppose you have got R_S here and you are taking an output from here and you have a

blocking capacitor here and this is R_1, R_2 and this is R_E and this is your R_D, this is your common emitter based circuit and you will have obviously resistance here as well as an input signal.

So, you have biased it properly in the active region and then give an input signal which is basically sinusoidal in nature to this base signal and then we will see, we will see its small signal analysis and we will see how its small signal analysis can be done.

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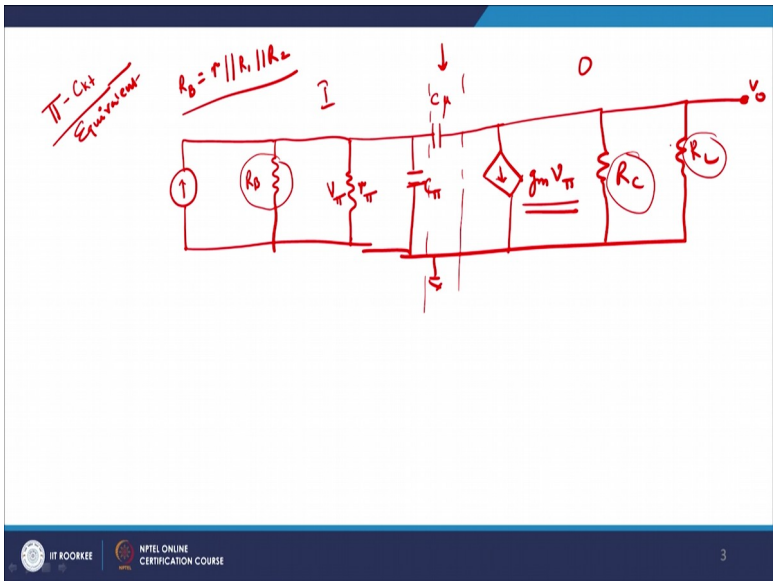

To do that, so we say that we do have equivalent circuit model. It is also known as pi circuit equivalent. So, we will do a pi circuit equivalent and therefore we will see this to be as R_B, we will refer to this as R_B, base resistance, followed by R_{Pi} and across it you will find V_{pi}, which is actually the input resistance and then you have got C_μ and you have got pi*μ*C_{pi}, I will explain to you these terms just now.

This is equal to g_m times V_{pi}, then you have got RC here, which is the collector resistance followed by the external load resistance which is R_L and this is V_{out}. So, we are at this stage looking into the fact that, just for practical purpose I will do like this. And this is your R_B, R_B is basically your base resistance, which is nothing but parallel combination of R_{in} parallel to R_2 and small r is the effective resistance between collector and the emitter side of the circuit.

Now, you see V_{pi} is basically the voltage which appears across the base terminal of the BJT, the common emitter configuration. And who is responsible for giving that, R_B is responsible for finding the value of voltage across the 2 ends and it also depends on the value of R_{pi} which you see. C_{pi} is basically the capacitance seen at this stage between base and emitter, right

because there will be a depletion capacitance as well as diffusion capacitance. And those if we add up happens to be C_{pi}.

What is more important at this stage is we should know what is C_μ, right. C_μ is basically the capacitance which you see, which is basically a feedback capacitance, which connects the input port to the output port of a 2 port network, especially a BJT here. g_m Times V_{pi} is nothing but, because BJT is a current controlled device and therefore g_m Times V_{pi} gives you the current flowing through the BJT. R_C is the collector resistance and R_L is the load resistance for all practical purposes.

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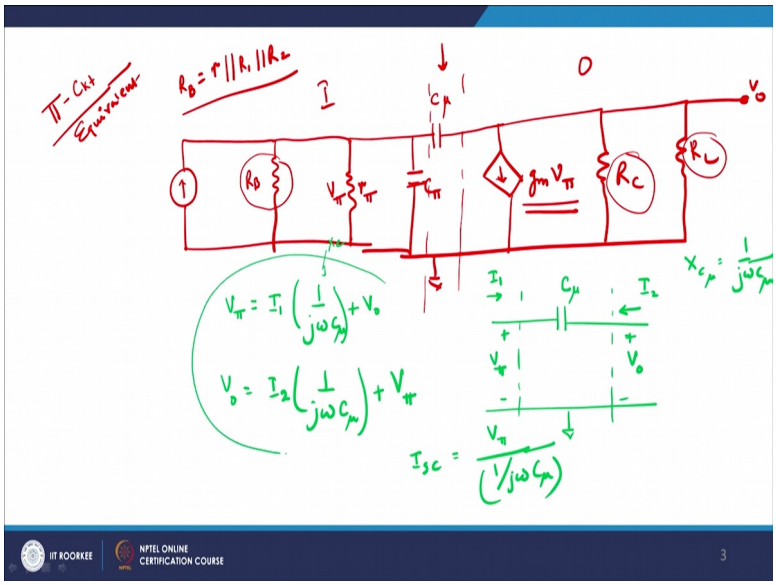

Now, we will like to model this C_μ with, this is where the Miller capacitance portion will be coming. We will like to model the C_μ here and let us see how we can actually do a C_μ modelling here in this case. Now, in this case we can model C_μ as a 2 port network and we will see how a 2 port network can actually work out and give me a result in this case. So, I have got C_μ here and I have got current I_1 and Current I_2, both going into the black box and we have got V_{pi} as the input voltages and V_0 is the output voltage.

So, basically a 2 port network as we have already seen, you must have already done in your network theory classes and you have got C_μ. Now, I can do I-V relationship, knowing that the effective impedance available to you is basically 1 by j ω C_μ. So, XC_μ will be equal to 1 by j ω C_μ, right. And that is what we will be writing now as far as this is concerned. So, we can write down V of pi to be equals to I_1 into 1 by j ω C_μ + V_0. And we can also write down V_0 to be equal to I_2, right 1 by j ω C_μ + V_{pi}.

So, you can see if you look very carefully, 1 by j ω C_μ is nothing but X_C. So, this is nothing but X_C, so X_C multiplied by I1 is the voltage drop across the objective capacitance which is X_C here and we define I_{SC} which is basically the current flowing through C_μ to be equal to V_{pi} divided by 1 by j ω C_μ. Right, where V_{pi} is the input voltage which is visible to the device, right. So, with these 2 networks or this 2 port network. we can draw the Norton equivalent circuit and we get something like this.

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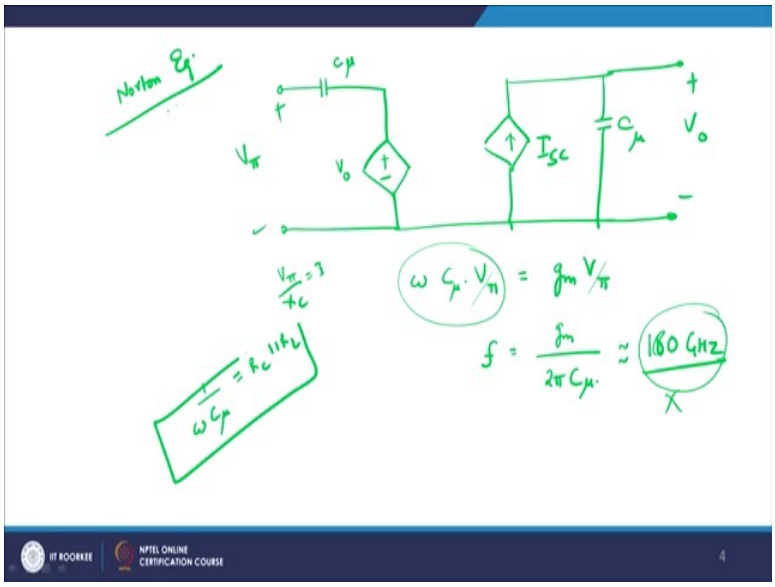

We have got C_μ here, this will be a voltage source, right, voltage source V_0 which is given by a voltage source here, this is equal to C_μ and then on this side we have got I_{SC} as the current source because of the voltage source V_0. And parallel to this you will have, of course, C_μ, right and then you will have V_0 here, this is your V_{pi}. And then you have got I_{SC} which is basically the current source. So, this is basically my Norton equivalent circuit for the common emitter based configuration.

And as a result you see this overall profile which you see in front of you. If you look at this overall profile here, then if I assume that, if this is true which you see, then I can safely write down that ω times C_μ multiplied by V_{pi} is nothing but equals to g_m times V_{pi} because both of the currents, right ω times C_μ into V_{pi} is nothing but V_{pi} by X_C. So, this whole thing is basically your V_{pi} by X_C, X_C is the reactive capacitance, which gives you the current. And that must also be equal to g_m times V_{pi}, where V_{pi} is the input voltage with you. So, therefore, if you look very carefully, and this will be 2 pi F, so V_{Pi}, V_{pi} will get cancelled out and F will be

equal to g_m upon 2 pi times C_μ, right. Now, if you put a typical value of g_m and C_μ, this comes out to be approximately 160 gigahertz, right, 160 gigahertz. Now, here comes the problem, therefore BJT, obviously cannot work at 160 gigahertz because it is a very large frequency which is seen to you, therefore it cannot work in such a large region of operation or range of operation.

So, what we should do? What we should do is we need to therefore find out what is the condition under which 1 by ωC_μ is equal to R_C parallel R_L which means that the effective capacitive reactance and 1 upon that, of course, 1 upon j ω C and the resistive, pure resistive network, when they exactly become equal to each other, we say that that is the point where you will have achieved the stability.

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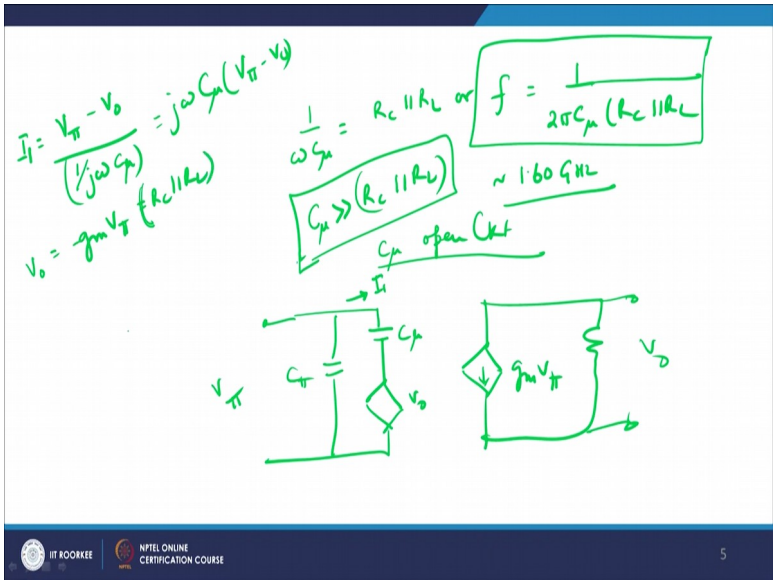

Under such a criteria, we see that 1 by ω Times C_μ equals to R_C parallel to R_L or f equals to 1 by 2 pi C_μ into R_C parallel to R_L. Right, this is the frequency of operation of the common emitter based BJT. And if you put approximate values of R_C, R_L and C_μ, I get this to be approximately equal to 1.60 gigahertz. So, we have drastically reduced the frequency of operation from 160 to 1.60, about 100 times decrease has been there in terms of the operating frequency.

And this can happen, provided C_μ is much larger as compared to R_C parallel R_L, right. So, you have to ensure that the capacitive reactance of the device is much much larger as compared to R_C parallel R_L. Right, and therefore I can safely assume that if C_μ is basically an open circuit therefore, right. Why, because it is much much larger compared to R_C parallel R_L and

therefore, it is open circuit and therefore if I draw the effective circuit diagram, I get something like this, this is V_0, this is C_μ and then you have got C_{pi}, right and then this goes to the input side.

And then in the output side you have got g_m Times V_{pi} and then you have got resistance RL and this is your output voltage V_0 and this is V_{pi}. And from here, this is a current I which is flowing through the device, I_1. Then I can safely write down I_1 to be equals to V_{pi} minus V_0 divided by 1 over j ω C mu because that is what we get, it must be equal to j ω C mu into V_{pi} - V_0. This will go up and you will get j ω C_μ into V_{pi} minus V_0. We also know therefore that V_0 is equal to - g_m Times V_{pi}, g_m Times V_{pi} multiplied by R_C parallel R_L, right.

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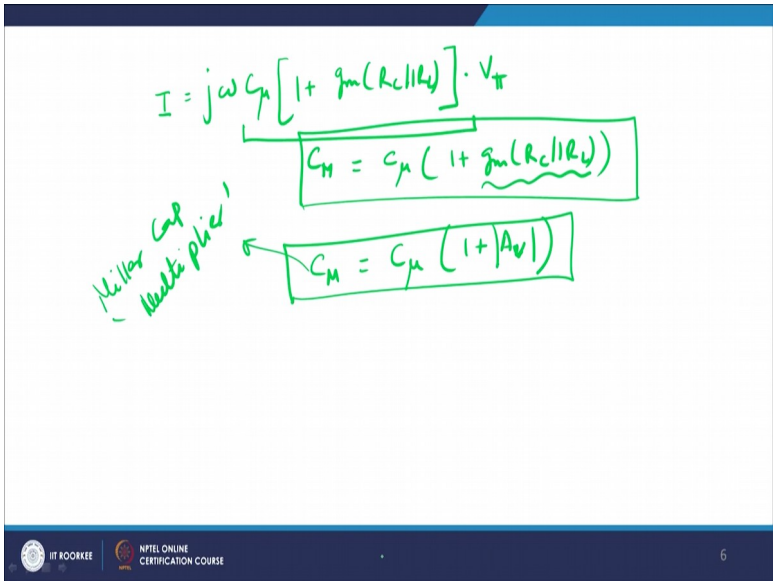

And therefore, I can write down the current I to be equals to j ω C_μ, right into 1+ g_m Times R_C parallel R_L, right into V_{pi}. And therefore, you see C_μ which was initially the effective capacitance seen is actually getting translated into a slightly larger value of capacitance and this is basically my CM or the Miller capacitance and is given as C_μ into 1+ g_m times R_C parallel R_L. Fine.

So, this is your CM which you get, this CM is equal to C_μ into 1+ g_m times R_C parallel R_L. And if you look very carefully, this is nothing but the voltage gain and therefore I can write down Miller capacitance as it CM, C_μ is equal to 1+ A_V mod of that. And this is what is known as the Miller Cap multiplier. Right, so this is the Miller cap multiplier, which occurs because you do have some gain, open loop gain of the system, which gets multiplied with C_μ

and that appears on the output side as CM. This component is basically therefore known as the Miller component.

So, what is the Miller component in BJT or CMOS? It basically is the component of capacitances which connects between the input and output and raises the value of voltage in the output side beyond a particular limit. That is what is known as Miller capacitances. Let me therefore give you physical reasoning behind this one.

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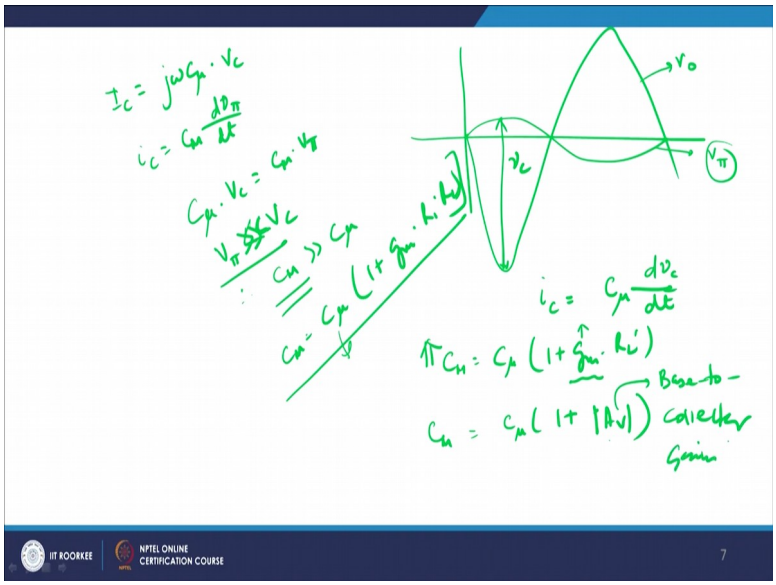

So, let us suppose I have got an input and output and my input is given by the small V_{pi}, this is V_{pi}, this is my input V_{pi}. My output will be obviously 180 degree phase shifted but highly amplified and therefore I get this as my V_{out}, this is my V_{in} and this difference suppose we refer to this as V_C or the voltage across the capacitance C. I can safely write down IC to be equal to C of μ dV_c by dt, right. We can also write down I_C to be equal to j ω C_μ into V_c as we have discussed just now.

I_c is also equal to CM times dV_{pi} / dt, so if you equate these 2 together, I get C_μ Times V_C equal to CM times V_{pi}. Right. Now, we already know that V pi is much much larger as compared to V_C. And therefore CM will be obviously, sorry, V, this is true that V_M is much much smaller as compared to V_C and therefore my CM will be much larger as compared to C_{pi}. And that is true also because CM is nothing but C_μ into 1+ g_m times R_1 into R_2 or R_1 parallel to R_2, right.

And you get overall Miller capacitances available to me, depending on the value of your feedback capacitance. This is the basic criteria or the basic concept of a Miller capacitance

and as we have seen just now that Miller capacitance gives you an enhanced value of your this thing, of the output. But then you see, as I discussed with you, CM will be equals to C_μ into 1+ g_m times R_L'. So, if you want to increase the gain or bandwidth or you want g_m to be large, you also end up having a larger CM.

A larger CM implies that your speeds will be restricted drastically and therefore, you have to do a sort of manipulation, a sort of optimisation between input and output in this case. And they have to make them look such that they are almost equal to each other. So, this is basically gain and it is also written as C_μ into 1+ mod of A_V, right. And this equals to CM, this is also referred to as base to collector gain.

So, this base to collector gain which you see as A_V and this gain is typically of the order of 10 to the power 5, 10 to the power 6, depending upon the type Op-Amp which has been chosen in this case. With this knowledge we have understood what is the Miller capacitance, what is the origin of Miller capacitance and how are Miller capacitances related to the overall capacitances in the system. Let me switch back to today's course and explain to you how it works out.

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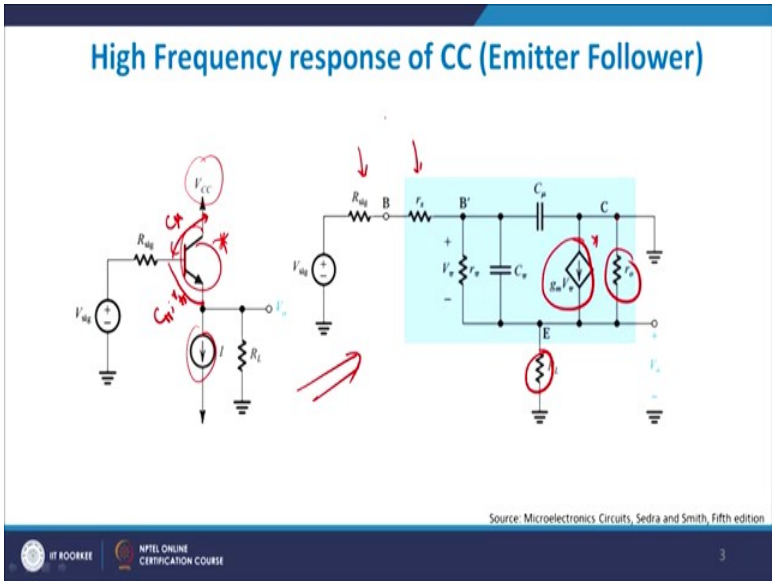

For example if you are doing common collector or emitter follower design, then this is what it looks like come on the emitter side you have the current source and the collector is connected to V_{CC} and the signal is inserted to the base side of the BJT. If you plot its equivalent circuit diagram, it looks something like this. So, g_m times V_{pi} is nothing but the device itself, so this is the device itself, right. Who is surrounding the devices, the collector is connected to R_0, it is basically an open circuit resistance value.

You will have C_μ and C_{pi} as the resistance between base and collector. So, between base and collector we will have C_μ and between base and emitter you will always have what is known as C_{pi} and R_{pi}. Fine. And this makes our life difficult in the sense that these capacitances become higher and higher at enhanced values of operation or resistance of the device. So, R_0 is basically my output resistance of the device, R_L is the load resistance, R_X and R_{Sig} are the input resistance seen by the device when the device is operating in saturation region.

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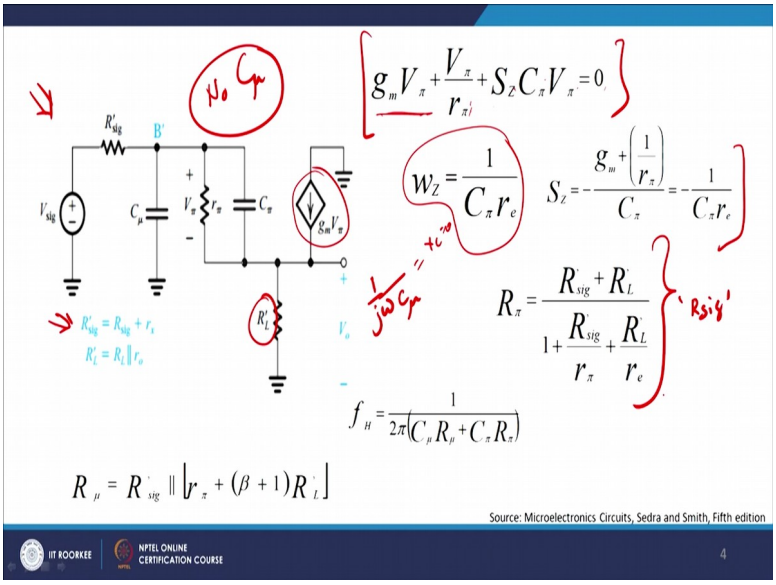

So if you go back to your previous discussion, what I was doing was C_μ if you see carefully has been removed. So, there is no C_μ and the reason is that at such a high, so when you are, so you remember 1 upon j ω. So, when your frequencies are relatively very large, then these are actually almost equal to 0 and therefore they can be shorted and therefore the capacitance have been shorted, the C_μ capacitances have been shorted.

And you get this picture here which you see in front of you, where V_{Sig} is applied signal voltage and C_μ is the applied capacitance and C of pi is basically the pi value or the input capacitance of the system. g_m times V_{pi} is nothing but the current which is flowing through the devise because this is basically a current control device.

So, I get R_{Sig}' to be equal to R_{Sig} + R_X, and R_L' with equal to R_L parallel to R_0, right. R_L prime equal to R_L, R_L is the load capacitance seen from the outside world and R_0 is the output impedance of the device. So, if you do a small Kirchoff's law solution then I get g_m times V_{pi} which is nothing but the current must be equal to V_{pi}, again the current, must be equal to S Z C_{pi} V_{pi} and this almost be equal to 0.

So, the net current should be equal to 0 because before also the current was equal to 0. From there I get ω Z equals to 1 by C_{pi} r_e, right. And therefore I can write down f to be equal to 1 by 2 pi C_{pi} r_e, right. Similarly, we can write down SZ to be GM +1 by R_{pi} upon C_{pi} is equal to 1 minus 1 by C_{pi} times re, this is the value of SZ. And similarly, R_{pi}, which is basically the resistance offered by the other resistances is given by this formula where R_{Sig}' + R_L' upon 1+ R_{Sig}' by R_{pi} + R_L' by r_e.

So, if you look at R_{Sig} is nothing but the signal resistance offered by the signal to the device itself. So, if you plot this graph or if you try to find it out, I will get F_H equal to 1 by 2 pi C_μ R_μ + C_{pi} R_{pi}. And this is what very important result which we get that the holding frequency or the frequency where you are holding the mid-frequency gain is basically determined by the capacitances and resistances of the device itself. And that gives me quite an interesting result as far as designing is concerned.

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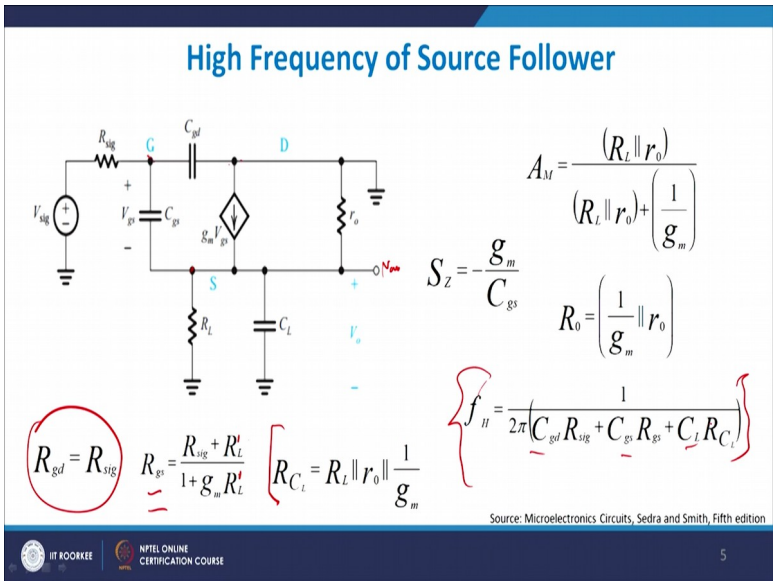

Now, if I do, so we are finished with common collector, let me do a source follower. As I discussed with you, source follower if you look very carefully, you are actually extracting the voltage from the source itself. So, this is V_{out} here, right and you are extracting it from a source. Similarly, if you look very carefully, R_{GD} equal to R_{Sig}, R_{GD} is gate to drain, gate to drain is basically your R_{Sig} and RGS equal to R_{Sig} + R_L' upon 1+ g_m times R_L', right, these are all primes here which you see.

And from there I get RC_L to be equal to RC_L to be equal to R_L parallel to R_0 parallel to 1 by GM, right. And therefore, your F_H happens to be all the combinations of R_{GD}, R C_{GS} and CL, load capacitances. So, in a source follower technique or in a high-frequency source follower technique, the resistances offered by the gate to drain overlap and gate to source overlap makes quite a lot difficult calculating the value of the frequency F_H. And that is quite an interesting task.

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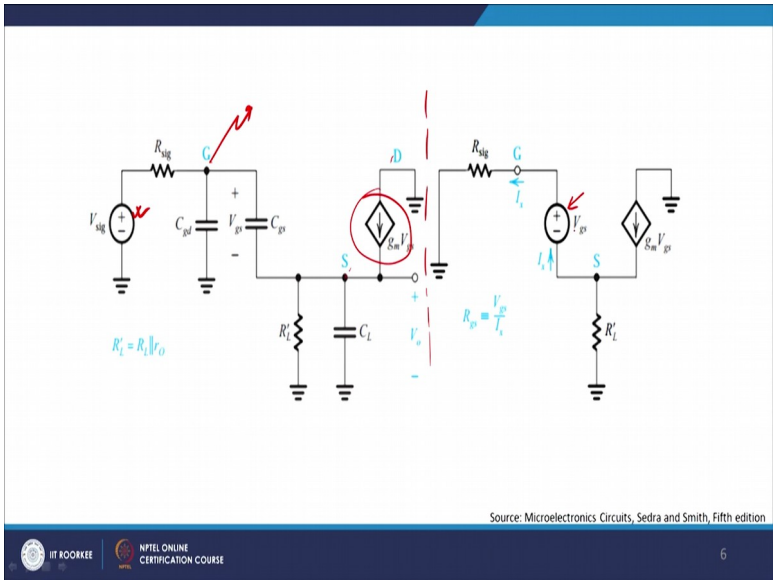

So, if I just break it down into a smaller piece here and show it to you, then I get R_{Sig} into V_{Sig} into C_{GD}. So, this is my gate terminal here and I have got C_{GD} and this goes via the source site to the drain side. So, this is the source and drain and this is the collector, drain current which is flowing through the device given by GM times V_{GS}. Right, so if you see and if you see the plot between these 2, they are exactly the same, the only thing is that this V_{sig} has been replaced by V_{GS} and this splits in the input side of the design.

And GM times V_{GS} is the amount of current which is flowing in the output side. So, if you make it V_{GS} large, this also becomes large, so that the same current is flowing through both the arms of the device. And R_L is the tail current source resistance which is being offered by the device itself.

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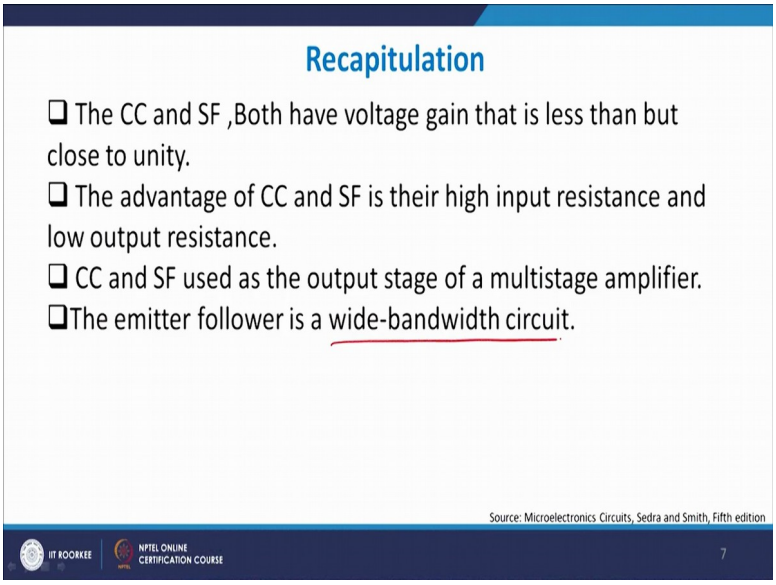

So, let me recapitulate what we did till now and let me show to you how it works out. If you look very carefully, both have voltage gain less than unity, both common collector and source follower have lesser gain which is quite less than unity. Obviously the advantage of this common collector and source follower is that it has got typically very high input impedance and low output impedance and therefore, matching of signals can be done very well using this technique, using this either CC or SF. Similarly CC or SF are also used as the final stage of multistage amplifier. And emitter follower has got a very wideband gap or bandwidth circuit in reality.

So, it has quite a large bandwidth by which it works fine and gives me a very good result as far as designing is concerned, in terms of both the system design as well as for the design available to us through the overall network of things. So, this takes care of approximately most of the understanding part of our common collector and source follower technique. So, we have seen that common collector and source follower, both have voltage gain less than one because the gain is very small but they are very good impedance matchers because their impedance is dependent on the input and output profile.

The advantage is that both have the high input impedance and very low output impedance and these impedances can be changed by varying certain input parameters. Generally, these CC and SF are used as the final stage of a multistage amplifier. So, typically if you are using a multistage amplifier, say 2 stage or 3 stage, then the last stage will be your CC or SF. Where you get the unity gain but your impedances are properly matched between input and

output. Emitter follower is basically a very wide band gap circuit, not only this which gives me typically a very large bandwidth to a larger extent.

The cost I pay for it is basically that though its bandwidth is large, your gain is relatively small, it is almost unity gain which you see. And therefore the price we pay for the larger bandwidth is the lower gain, right. And that is a n important drawback of this CC and SF. So, let me recapitulate what we did today. I explained to you what is a Miller capacitances and how Miller capacitances play in important role as far as determining the mid-frequency gain is concerned.

And we also saw that if you have Miller multiplier factor, the output capacitances will actually be multiplied by a factor of $1+ g_m$ times R_d which is basically my A_V and will appear in the output side, that makes my life difficult. And thirdly is that if I want to therefore make my capacitance small, I also end up having reducing my gain of the mid-frequency gain of the amplifier, right.

Subsequently we looked into the common collector and source follower technique and we saw the various principles and formulae used for doing that. Where these will be used, we also saw that and what will be the voltage gain for common collector and source follower technique. This we have followed in this module. I thank you for your patient hearing.