Microelectronics: Devices to Circuits
Professor Sudeb Dasgupta
Department of Electronics and Communication Engineering
Indian Institute of Technology, Roorkee
Lecture-42
High Frequency Response of CS and CE Amplifier

Hello and welcome to the next module of the NPTEL online certification course on Microelectronics: Devices and Circuits. We take up today's module as high frequency response of common source and common emitter CMOS-based amplifier. And we will be concentrating on the frequency spectrum or the frequency, how does the gain of the amplifier change with respect to frequency. What is the motivation for such a module? The motivation is that since these are basically used as audio amplifiers, therefore they need to be giving me a constant gain irrespective of large change in the frequency of the input.

So, my voice goes from 20 hertz to 20 kilo hertz, right, the typical audio frequency range. Now, if the amplifier frequency, if the amplifier high-frequency gain suddenly drops down, say at about 18 kilo hertz, 18.5 kilo hertz, the gain drops down. Then those frequencies or those voices, the voices with those frequencies, the audio range in those frequencies will not be properly amplified and I will not be able to hear those frequencies in a better manner.

So, ideally the gain should be almost independent of frequency for CS and CE mode design. And that is the reason we need to know, what are the factors which influence the behaviour of the spectrum of the frequency or the band of the frequency. And we will be concentrating currently on the high-frequency part. Just before we move forward, let me recapitulate what we did in our previous module. We saw that, in our previous module we saw that we were actually doing what is known as the Bode plot, right, we were doing Bode plot.

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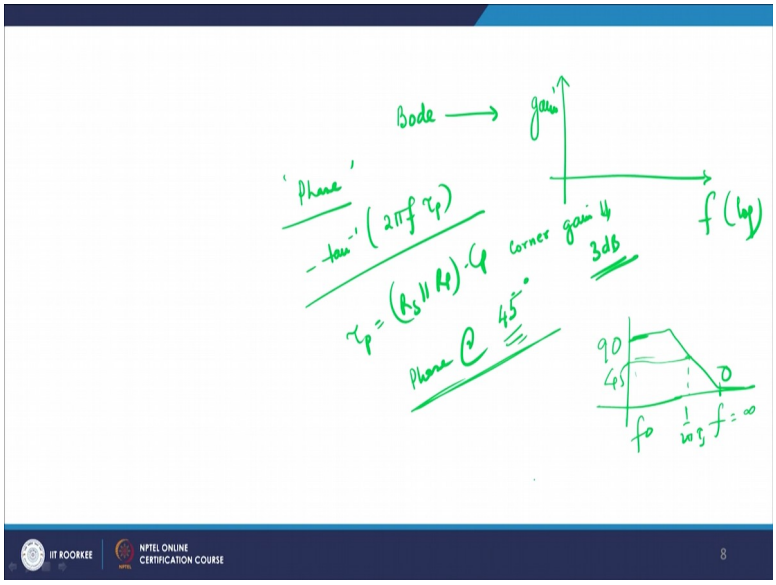

And in the Bode plot we were actually looking into the, what is a Bode plot, that we saw that Bode plot was basically gain with respect to frequency we saw that and frequency should be in log scale. We also saw how to make this bode plot and we expected what is known as the coordinate frequency where the gain drops to 3 dB of its original value and at that particular point, what is the frequency which should be able to gather.

We also understood what is known as a phase or phase margin or phase and is defined as minus of tan inverse 2 pi f of tau_P where tau_P is given as R_S parallel to R_P multiplied by C_P. Right and typically the phase at unity gain, which is basically meaning whenever you have unity gain, is approximately equal to 45 degrees. Right, the phase margin, the phase is basically 45 degree. So, we should be able to find out at 90 degrees when you have, you will have added a given frequency is very 0, frequency 0 you will have 90 degree and then it goes on and becomes, phase becomes at very large value it becomes 0.

Somewhere in the middle where the frequency drops to 1 by 2 pi Tau_S, this is 45 degree. So this is how the phase varies for an amplifier, right. And the gain how it varies, we have already seen working as a low pass, and the high pass, as a bandpass filter we can I do it. We now come and we now discuss about the frequency response.

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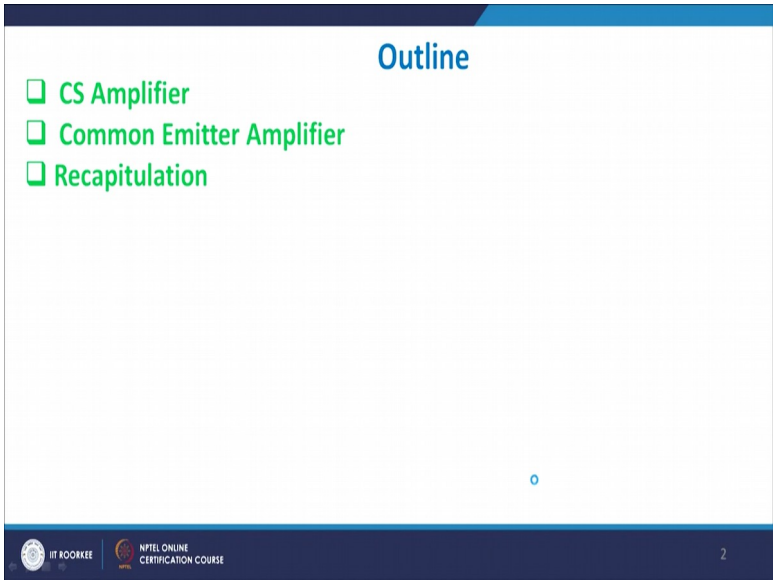

So, what is the outline of this current topic? The current topic is that we will take up another CS amplifier which we have already been doing previously also. This is basically common source amplifier, right and then we will look into the common emitter amplifier in the BJ T configuration and then we will be recapitulating the high-frequency response for CS and this thing, for common emitter.

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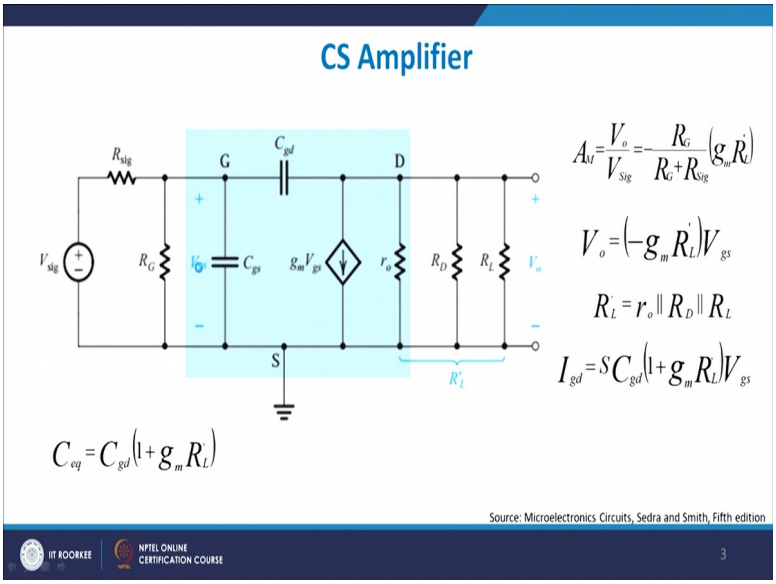

This is the small signal diagram for common source amplifier.

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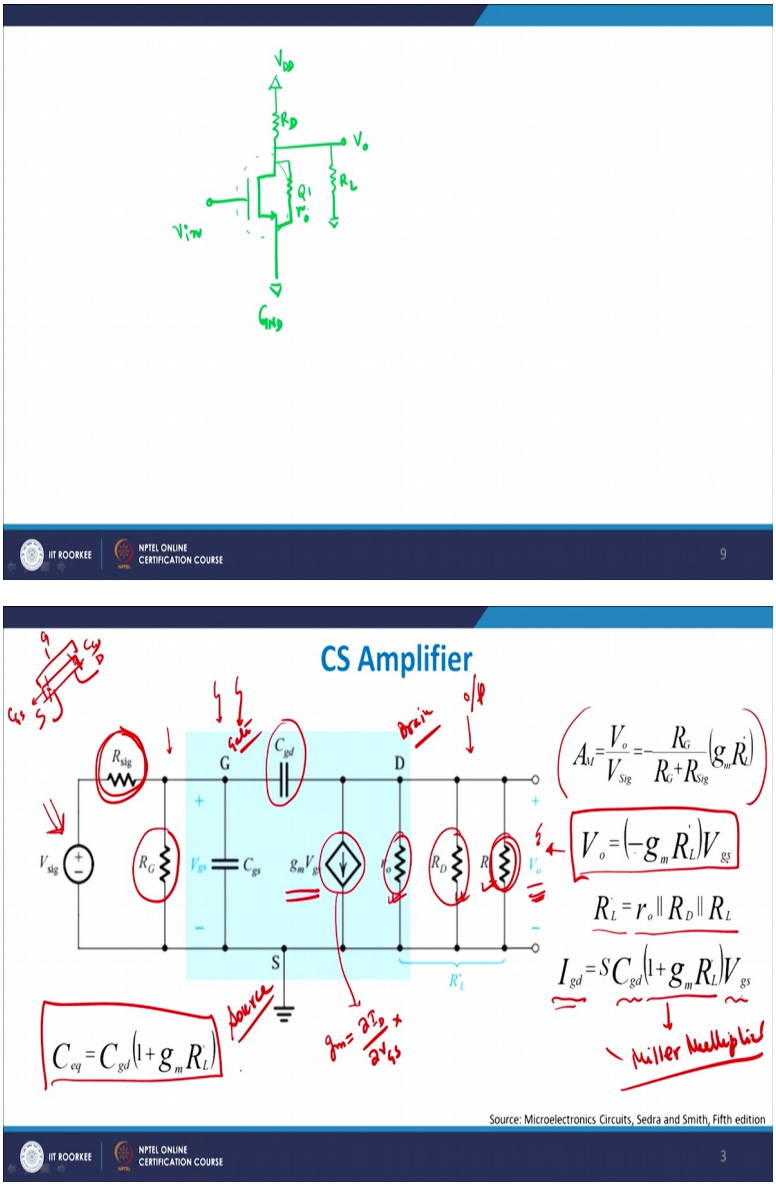

Let me just draw for you against the common source amplifier itself. The common source amplifier looks something like this, we have already explained it earlier also, that it looks something like this. Right, I am not giving any source degeneration resistance here. And this is the output I am taking and this is my V_{DD}, this is ground, and we have input here, then we do have gate here, we do have a MOS device here, which is basically the MOS device here and this is one output. Right, so if you do a corresponding small signal analysis here, I can replace this Q1 by GM V_{GS}.

Because GM is basically the trance conductance, right and GM is defined equal to $\partial I_D / \partial V_{GS}$. So, if you multiply this with V_{GS}, V_{GS} gets cancelled out and you get, we are left to the current source. So, therefore we have already discussed this point that GM multiplied by V_{GS} will

give me this current source here. Look at the input part 1st of all, so this, we will look at the blue part just now. This blue part is actually the device part. And this is certain the circuit which we insert in input side and this is the circuit which you insert in the output side.

So, if you go back, we generally have an external load here, R_L, right, and this is my R_D and I have also a resistance across source and drain given by R_0. So, this R_0, R_D and R_L are actually parallel to each other. We will come to that later on. This is the signal source which we are giving, right and this is the ideal voltage source. So, it will have almost 0, very low output impedance. But in reality there will be always a signal impedance available to me and therefore that is given by this R_{sig} which you see.

So R sig is in series to the voltage source. You also have R_G which is basically the resistance which is at the gate side of my design. It is typically very large value because the gate resistances are very large. Right, and they are held parallel to the gate terminal or the gate node. So, it is very large primarily means that for all the V sig will appear across the gate. So, what happens primarily is that your signal voltage, which is V sig here goes through a potential divider network of R_{Sig} and R_G and depending on the relative values of this R_{Sig} and R_G, a part of V_{Sig} appears on the gate side of it.

You will ask me why we do all these things, the reason being that if you do not do it, there might be a chance that the voltage, that suppose the voltage, the voltage source suddenly gets shorted and the voltage source suddenly the rises to a very large value. Then it might destroy the MOS device permanently and that is the reason we generally give resistance biasing or potential divider biasing at the input side, so that not all of the voltage of the gate appears, of the input signal appears on the Gate side.

So this is all about your left-hand side. Now, on the right-hand side, which is basically your output side, if you look very carefully, you have R_D which is basically the drain resistance, you have a load resistance R_L here and you have output voltage V_0. And this R_0 is the applied voltage. Now, if you look very carefully, if we look at this diagram, for example, very simple, it is output by input, V 0 is output voltage by V Sig is the input voltage. It is given as GM multiplied by R_L', where R_L' is basically the parallel combination of R_0, R_D and RL.

So, this is the effective resistance seen by the output voltage source from this side. So, GM multiplied by R_L' multiplied by R_G divided by R_G into $R_G + R_{Sig}$. Therefore, I can safely write down V_0 to be equals to minus GM times R_L into V_{GS} because V_{GS} is the input voltage and

your minus GM times R_L is basically the voltage gain which you see and R_L' is this one. Now, the gate to drain voltage, now let me to this blue part and explain to you the other principles here.

See, you do have, this is the, MOSFET is basically as you remember from your basic days, that is basically 3 terminal device. It is 4 terminal but for all practical purposes in this case, we will take as 3 terminal. So, this is your gate, this is your drain, right and this is your source. So, source, gate and drain, so these 3 terminals are there with me. Now, a gate to drain, you will always have a capacitance which is the depletion capacitance by virtue of overlap between gate and drain.

Remember this is C_{GD}, right, you also have C_{GS}, gate to force. So, if you remember your basic MOS device structure and then it looks something like this, then you have something like gate and this is your gateway, this is your gate, this is your source and drain. So, you will always have a capacitance here and the capacitance here. This is C_{GS}, right and this is your C_{GD}, right. So, I have C_{GS} and I have a C_{GD} capacitance across the 2 ends which is with me.

Now what happens is that once you multiply, so if you want to find out the total current flowing through I_{GD} or the gate to drain current, then because of the overlap capacitances, then it is basically C_{GD} multiplied by V_{GS} that is the current. But you also have a 1 + GM multiplied by RL Prime. This is known as what is known as the Miller multiplier factor. This is the Miller multiplier. It means that your C equivalent, if you look at C equivalent, it is nothing but C_{GD} multiplied by 1+ GM times R_L'.

So, which means that quite an interesting phenomena, that gate to drain capacitance appears in the output side as a increased value of capacitance by how much, 1+ GM times R'. So, higher the value of your transconductance of your MOS device, more will be the current of course but then more will also be the gay to drain capacitances. From where I am getting this, we will not discuss at this stage but at this stage we will just assume it to be Miller indices or Miller multiplier.

If time permits we will come to this later on which means that because of some overlap, you generally have a Miller capacitances which comes into picture and these Miller capacitances tend to show an increased value of your capacitances. Right and therefore I get C_{GD} 1+ GM times R_L which you see here.

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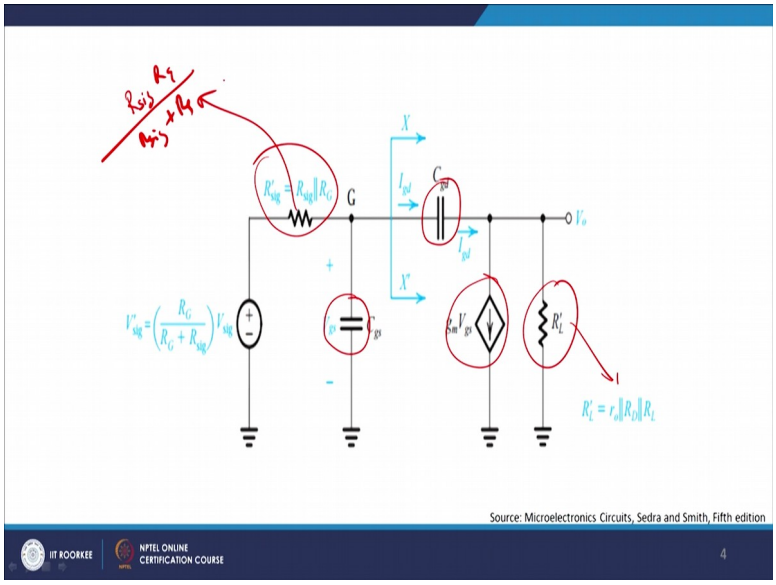

And from here if I go back to my previous, and therefore if we just drew the small signal model of it, I get C_{GS} here, I get C_{GD} and this is GM V_{GS} is a current source, this R_L Prime takes care of R_0 + parallel to R_D parallel to R_L. And this R_{Sig} is basically R_{Sig} is parallel to R_D, it is basically R_{Sig} R_G divided by R_{Sig} + R_G. Right, this value, this is a typical value which you get. And this is the effective value which you get for all practical purposes.

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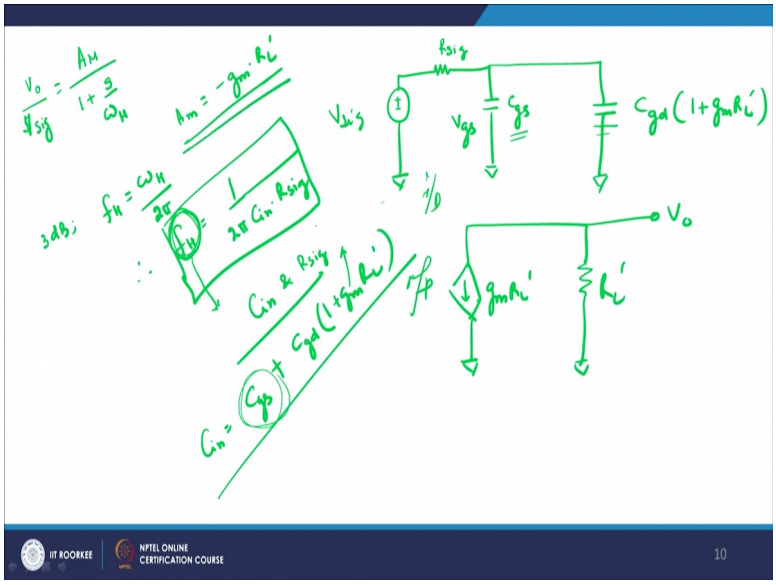

Now, let me come to explanation here and explain to you maybe a simple derivation here. Let me show to you that I have a V_{Sig} here, I have R_{Sig} here, there is C_{GS}, gate to source across which you will have V_{GS} and this is your R_{Sig}, this is your V_{signal} and then you have your C_{GD} into 1+ GM times R_L'. So, this is the effective value which you see in front of you. Now, if you therefore plot the output side, I can write it safely as GM times R_L', right, this will be in parallel to R_L' and there will be output here.

So, this will be the input side and this is your output side, right. And I get R_L' multiplied by V_0. Now, R_L' consists of 3 resistances and these 3 resistances will be responsible for giving you the overall picture. Now, therefore, if you plot V_0 by V, sorry V_{signal}, output voltage by V_{signal} voltage, I will typically get a general form will be 1 + S by $omega_H$ in terms of S. Where A_M is the mid-frequency gain, which is independent of frequency, remember, is nothing but minus GM times R_L.

And this is the mid-frequency that you get here. At 3dB if you want to find out, then I get F of H equals to omega H by 2 pi and therefore, I get F of H to be equal to 1 by 2 pi C_{in} into S into, sorry, let me just again write down this whole thing, so this is easy here and then, so I get 2 pi, right, C_{in} into R_{Sig}. This is your sort of 3 dB sort of corner frequency. So the corner frequency which is again a 3 dB corner frequency is being primarily determined by the input capacitance here and the R_{Sig}.

What is input capacitance? Input capacitance is nothing but C_{GS}, gate to source + C_{GD} into 1 + GM times R_L'. Why, because this and this are not parallel to each other. And therefore, they

will be adding directly with respect to each other. Right, and you can see quite an interesting phenomena which has come out from here. That, therefore depending on the value of C_{GS}, the frequency of the, cut-off frequency or the 3 dB frequency will go on changing. Similarly, if you make your GM higher, because you want the current to be high because you want the gain to be high, this came to be high for example, you end up having a smaller value of F_H, right.

So, your smaller value of F_H primarily means that your cut-off frequencies are lowered now. It is not a good idea if you want your bandwidth to be very large and that is the reason that the designing is a bit critical, that just simply by increasing the transconductance of the device will not always make your life easier and this is what the problem area which you face in general you get.

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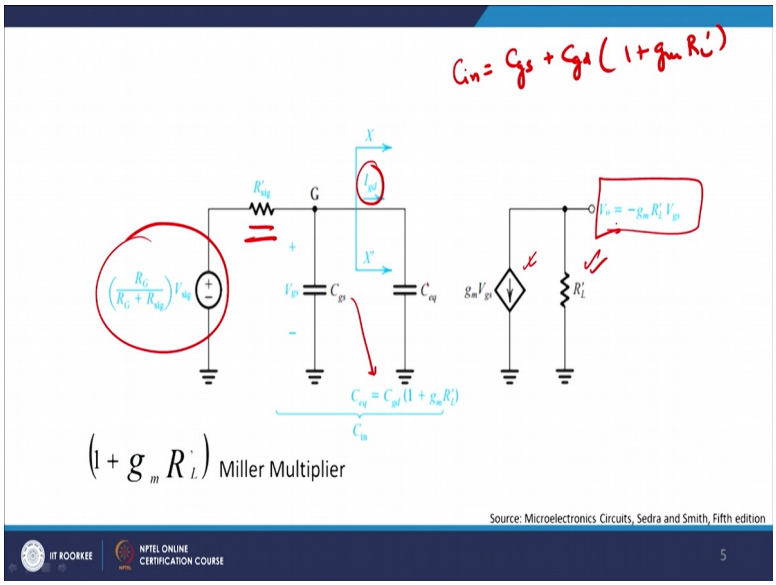

So, this is the structure which you get from here, let me come therefore to the effective as I was discussing with you just now. That I have got, this is the effective resistance which is seen from the device, this is the signal resistance, and current flowing through is I_{GD}, gate to drain and C equivalent is given by C_{GD} 1+ GM times R_L, whereas C_N is therefore equal to CGS + this quantity. So, C_{in} will be the sum of these 2 quantities and that is the reason I was telling you that effective C in value will be given as C_{GS} + C_{GD} into 1 + GM times R_L'.

And that is what you will get here. This is R_L' with you get and this is the MOS device equivalent circuit and this is my output voltage, final output voltage given by minus GM times R_L' minus V_{GS}. Negative sign because it is phase shifted by 180 degree and therefore

you will always have a negative sign attached to it. With this knowledge, let me therefore plot for you the function which we have just now derived.

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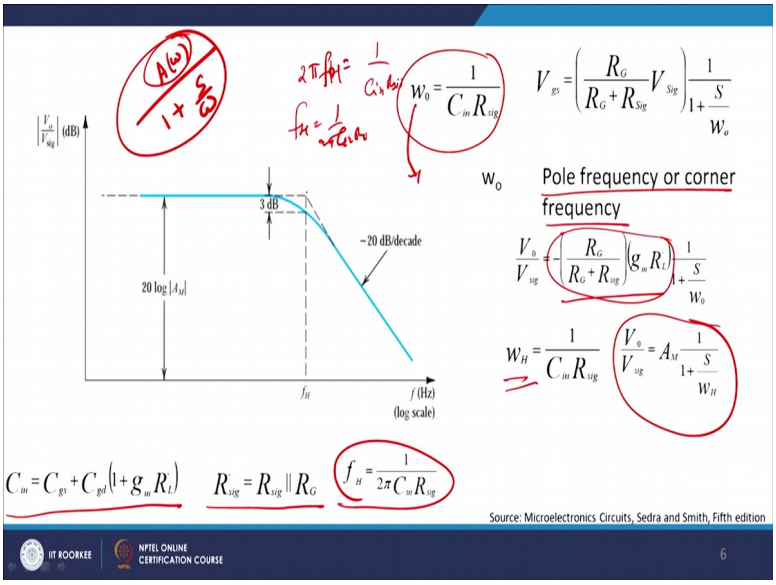

And if you look, in this omega as I discussed with you was 1 by $2C_{in}$, so this omega 0 is basically 2 pi F of H is equal to 1 by C_{in} R_{Sig}. So, F of H will be equal to 1 by 2 pi C_{in} R_{Sig} and that is what is written here also. So, this omega is referred to as the pole frequency or the corner frequency and it is given by this. So, if I write down in terms of V_0 by V_{Sig}, it is minus R_G by R_G + R_{Sig} into GM R_L into 1 upon 1+ S by omega 0.

Because if you, as I discussed with you, general formula is A of omega, which is the mid frequency gain upon 1+ S by omega that is the general formula for any gain structure of any amplifier. This is the mid-frequency gain, mid-frequency gain is given by this quantity. So, this divided by 1+ S by j omega. Omega H is given by 1+ C_{in} into R_{Sigma} and therefore this is the formula which I just now discuss with you here. Where therefore, as I discussed with you, C_{in} is equal to C_{GS} + C_{GD}, research, where R_{Sig}' is equal to this much and F_H equal to1 by 2 pi C_{in} into R_{Sig}.

Therefore, at F_H, which is this one, I would expect to see a 3 dB drop in my gain. Right, so the corner frequency is that frequency at which I get a 3 dB drop in my gain. And the point at which this happens is determined by the value of C and an R_{Sigma} which is the output impedance of my voltage source which is driving the MOS device and the input capacitance is seen by the MOS device. Please understand that is no output capacitance still playing a role here, apart from C_{GD}, gate to drain.

So, gate to drain is again multiplied by 1+ GM times R_L'. So, the input capacitance comes from C_{GS}, gate to source and the output side comes from gate to drain and then both get added up together and that gives you the value of your this thing. So, this is your 20 log A of M, this is your mid-frequency gain which you get, at higher frequencies therefore they start to drop. Therefore a common source or a common emitter mode configuration at higher frequencies also shows a drop of 20 dB per decade, which we have already discussed in our previous modules.

And we have seen that this works pretty fine for all the practical purposes. We will come to common emitter, before we come to common emitter, therefore let me explain to you what is known as an open circuit timing, open circuit time constant and explain to you what is known as an open circuit time constant and I will show to you how it works out.

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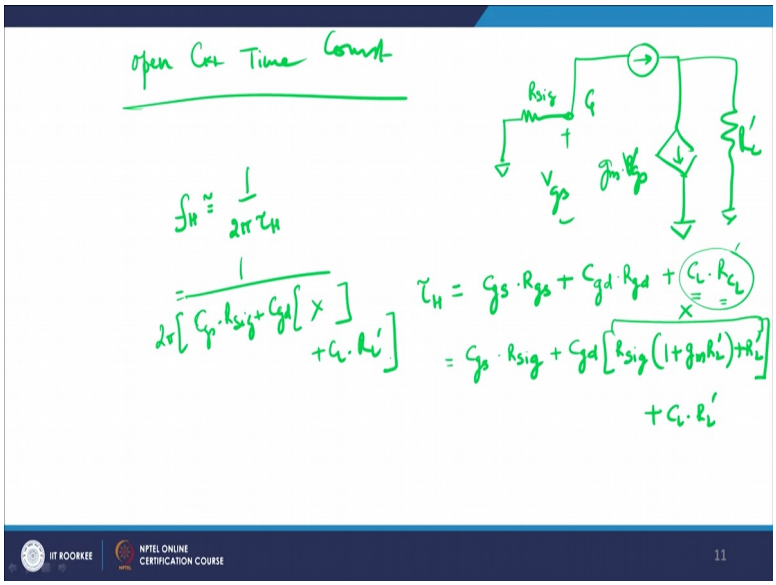

So, let me give you, so I have a signal source here and I have grounded and this goes to get, this is R Sig which you see and then the same thing can be continued and I will have the current source here, current source here, and then this is GM times V_{GS} and then you have got R_L'. This is your current. So, this is your plus minus V_{GS}. Right, so I get from here, if you do small analysis, I am not going to dig it the whole because it is out of scope, I will get the total this thing will be given as C_{GS} multiplied by R_{GS} + C_{GD}, right, let me write down for you, let me just C_{GD} multiplied by R_{GD} + C_L multiplied by RC_L.

So, C_L is the load capacitance multiplied by the resistance offered by the load capacitance in terms of loading. So, if I do a small rearrangement, I get C_{GS} multiplied by R_{Sig} are assuming

that RG is approximately equal to R Sig. And if I do CGD, near, I will get R Sig into 1+ GM times R_L', right + R_L', why because this RL Prime is coming here, right + C_L times RL Prime. So, I will get C_L times R_L' here.

So, if you solve it I get F of H becomes approximately equal to 1 by 2 pi tau_H. So, if you put tau_H tau, I will get this as 1 upon 2 pi C_{GS} multiplied by R_{Sig} + C_{GD} multiplied by this whole quantity, suppose this is X + C_L times R_L'. So, you see that F_H value depends upon the value of your gate to source capacitance, it also depends upon the value of gate to drain but multiplied by 1+ GM R_L because of Miller multiplication factor and it also depends upon the value of an external load voltage which is seen to us. And that gives you a typically nice idea about the open time constant for this case.

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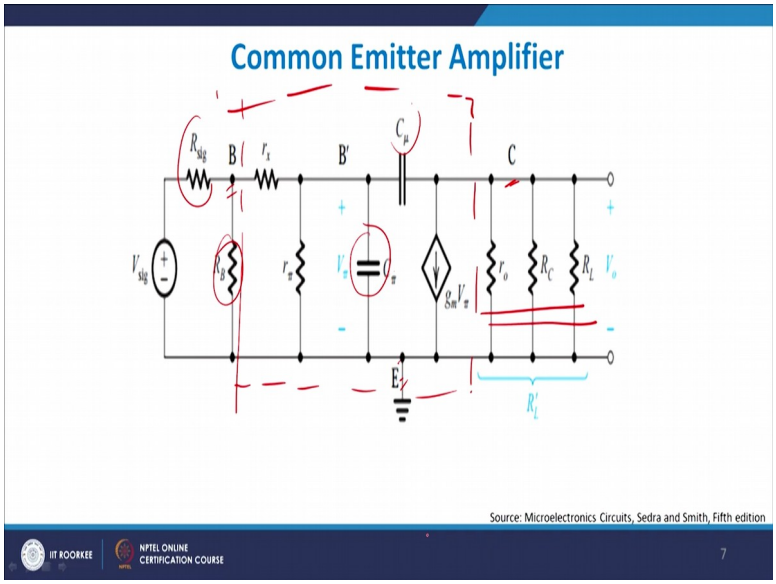

For the case of common emitter mode configuration let me come to common emitter amplifier, we have a BJ T based common emitter amplifier. So, now you have, this is the base, right, this is the collector and this is the emitter. Now, this is your signal, so this is your signal and this is your base resistance which you see, right, R_B. So R_G there is analogous to R_B here and R_0, R_C and R_L are effective load in the output side.

So, this is your actual device, this is the actual device, where this is the base, this is the base terminal, emitter terminal and collected terminal and we have got 2 capacitance here, C_{pi} and C mu, these are basically the capacitances, depletion capacitances between emitter base, collector and base emitter. So, emitter base is C_{pi} and base collector is C_μ. And GM times V_{pi}

is basically the amount of voltage or the current flowing through the bipolar junction transistor, through the BJT, right.

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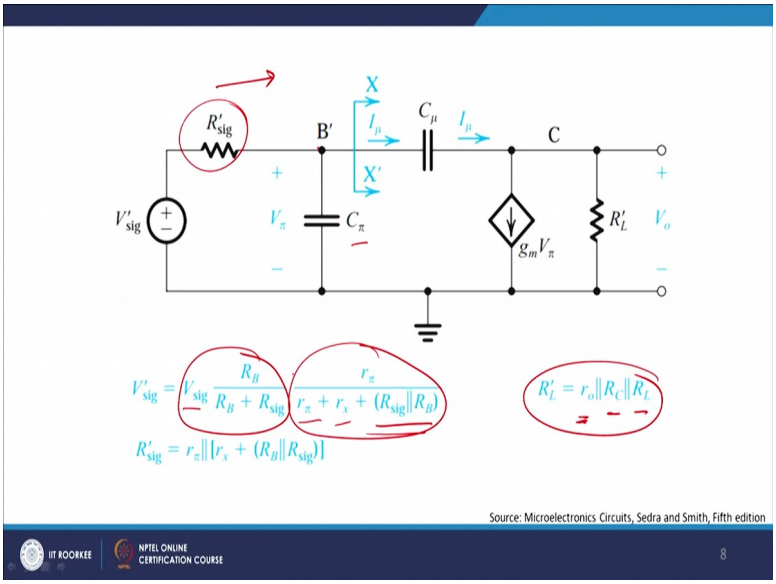

Now, if you solve it, it is exactly the same as the previous case, the only thing here is that you now have, if you look from the left-hand side, which is this one for common emitter base configuration. I get V_{Sig} multiplied by R_B upon R_B+ R_{Sig}. This gives you sort of voltage divider network and gives you effective value of voltage seen from the base side of the common emitter configuration divided into R_{pi} Upon R_{pi} + R_X.

So, this is again a voltage divider network which you see here. R_{Sig} + R_B, which is R_{Sig} is basically is this part, right parallel to R_B, R_B is the base resistance offered by the device and R_{pi} and R_X are nothing but the pi and X values of your emitter, base, collector junction. And R_L is basically R_0 R_C R_L. So, collector resistance, load resistance and the resistance offered by the device itself, right. And that gives you the value of R_{Sig}' and VSig Prime.

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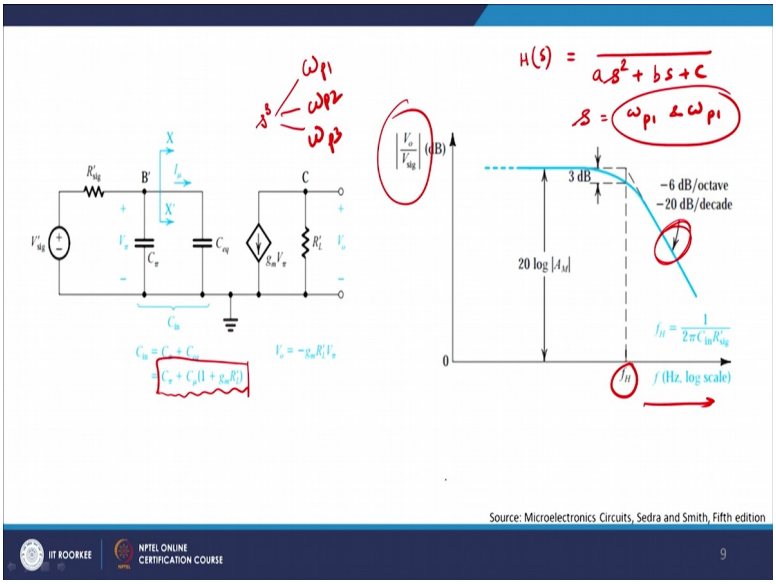

And with this if you plot again, exactly the same thing as your previous case, so common source and common source MOS amplifier and common emitter bipolar transistor, high-frequency looks almost the same, qualitatively as well as most quantitatively. So, if you plot again, therefore gain versus frequency and you see that your cut-off frequency F_H comes out of the again somewhere here, which depends upon the value of C_{in} an R_{Sig}' , right.

And this is again a Miller capacitance which you see, Miller indices, maybe the next module I will just give you a small insight into the Miller capacitances because this is quite an important term which we will be encountering time and again, especially in amplifier circuits. And I might go into the details of this one at a later time, maybe in the next module.

So, I get 20 dB per decade drop here which you see, this gives me a drop which is quite substantial drop in terms of voltage gain. If you therefore see and try to find out one important point which you should know or you should be able to find out is that as I discussed in the starting of the lecture, that typically if you take up a transfer function H(S) and you do have second-order transfer function say $AS^2 + BS + C$ then you typically have 2 poles, omega $_{P1}$ and omega $_{P2}$.

Why, because this is a square term here, so there will be 2 poles are associated with it. Similarly if there is a cubic term in the denominator, you will have 3 poles associated with it omega $_{P1}$, omega $_{P2}$ and omega $_{P3}$, right. So, these poles will depend upon, the placement of

these poles will depend upon the frequency at which they are operating in Sigma G omega plot.

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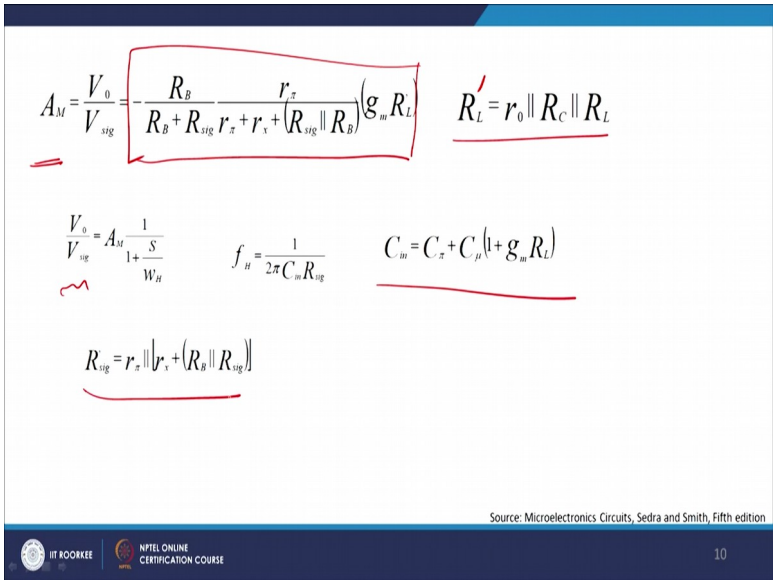

So, same again, I am just repeating the same thing which I did earlier. That I get A_M, the mid-frequency gain is given by this whole quantity multiplied by GM times RL Prime, right, with the negative sign because again here a 180 degrees phase shift, RL, this basically RL Prime, so R_L' will be equal to R_0 in parallel to R_C parallel to R_L. And I get this, again V_0 by V_{Sig} I get C_{in} equal to this much and I get R_{Sig}.

So, I wanted to just give you an idea that if you take MOS-based amplifier in CS configuration or BJT in CE configuration, the behaviour is almost the same qualitatively as well as quantitatively, right. And the primary pole, the first poll or the major poll comes because of C_{in} times R_{Sig}, right. Because of this you will get frequency which is a 3 dB frequency available to me, right.

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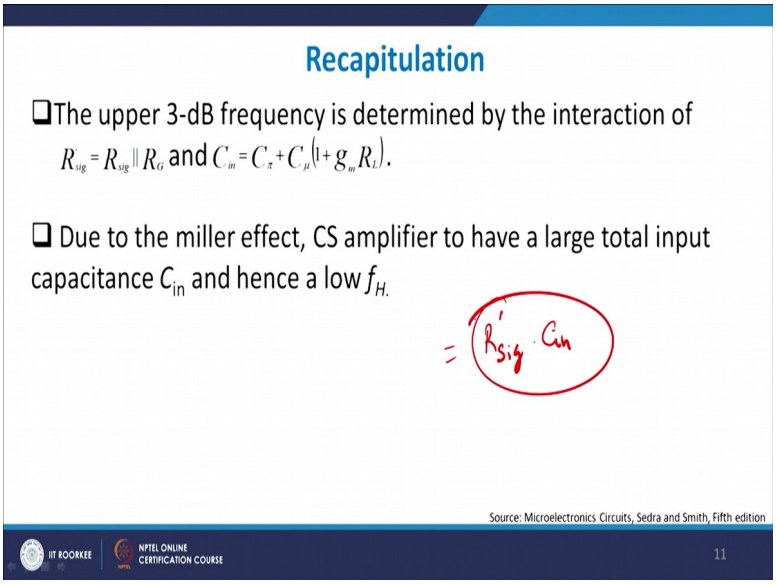

So, let me recapitulate the upper 3 dB frequency is determined by the interaction of as I discussed with you R_{Sig} and C_{in}. As I discussed with you, therefore the typically your 3 dB bandwidth will be, 3 dB cut-off point will be determined by the product of R_{Sig} and C_{in}. So, this will be the product which will determine the F_H value.

Now, one important point which we have also studied this time around is because of Miller effect, we will take up this Miller effect in detail, maybe next module. If we take the Miller effect, then CS amplifier or even BJT shows you an exaggerated value of your output capacitances, which is multiplied by a typically factor of GM times R_L.

So, your effective value increases and that is the problem area. That though you want to increase again by increasing the value of transconductance of the device, you end up having also a larger value of your input, effective value of your input capacitance and therefore, your cut-off frequencies also get reduced drastically and you will not get a large band of constant gain feature.

And that is the problem area which people face as far as this specially with Miller capacitance is concerned. With this we have almost finished with the concept of this thing. Next time when we come back, we will discuss source follower and a part of Miller effect to give you a feeling about what Miller effect is and how does it influence our high-frequency response of CS or CE or source follower amplifier. Okay. Thank you very much.