Microelectronics: Devices to Circuits
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Lecture 39
Multistage Amplifier with SPICE Simulation.

Hello everybody and welcome to the NPTEL online certification course on microelectronics devices to circuits. We start today's module the name of today's module is multistage amplifier with spice simulation. So what we will do in this module of approximately half an hour is, giving you an idea about the structure of a multistage amplifier and then we will look into how to design a spice deck file in order to solve a Multistage Amplifier. And what parameters need to be extracted from the amplifier design. So, let me just recapitulate what we need to do.

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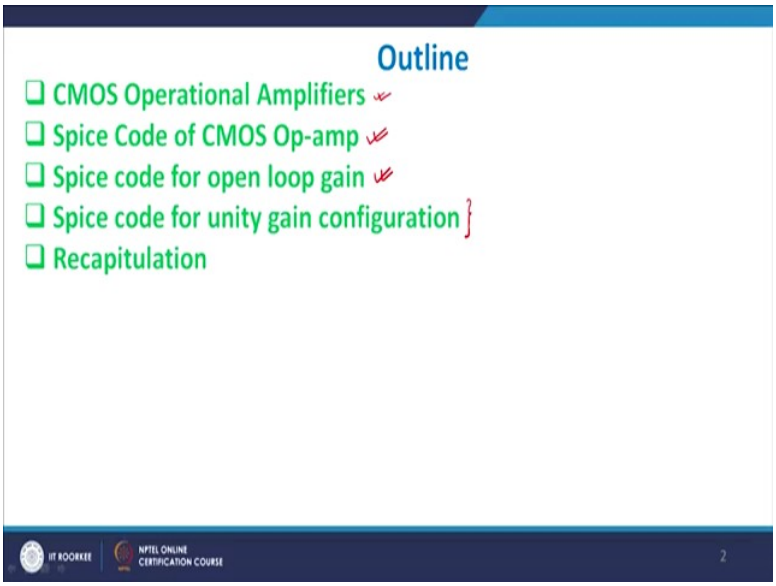

So we will first start with CMOS operational amplifier in the outline of the talk as you can see. And then we will do the spice coding of the CMOS op amp and then we will look into the open loop gain and closed loop gain for operational amplifier and then we will also show you a spice code for unity gain amplifier or unity gain configuration of operational amplifier. Before we go forward therefore let me recapitulate what we did in a previous turn.

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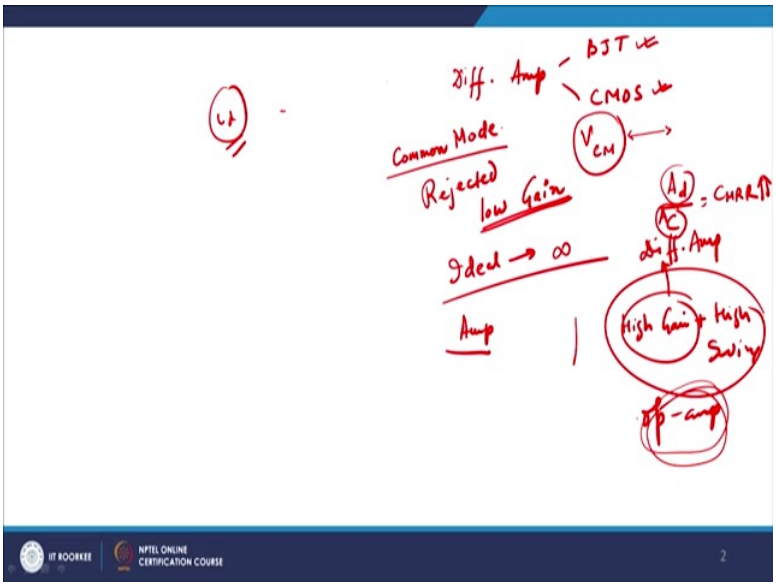

In our previous turn be actually looked into what are known as differential amplifiers, right, both the BJT design as well as CMOS-based design. We also saw that you need to give a common mode signal to both of them initially, so that they are in the active region. And we don't want them to go into saturation region drastically and therefore from active to cut-off and cut off to active should be decision parameter which will be available for BJP as well as for CMOS.

We also saw that common mode signals are, that is a major prime importance of concern, is that all your common mode signals, right? Which is basically noise, for example, common mode signals to board the arms of BJT they get rejected. So all your common mode signals have got very-very low gain, right? And as a result it gets rejected very easily, which means that if you free the noise to both the arms of symmetrically designed differential amplifier the noise will be easily rejected.

Whereas the different signal which we had defined as id or idv as a different signal between the 2 arms of the amplifier they gets amplified drastically. And the ratio which we have already defined earlier differential mode gain divided by common mode game here was referred to as CMRR and this should be as high as possible ideally value is as I discussed with you it should be equal to infinity.

So if you design and operational amplifier or a differential amplifier. Differential amplifier is no doubt the first days of the operational amplifier. So today I'll show you the second stage

of the differential amplifier and I will show how it works out properly as a signal stage op amp. So we will show you the circuit diagram of an operational amplifier when we cascade sort of differential ended operation with a single stage amplifier, right?

We also saw and we also came to the conclusion that whenever you are designing an amplifier, it is always advisable to first of all design an amplifier with let us say high gain, right? And then cascade it with high swing, right? And that is what is basically an op amp, right?

So this will be a differential amplifier dif Amp, so the first age of any operational amplifier is basically a differential amplifier. And the second stage is basically a high swing stage or a high gain stage and that results in basic understanding of the operational amplifier. So this is the basic flow which we have been doing it for quite a long time. And let me therefore come and show it to you the basic diagram of a CMOS operational amplifier.

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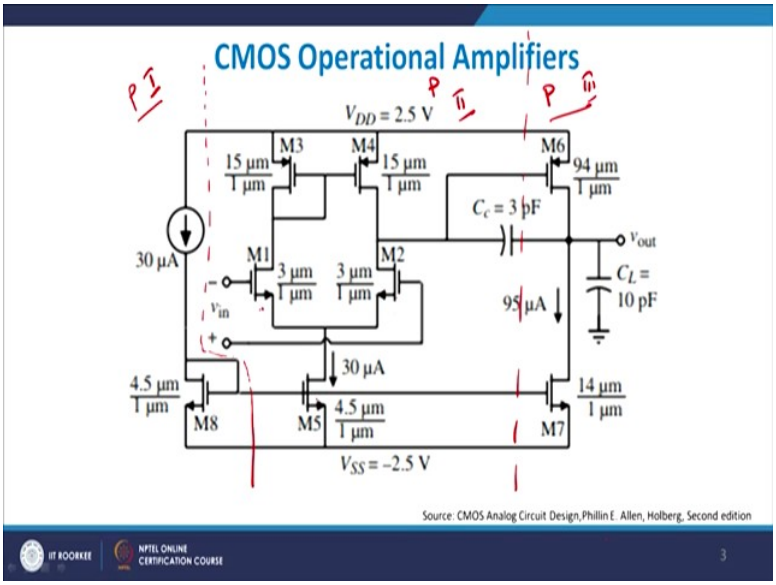

This is the typical diagram of the operational amplifier out of which if you see very carefully, I will just divide the whole thing into few parts, so it is easier for you to gather information for each of them and I am doing it like this. So this is part number 1, right? So this is part number 1, right? And then we have part number 2 here, this is part number 3 and this is part number 2, right?

So you have part 1 here, right? P1 and then you have P2 and you have got P3 here it all respects, you do have your design here. I will first concentrate on P2 and then we will come to P3 and before as we move along. If we look at P2, right? The part 2 which you see here, it

is nothing but differential amplifier with M1 and M2 as input devices and M3 and M4 our basically the cascaded device or the low device and if you look at M5 it is nothing but the current source which is available to you.

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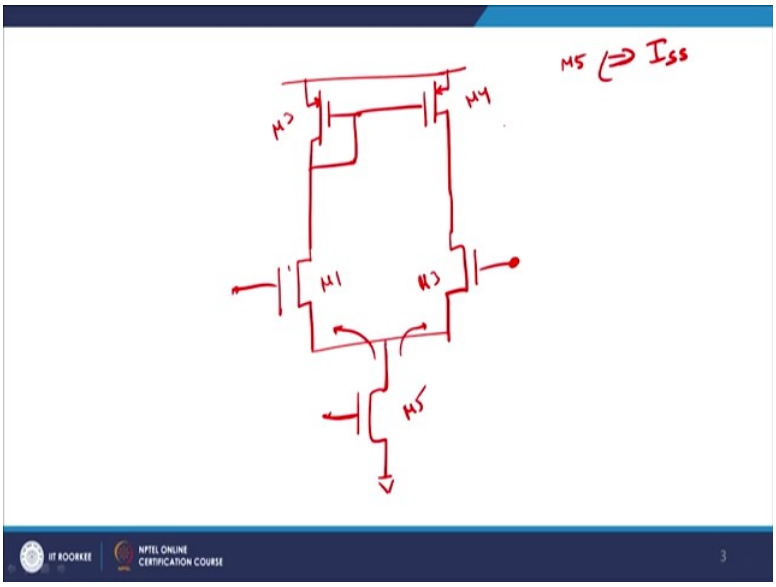

Now, let me draw you this diagram only in a schematic mode. Any will see how it works out. As you can see therefore it will be something like this. This is again CMOS and we are using PMOS load and this PMOS load is, this is mirrored here, so this is current mirrored and then we have got here 1 NMOS driver another and NMOS device here and then we have got this coming out like this, this, this and this.

So, this is M1, M2, M3, M4 and M5, right? So this M5 is primarily the ISS. Which means that this is basically the tail current source, right? And this is responsible for giving the current to both this arm as well as this, right? And you have to make this M5 is analogous to your ISS or the current source.

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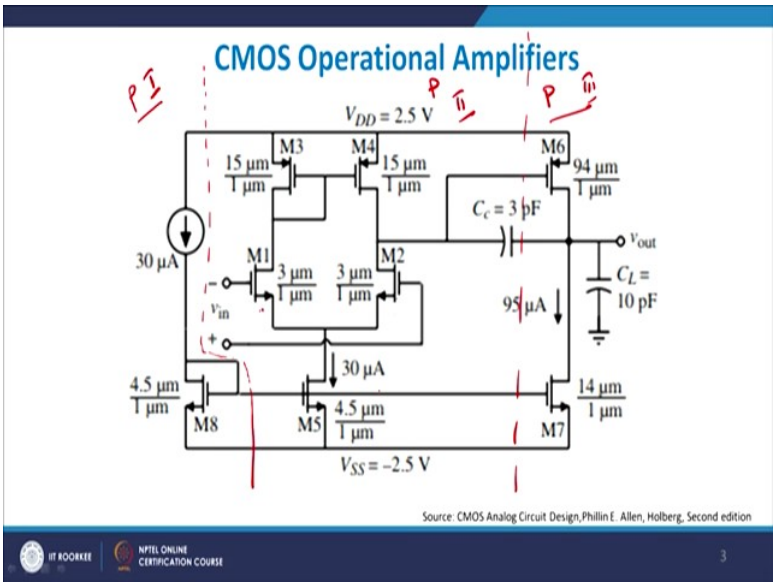

And therefore if you see its aspect ratio is very large, you see 4.5 by 1 micron. So this is design is based on 1 micron technology which means that channel length of all the transistors used here is approximately 1 micron. And the ratio if you look at W by L ratios of M5 is typically very high, right? It is 4.5 micrometer by one micrometer, right? And your VSS is latched to minus 2.5 volts, so it is not grounded here, if you go back.

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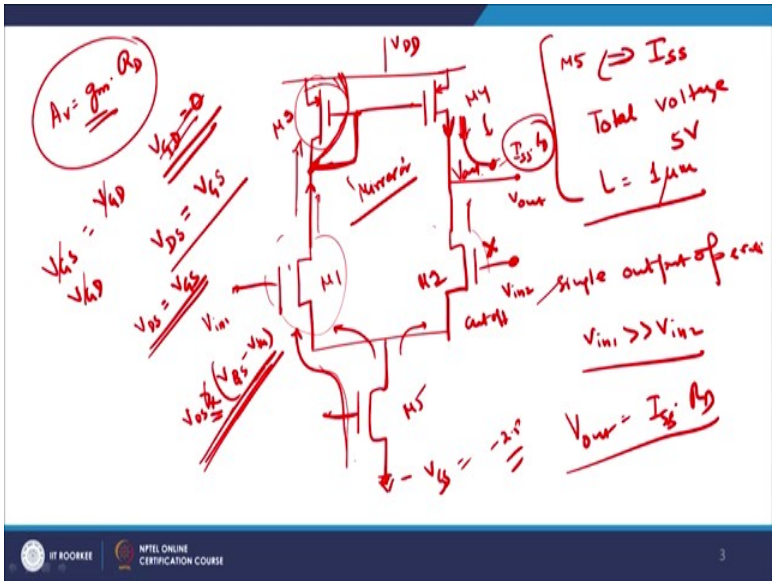

It is not grounded here but this is VDD which is plus 2.5 and we have got minus VSS which is basically minus 2.5 and therefore the total swing, the total voltage available, swing available to me is basically equals to 5 volts, right? And this is L equals to 1 micron

technology which people have been using in this case. I will give you the operation and then we can go step-by-step, one step ahead.

See, if you remember that the gain was given as equals to gm times are RD, right? Where gm was a trans conductance of this M1 and M3. Assuming M1 and M3 are equivalent in nature and also assuming that they have been properly biased in the active region I can safely write down the overall gain to be equals to gm times RD where gm is the trans conductance of this device as well as this device.

And RD is basically the resistance offered by M3 and M4 low devices, right? So that is the reason you typically like to have these PMOS devices because PMOS have got a whole as the charge carriers and therefore, its mobility is low and therefore its current is small which results in a higher resistance. Higher resistance means obviously a higher gain in the output side.

So the output has been taken from this place, if you see very carefully, the output is taken as a single ended output, right? So this is output which you see. So if you look very carefully this is the output here V out. So this is also known as a single output operation. Why single output? Because you're only taking output from the single end they are not taking from the double end, right? So its gain will be approximately half.

Let us see how it works out? Your V in 1 is given here and this is say M1 M2 and this is V in 2 and let us suppose V in 1 is much-much larger sum but to V in 2 and therefore V in 2 is cut off, right? At this stage and all the current flows through this arm and it goes to M3, right? So what am trying to say is that V in 1 is typically very large much larger than a threshold voltage of M1.

Therefore, what it does is, it carries all the current through M5, M1 on to M3. Now in M3 your gate and drain our short head. So your V_{GD} is equals to 0. Gate to drain is always equals to 0. Which means that V_{GS} gate to source this to this, right? Is this one and gate to drain are both equal to each other, so V_{GS} equals to V_{CD}, right? V_{GS} gate to source is equals to gate to drain, right?

Because Gate to drain is actually equals to 0, gate to drain equals to 0. I will just make some small corrections here. See here is that your drain voltage and your gate voltage are equal, so V_G and V_D are equal. So if you put source here V_{DS}, right? And you put V_{GS}, so they are

always equal. So your drain to source voltage is always equal to gate to source voltage implying that the device is always into saturation region of operation.

Because if you remember the region of operation was VDA should be greater than equals to V_{GS} minus V_{TH}, right? That was what was told to you, it should be less than or equal to. For PMOS it should be less than equal to but since it is always equal to therefore this will always be in saturated state.

So they will always behave like a resistor if you shot this thing gate to drain, if you short the gate to drain. Further you also ensure that this potential, M4 gate potential is exactly equal to the drain potential of M3, right? And therefore this is sort of replica here, so all the current which is flowing from here the exactly same current will be flowing through this arm, right? This is known as the mirroring action in analog design.

This is known as mirroring action at the result, if you remember for the current to be saved in 2 arms of a 2 identical MOSFET gate to source voltage should be equal first of all threshold voltage should also be equal. And you also have to ensure that if it is in the priorities of operation the drain to source voltage should also be equal, right? So all these 3 are ensure to be equal for both M3 and M4, if you simply shot gate and source of M3, right?

And as a result the same current is flowing from this are exactly the same current flows through this arm and goes to V out because this is cut off, so the same current flows through V_{out}, right? And therefore whatever current was flowing through this ISS is coming out here this multiplied by R_D is V_{out} so therefore you get V_{out} to be equals to I_{SS} times R_D in a general sense.

And as a result that is the voltage drop which you see as equals to V out, right? And that is what is V_{out} is all about. So now if you go on increasing the value of your M2 gate voltage and lowering your V in 1 then part of I_{SS} will be transferred to M2 and therefore you will automatically, so this will be less than I_{SS} and this will be slightly greater than 0 and if you add, sum of them will always be equal to I_{SS}, total current source.

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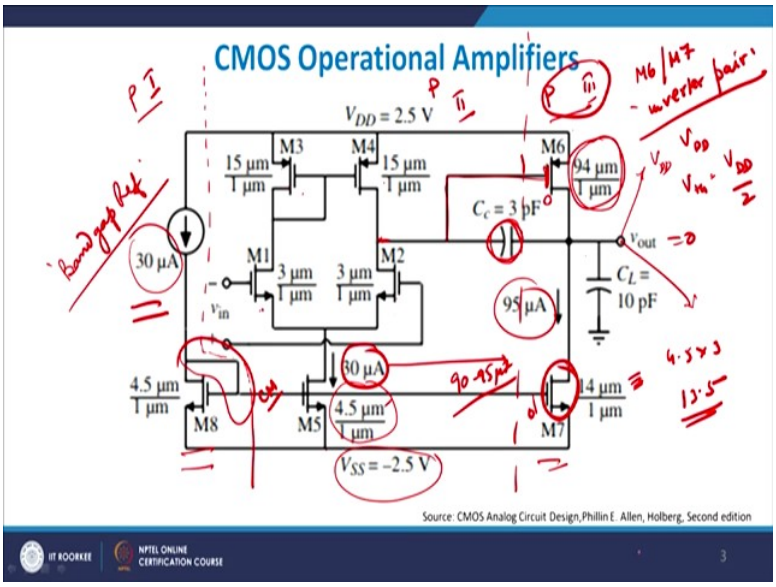

Now that is the general scheme of things which you see now. You do have a capacitor here which is basically a role of a blocking capacitor because it does not let any DC component to pass through it and reach to this particular point it only reads the A/C component to pass through it because you don't want any DC component to load your subsequent stage. The subsequent stage now is basically your P3, right?

We are finished with P2, this is P2 which we have done, so this M3 was mirroring with M4 and the current was going through this point as a result it is going through the same current multiplied by RD is the voltage here, voltage appears across the PMOS here, right? Now if you look very carefully this is basically a pseudo NMOS inverter and therefore part 3 is basically a high swing stage.

I will give you an example why? Say for example, if you look very carefully M6 & M7 forms an inverter, right? Forms an inverter pair which results in what? Which results in the fact that if you're using a V_{DD} here then switching threshold will be approximately equals to V_{DD} by 2, so if the voltage here just crosses V_{DD} by 2 this will ensure V_{out} to go to latch to V_{DD} and then it is just below V_{DD} this will ensure it goes to some other voltage.

You see you are feeding to the gate and of my device, right? So when this voltage is 0, this is on and therefore this output voltage is latched to V_{DD} and the V_{out} goes to 0. When this goes to one and this goes to, say this is one that this goes to 0 and therefore this output goes to 0

when this M7 is 1, right? And as a result you will have a large amount of current flowing through this particular point.

You see M6 has been made very-very large and I mentioned, right? This is to ensure that your typical resistances are small and voltage across this is very-very small and it really get high-end V_{DD} full swing available to you in the output state. Who drives M7 ? It is being driven by this M8. Look at the fact that this M8 it is M7 and you have a current source 30 micron ampere this is also referred to as band gap reference we will discuss that particular point.

Assume that band gap Reference is basically current source which is basically temperature independent and it is a very fixed current source which is given to operation amplifier the same current source is getting replicated at every other point, so if this is 30, this is also 30 because you have a current mirroring action here, this is your CM current mirroring action here and as a result you have 30 microamperes here and approximately the same here provided but it is approximately 2.5 times, this is 4.5 and this is 14, right?

And therefore, what you will see, you expect to see a large increase in the current here and that the reason you see this to be as equals to 90 microamperes the reason being this approximately 3 times which you see, right? Now, for example, 4.5 into 3 if you do I get 13.5 which is approximately 14 micron which means 30 microamperes will appear as 90 to 95 microamperes at this particular point and that the reason you see a large amount of current flowing through here. This is the general structure of a CMOS operational amplifier,

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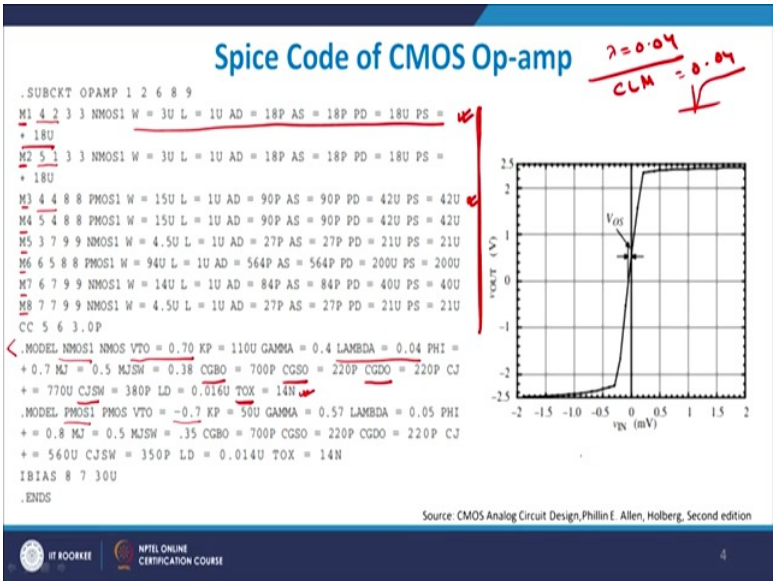

Let me come to the spice code of a CMOS operational amplifier. Spice code is basically a code written in spice language. We will come to spice we will have one module on spice later on but at this stage the circuit in front of you gives you an basic idea about the sub circuit of the operational amplifier and you can see here basically M1, M2, M3, M4 are the entities which you are naming here and these are basically the transistors which are being named here.

And these are the nodes across which they are connected to each other. So 4, 2, 5, 1 and so on and so forth. This is width, this is length, this is the area of drain, area of the source then you have got the parameter of the drain and parameter of the source. These are the 5 quantities which are written for each one of them and these are basically process dependent parameters which are inserted onto the system by the spice module developer.

So you do have certain sub circuits for all of them and you have large number of, for all the devices we first of all defined its structure and how it looks like and across which to nodes they are connected then we define a dot model file which gave you an idea about the type of device it is. For example VT0 is basically the threshold voltage of NMOS is been taken to be equals to 0.70 voltage, right?

0.7 volt is the threshold voltage of NMOS into consideration. We are also assuming this is not an ideal current source but a non-ideal current source with lambda equals to 0.04, so this is 0.04 primarily meaning that CLM parameter is basically 0.04 and therefore when you got a graph it will be something like this. It will not be exactly the straight line across Y axis. Similarly this is the capacitance of gate to bulk, gate to source and gate to drain in Pico farads, right?

We have junction capacitances here and we have got oxide thickness as 14 nanometers and so on and so forth. So these are the model files for NMOS 1 and these are the model files for PMOS 1. So PMOS one is exactly minus 0.07, so therefore fairly symmetrical with respect to each other but everything else almost remains the same, right? And this is how you write your spice code file for the CMOS operational amplifier.

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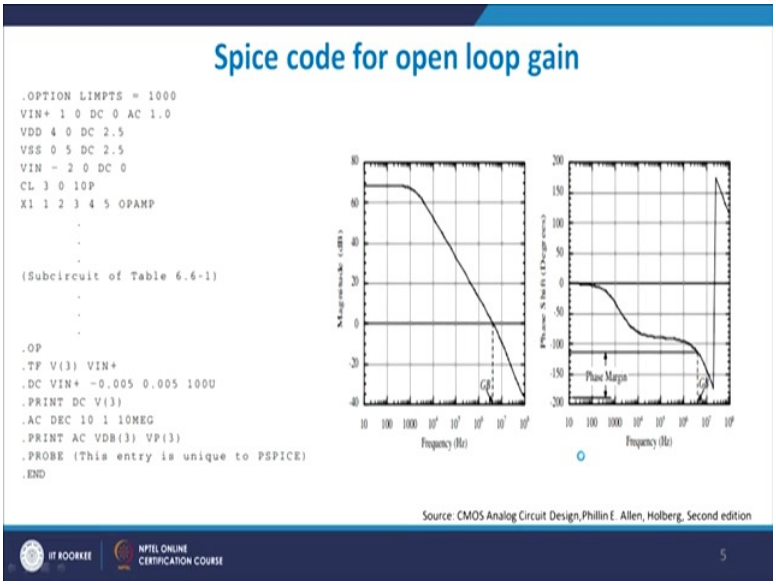

Now when you want to find out the open loop gain, right?

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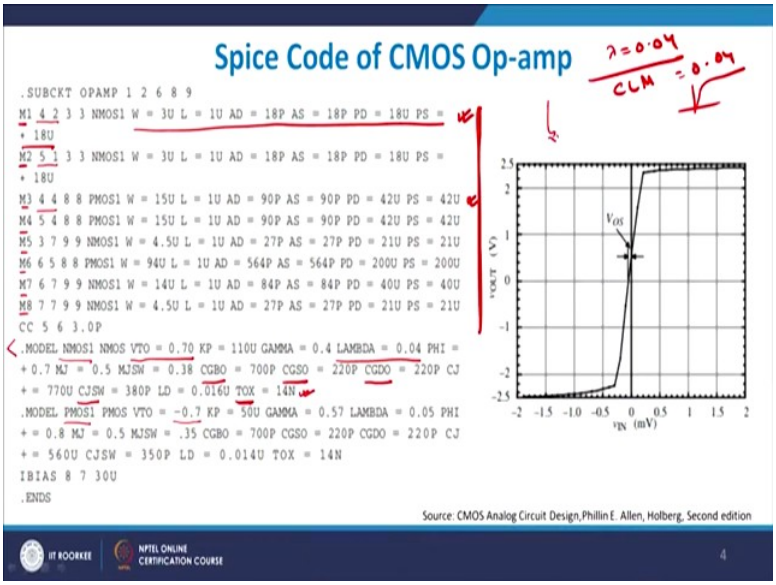

So, let me come back to this point basically if you look at graph here this is V out versus V in which is basically also referred to as VTC, so this is basically the VTC often operational amplifier. So you give an input swing from minus 0.2 to plus 0.2, right?

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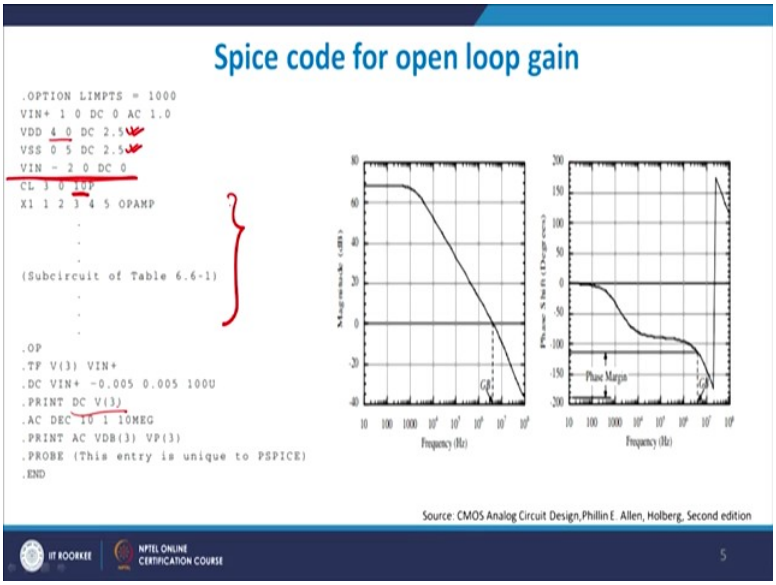

And that's what is given here. So if you see at V_{in}, if you look at V_{in} then you see that I am giving VSS to be equals to 2.5, right? It cannot be between node 4 and 0 and DC bias and V_{DD} is 2.5 which am giving here V_{in} is going from minus 2 volts, right? Minus 2 volts to 0 volts, right? And I'm able to get the picture here then I define load capacitance as 10 Pico farad between note 3 and 0 and so on and so forth. So what happens is that, you just read the circuit here and then you try to find out the value of the DC bias or the DC output bias at this particular point.

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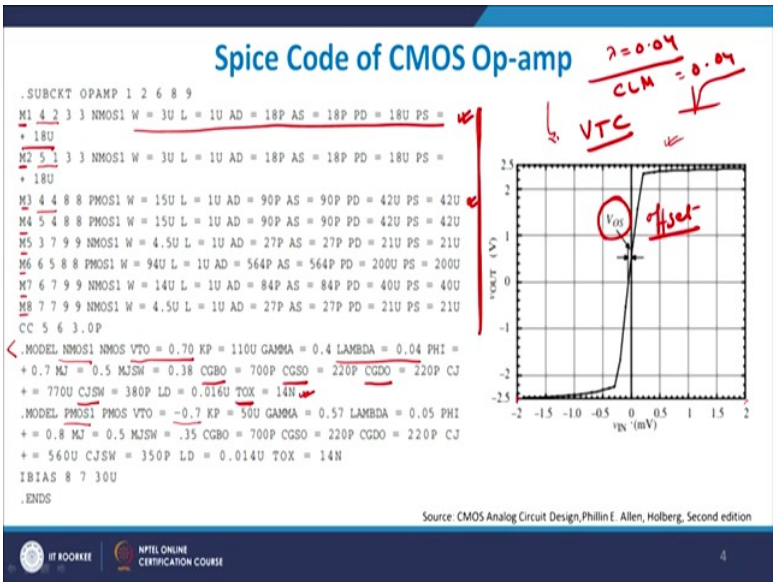

Then what you get from this discussion is that you try to find out V_{out} versus Vin which means that you give a sweep of V_{in} for every value of V_{in} you try to find out the V_{out} and as

expected the VTC looks something like this which is shown in front of you, so when V_{in} is very-very low the output is 0, right? And it is very-very low when V_{in} is very-very high one of the V_{in} is very-very high you get output to be very high, right?

And this is we have already discussed this point in our earlier discussions of differential amplifier. But remember that when V_{in} equals to 0 the difference between them should be equal to 0 then output also should be equal to 0 but in reality not true. So therefore you always have an offset with you, that the reason I write here V_{OS}.

V_{OS} basically the offset. This is basically your offset. Voltage offset at corresponding to Vin equals to 0, right? This offset does what? You have to subtract this offset later on into your system. If it's a positive offset you need to subtract it from the output and if it is a negative offset you need to add it to the output to get the achievable signal.

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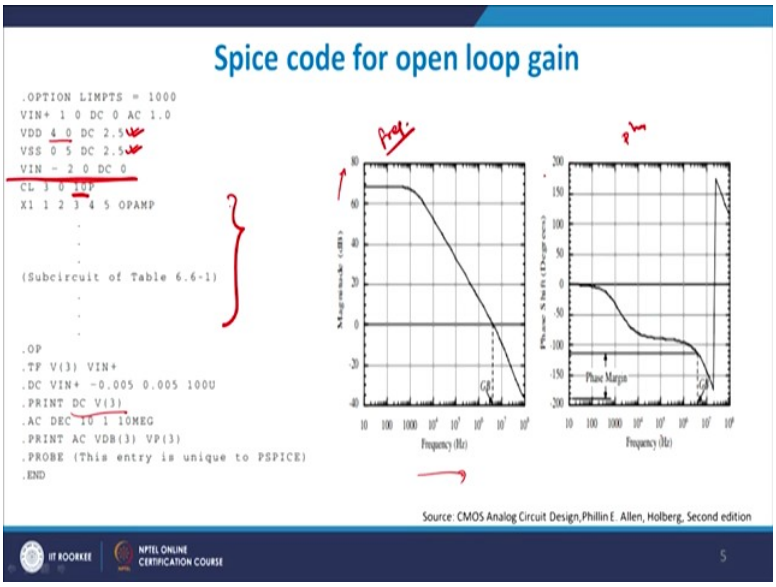

So we plot a magnitude which is basically gain versus frequency. So this is your frequency spectrum which you do, right? And then you also plot phase versus frequency also using spice code.

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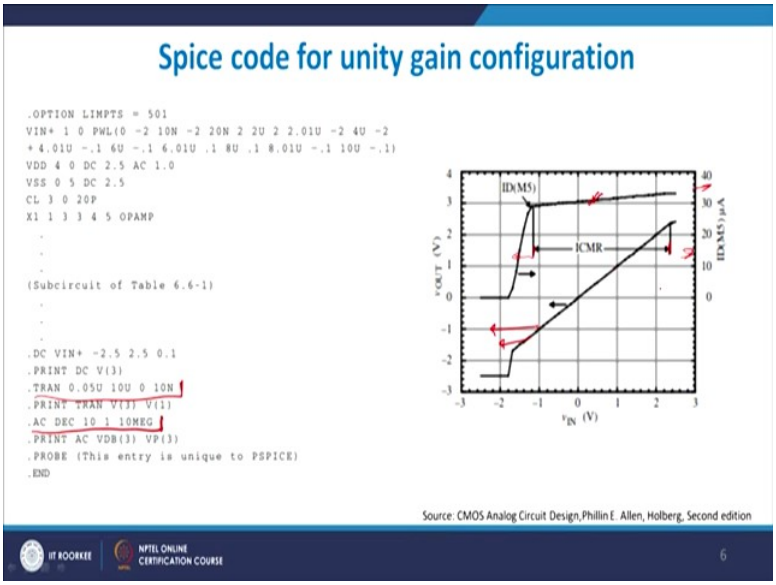

If you want to do it for unity gain configuration. Unity gain basically means that you just short the input and output, right? So you have a unity gain feedback loop and therefore that gives you a unity gain output. You get a V_{DD} as I have discussed with you again V_{DD} but here we use dot AC because you are giving an AC cycle and across the 10 mega ohm resistance you are trying to do it and then you are trying to find out the transient value of the voltages at every particular point.

So, when I find out V_{out} versus V_{in} I see that, this is basically your I_D which is basically on this side and this one is on this side, right? So, I see that this is basically my ICMR from this part to this part is my ICMR input common mode range, right? And anything lower than this you force the device to be into the deep linear region and if anything greater than this you allow it to be going to saturation region, right? And this is the spice code for the unity gain buffer which you see.

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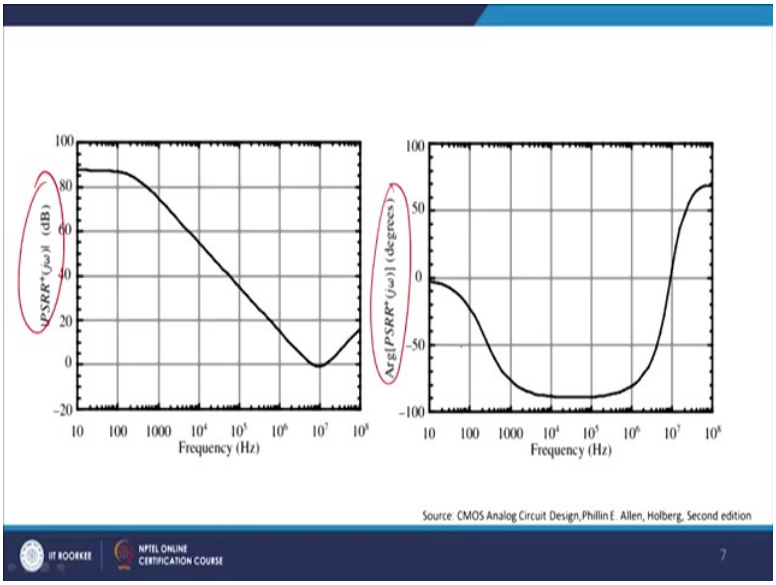

Then we plot the same plot for PSRR and for your phase of PSRR this is power supply rejection ratio, we will come to this later on but very important part is that this power supply rejection ratio is basically the capability of the operation amplifier to remove noise from the power supply. And as we can see at lower frequencies the gain is typically very high it can remove very well but as the frequency goes on increasing there is a drop in the output in this case. Similarly, for low frequency we get the same thing.

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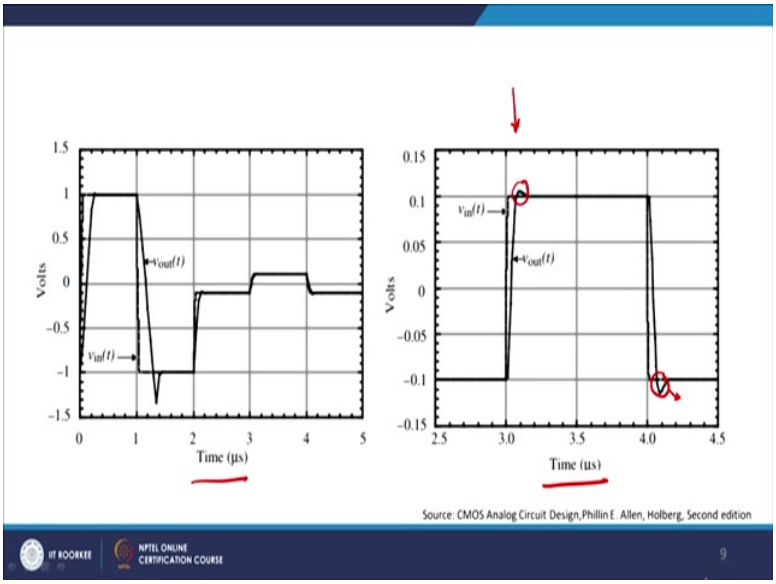

We come to the last part and that is basically transient analysis and we see that for various different time analysis, how a timing analysis? How we get the output voltage with us and the methodology adopted here is that again we do a transient analysis. So rather than doing a DC

analysis and we do a transient analysis. In the transient analysis for a very short duration of time we try to find out the output voltage changes because of the change in input voltage.

And you will see that when my V_{in} rises my V_{out} also rises, this diagram. But it arises with certain extra delay which is expected also because that is basically the delay of the inverter itself. Not only that but one important point is that you see a small hump here and a small hump here. This hump is basically to do with the clock feed through which means that because of very fast changing output there is a capacitive coupling between the output and the V_{DD} and as a result you will certainly see a small hump in the output.

Same thing happens in the lower transition when the output goes below particular point which is minus 0.1. So even if you are V_{DD} is 0.1 to minus 0.1 for a very short duration of time the output voltage can actually exceed 0.1 and go below minus 0.1, right? And that is because of the fact that you do have a capacity of coupling between the input and output which results in a sort of clock feed through mechanism in this case, right? And this results in a larger change.

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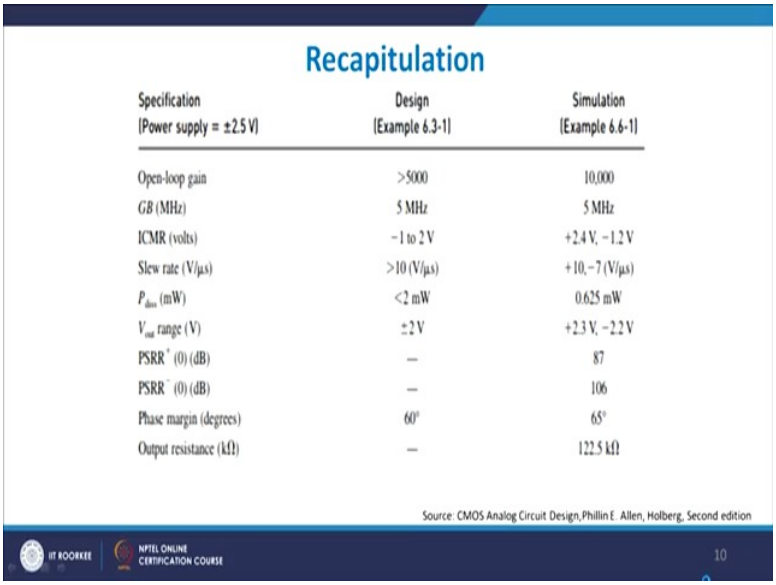

Let me therefore recapitulate to you and show you overall picture of the operational amplifier which we have designed till now. This example, we have taken it from a standard operating manual. And we have found out that two-stage op amp your typical design we have taken out to be 5000. The same design principles if we put it on a spice profile we get approximately 10,000 as my simulation output.

This is the gain bandwidth product of 5 megahertz and we also get 5 megahertz here. ICMR is minus 1 to 2 worlds and it is plus 2.4 to minus 1.2 volts, so it is almost the same thing. The slew rate are also equivalent. The power dissipation is typically very small. My output range is plus minus 2 volts for design. I was planning for plus 1 volt to minus 1 world variation in output, right?

PSRR and phase noise margins and output resistances are also within the domain which is available to us. Now, the idea here was that to just give you a brief inside into spice, right, and how you can use the spice for multistage operational amplifier calculation. They will also come back to this spice module in details in maybe about 6 to 7 modules later when we discuss spice.

Then again I would recommend that you come back to this module once again, right? So that once you study the spice properly you can come back once again to this spice module for multistage amplifier, right? How to write a net least? How to write a schematic entry in a spice?

All will be told to you in subsequent modules but at this stage I just showed to you that it is possible using simple spice tool to actually extract the values of gain, bandwidth, CMMR, Slew rate, PSSR, open loop gain bandwidth product for a simple two-stage operational amplifier. So what we discussed here was basically your two-stage operational amplifier only.

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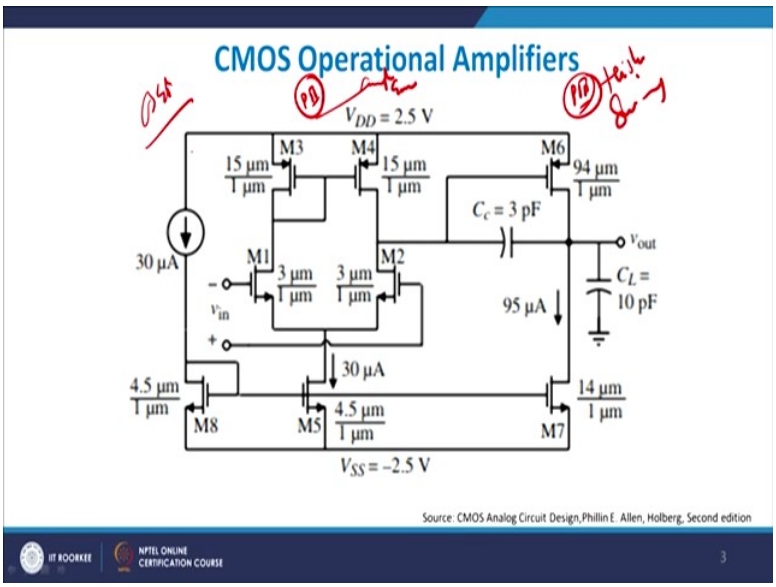

If you look very carefully here what we discussed was basically a two-stage operational amplifier. And as you can see here this two-stage operational amplifier was working because of 2 main reasons that you had part 2 which is basically, primarily the differential amplifier part which gives you a very high gain part and you have got part 3 which helps you to give you high swing part, right?

So you have an inverter which actually therefore pulls your output voltage directly to V_{DD} up or it goes down to V_{SS} at a bottom low. So part 3 which is basically this one helps you to go for high swings, right? High swings and this is high gain. This is your band gap reference which you see BGR and this is your V_{SS} which is minus 2.5 volts supply which you give at this stage, right?

So what we did in this half an hour module was to give you an idea about the working principles of a two-stage operational amplifier where the first stage is differential and the second one is high swing rate. We also saw the spice coding how to do it, a methodology adopted.

We will revert back to this module once again when once you finish spice module later on and then we recapitulate it by doing comparison between a simulation results and the spice results, right? Simulation spice results and handwork results together. And we saw they are very close to each other at certain point of time. I thank you for your patient hearing, thanks once again.