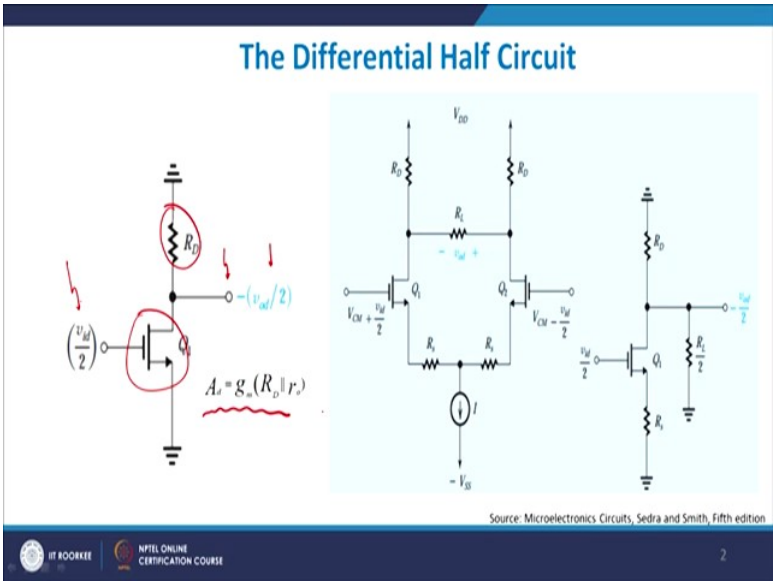
Microelectronics: Devices to Circuits
Professor Sudeb Dasgupta
Department of Electronics and Communication Engineering
Indian Institute of Technology Roorkee
Lecture 38
Small Signal Operation and Differential Amplifiers - 2

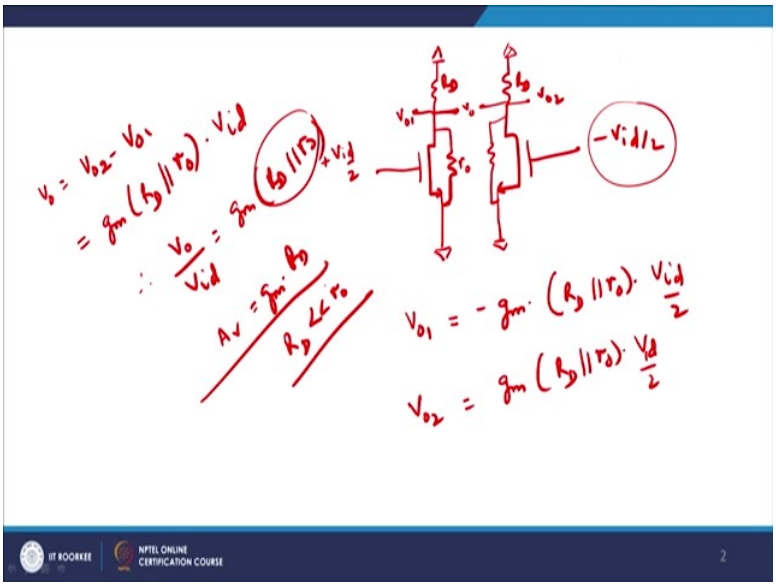
Hello and welcome to the NPTEL online certification course on Microelectronics Devices and Circuits. In our previous module we had seen the basic concept of MOS based differential amplifier. We have also seen the concept of half circuit as applied to MOS-based differential amplifiers and we saw the advantage that a MOS-based differential circuit will have mathematically advantage because once we are able to find out the voltage at a particular point, for a particular bridge the opposite of that will be applied to another bridge and therefore we can easily calculate the overall gain. So, what we will do now is, we will just continue from where we left in our previous discussion.

(Refer Slide Time: 1:25)



And we saw that this is the differential, so you see this is basically your half circuit which is in front of you, differential half circuit which I was discussing with you that you do have a Q1 which is basically your MOS transistor here and I apply a voltage V_{id} by 2 where V_{id} is basically the input voltage difference and R_D is resistance offered. And we get minus V_{od} by 2 is the output voltage with the negative sign because it is 180 degree phase shift. In such a scenario the overall gain is given as gm times R_D parallel to ro, right?

(Refer Slide Time: 1:55)

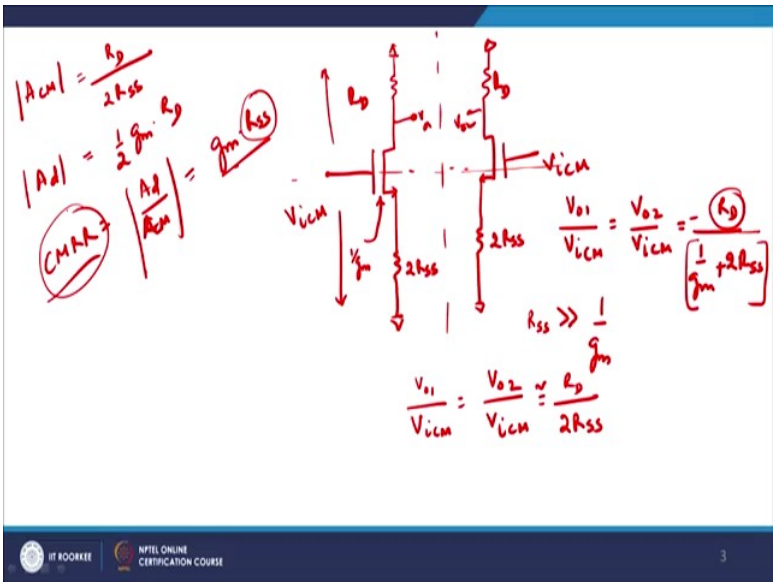


And let me show you how this works out. If I have got to circuits here, right? And they are primarily given like this and this is plus V_{id} by 2, this is R_D and then this is again the same here. So there are 2 half circuits which is here and then this is the series resistance of the device itself, so this is Ro, this is R_D and this is again V0 output voltage which we are trying to find out and this is minus V_{id} by 2.

So, you see V_{01} which is this one, this is the output V_{01}, right? And this is V_{02}. So V_{01} if you want to find out will be minus gm times R_D parallel to ro multiplied by V_{id} by 2. Similarly, V_{o2} will be equals to g_m times R_D parallel to r_o into V_{id} by 2, so it would have been minus but since there is a minus sign already available into the input signal, minus and minus becomes plus and I get this into consideration.

Therefore, output voltage V_o will be equal to V_{o2} minus V_{o1} and this comes out to be equals to gm times R_D parallel to r_o multiplied by V_{id} and therefore, Vo output by V_{id} is nothing but gm times R_D parallel to r_o. Now, of course, as you very well know that my R_D will be, r_o is much much larger as compared to R_D and therefore, for all practical purposes the gain will be equal to gm times R_D. In reality this gm R_D parallel ro which is this parallel resistance which you see because we have assumed all we know that R_D is much smaller as compared to r_o, right? And we get that into consideration for all practical purposes.

(Refer Slide Time: 4:13)



Now with this knowledge and we therefore see that, now let me put the same concept. It will do the same concept here and explain to you that for a common mode signal for example. For a common more signal let say what happens. For a common mode signal I need to find out CMRR now and therefore what I will do is, I will just take 2 R_{SS}.

This is with the current source, tail current source, remember. So I have divided into R_{SS} by 2 because when you take in parallel this 1 by 2 R_{SS} will give you just R_{SS} as the output voltage because they are in parallel with respect to each other. So assume that I have given V_{iCM} here, I have also given V_{iCM} here. This is R_D and then I have put across this concept here and we will try to find out the output voltage here.

So this is V_{01} and this is V_{02}. If you want to find out the output voltage, so this is basically my half circuit here, so why is it R_{SS} by 2? Because we have divided it into 2 parts and we got R_{SS} by 2 as the overall signal. So, if I find out V_{01} by V_{iCM} this will be equal to V_{02} by V_{iCM} will be equal to minus R_D upon 1 by g_m times 2* R_{SS}, why?

Because you remember in one of our previous discussions we had seen that if you want to find out the gain or the output voltage gain just by inspection then you just have to do one thing that you divide the whole thing into 2 such that somewhere in the middle, the device is in the middle and this is the output profile and this is your grounded profile.

So, when you go from the side you just check out how much amount of resistance is being offered in the line below. Below this dotted line it is 1 by gm because when you look from

the source side into the MOS device the resistance offered is 1 by g_m and series side is $2R_{SS}$. So, the denominator is therefore 1 by g_m plus 2 R_{SS} and from top if you come, from V_{DD} which is grounded here I get R_D as the output.

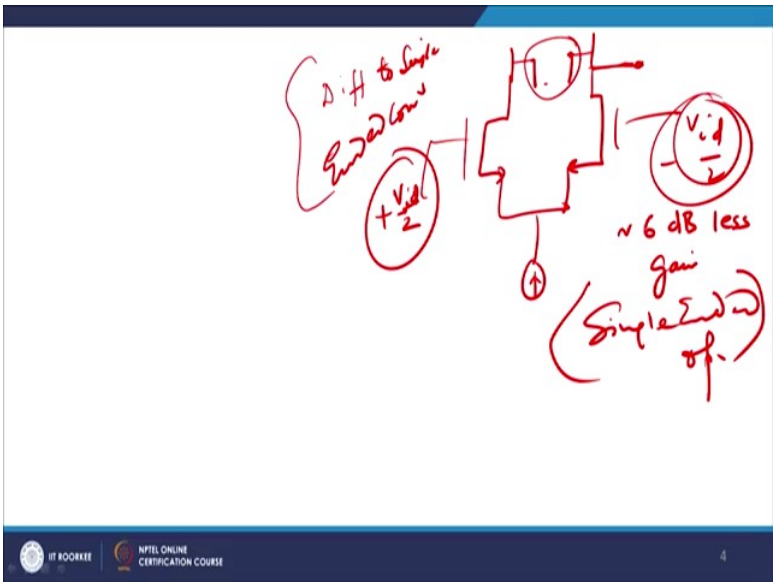
So I get minus R_D upon 1 by gm plus 2 R_{SS} as my value. We already know that R_{SS} is much-much larger as compared to 1 by g_m and therefore I can safely write down V_{01} by V_{iCM} equals to V_{02} by V_{iCM} this is the common mode signal to be equal to R_D upon, right? 2 times R_{SS} because gm is much smaller and I can neglect that value here and I get R_D by 2 R_{SS} as my overall picture.

So, let me find out common mode gain therefore and make it mod. I get R_D upon 2 R_{SS} and I get A_D which is the differential mode gain to be equals to 1 by 2 g_m times R_D, why 1 by 2? Because now you see I am trying to find out for a single circuit. So that the reason this is not g_mR_D it is g_mR_D by 2. If you want a differential you multiply it by 2 and I get g_m R_D, right?

And therefore I get CMRR which is common mode rejection ratio to be equals to mod (A_D by A_{CM}) of that and if you try to find out this overall picture I get g_m times R_{SS}. And since RSS is relatively very-very high because you are using tail current source which is assumed to be an ideal current source R_{SS} value is very-very high and therefore CMRR happens to be very high 10 to the power 5, 10 to the power 6 orders of magnitude.

So, with this knowledge what we have understood therefore is that if we do have a differential or a common mode signal. The common mode signal will give you a large value of CMRR. Now, let me just give you a brief inside into one important point which needs to be looked into. Let me see maybe I can explain to you in this case, right?

(Refer Slide Time: 8:18)

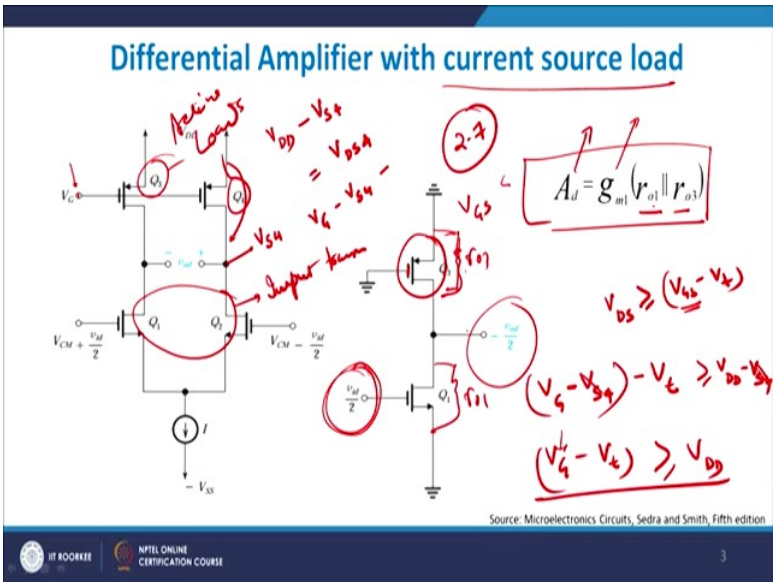


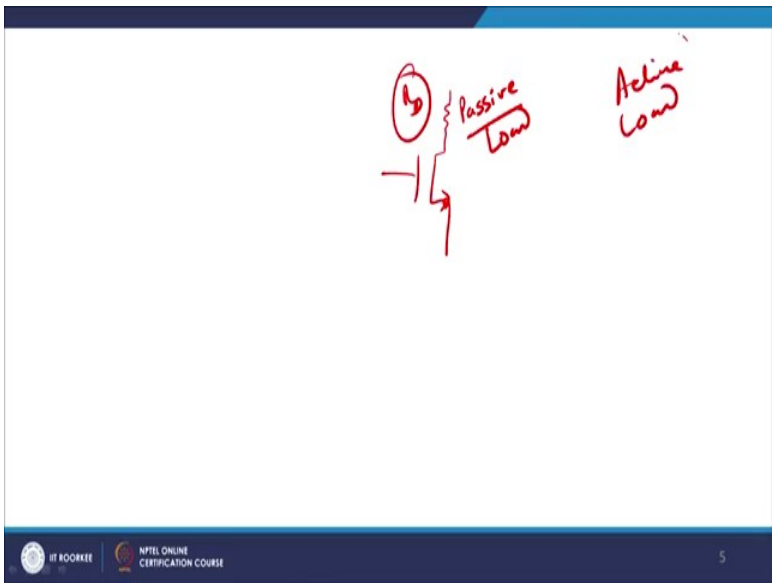
What we were doing is, that they were actually looking into 2 important fact that whenever you do have, let us suppose I have a device and we have another device here and then we have current source which is here. So rather than taking differential output, we can also take a single ended output then your gain falls by 2 but you get a differential, you get a single ended, this is known as a differential to single ended output converter.

So from a differential input and you will get differential input here minus V_{id} by 2 plus V_{id} by 2, right? And I am giving this and this, right? And am trying to find out if it would have been purely differential I would have found out here but no, I am only interested in single ended output, I get this. So you will see that and you can do it yourself by issuing small manipulation and small derivation that this primarily will be giving you twice lesser gain approximately 6 dB less gain will be there, if you do a single ended operation, right?

If you do a single ended operation you will get 6 dB less gain in a more so in a different manner. And second cost you pay for it is, of course, your common mode rejection is not very good, right? So, this is one of the problem areas which people faced when we were doing a differential amplifier, the single ended amplifier.

(Refer Slide Time: 10:12) 10:44





With this knowledge let me therefore explain to you the various other factors that, when we do a differential amplifier with the current source, so what happened was, with this large gain, it also rejects noise as we discussed common mode signals. But if you go back to your previous discussions and understandings you will see that we did have a R_D here, remember. We had a R_D here so, I have a R_D here.

Now this R_D is generally realized, so these are known as Passive loads because you're putting a resistance here, right? We also have what is known as an active load. Active load means a MOS device acting as a register that is known as an active load. So most of the time but we

try to do is, we try to insert in place of R_D which is a passive load because it has high power dissipation we try to insert an active load, right?

And this is one of the examples of the active load which you see. So also known as a current source load an active load. So what I do is, I give a gate voltage here and these are basically your P MOS device, so these are N MOS and these are P MOS devices, right? And if you give a gate voltage here such that it is lower of threshold voltage of the device, switches it on keeps in the triode region and starts working as a diode.

So what is the V_{DS} value here? The difference between V_{DS} value is, threshold is connected to V_{DD}, if we talk of Q4 then V_{DD} minus let us suppose this is, let me say source, V_{source} of 4. So, I get V_{DD} minus V_S of 4 is nothing but V_{DS} of 4, drain to source of 4, right? And therefore, gate is V_G and minus V_{S4}, this is gate to source voltage because, if you subtract this because you remember, what was the condition V_{DS} should be greater than equal to V_{GS} for an NMOS, right? And should be less than equals to V_{GS} minus V_t for PMOS.

So if you find out V_{GS}? V_{GS} is gate to source is V_G minus V_{S4} is gate to source, right? So this is your gate to source minus threshold voltage of the MOS device which is Q4, right? And this should be greater than equal to V_{DS} which is nothing but V_{DD} minus V_{S4}, right? If, you look very carefully these 2 will get cancelled out V_{S4} V_{S4}. I get V_G minus V_t should be greater than V_{DD} for this device to be staying in saturation, right?

So once you are able to sustain a large value of V_G, so if your V_{DD} say 2 volts and threshold voltage of these devices are 0.7 then you have to at least gave 2.7 voltage at the gate side to make them behave as ON state devices and they will be acting as resistors here, right? So these are active load devices also which are there with us. So this is what we get.

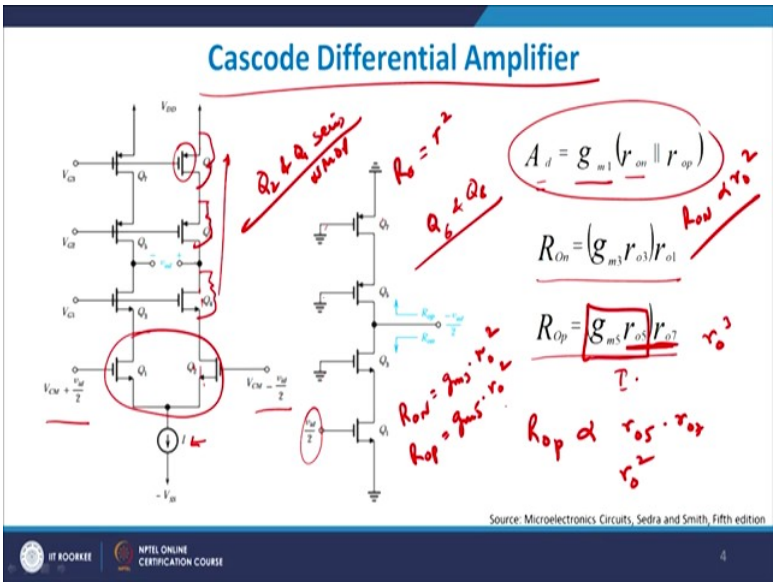
Similarly, in P MOS I can do one more thing that this Q3 can be actually grounded, so if you ground your MOS device and if your drain voltage is already grounded here and your gate is also grounded then gate to source is this one, right? Will always be negative value and therefore this will always make your Q3 on ON state and therefore they will all be like pure resistive domain architecture and they will give you V_{OD} by 2.

If I give, half circuit concept, so if I give V_{id} by 2 here I get V_{OD} by 2 in the output side. And therefore, I get A_d equals to g_{m1} into r_{01} into parallel to r_{03} which means that the overall differential mode gain is depending on the transconductance of the input transistor. So these

Q1 and Q2 are referred to as input transistors, right, whereas Q3 and Q4 are referred to as loads.

In this case active loads, right? So they are referred to as active loads. And therefore when you do r_{01} parallel to r_{03} because if you look carefully r_{03} is here and you have r_{01} here. Since these 2 are in parallel the effective load seen by the Q1 will be r_{01} parallel to r_{03} and you can automatically therefore gates the value of drain voltage in the output side.

(Refer Slide Time: 14:42)



Another method which people adopted and it is still being adopted with certain disadvantages of course is, what is known as a Cascode differential amplifier. So, what we do is, your Q1 and Q2 which is basically your driver transistors they are N MOS devices driven by V_{CM} plus V_{id} by 2 and V_{CM} minus V_{id} by 2 as we discussed earlier and we have a current source here.

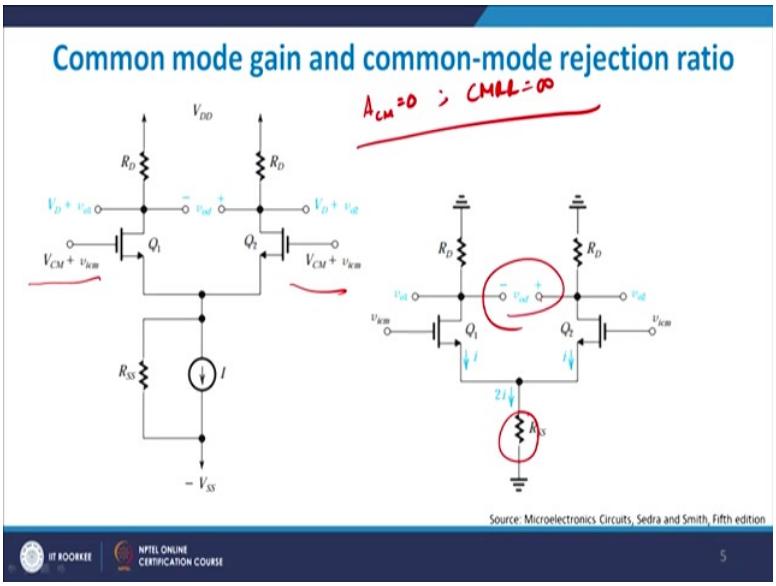
But what we tried to do is in the pull up state, in the higher state we try to have large number of devices and stacked, so in a Cascoded fashion. So that the overall gain can be increased higher and higher because you will have so much larger of devices in parallel with respect to each other. Therefore, I get in this case to be equals to g_m 1 which is again this one into r_{on}. r_{on} is basically r_o output resistance of N MOS which is this one.

And then parallel resistance of, gives you r_{op}, so g_{m1} into r_{op} into r_{on} is effectively a value of Ad, so if you look at the half circuit concept once again I ground these 3 small signal analysis you have V_{id} by 2 here and I get r_{op} equals to r_{on} which is r_{on} equals to this much. r_{on} and r_{op} is what? r_{op} if you look very carefully is basically looking from the side if you go up.

So you will always have r_{o7} and r_{o5} in series. You see g_{m5} into r_{o5} is nothing but the current flowing through the resistance into the MOS device Q5 current that if you multiply with r_{o7} which is basically the parallel impedance then we get automatically the value of this thing. So if you remember when we try to find out the resistance, it is basically the small signal resistance square which we are trying to find out, right?

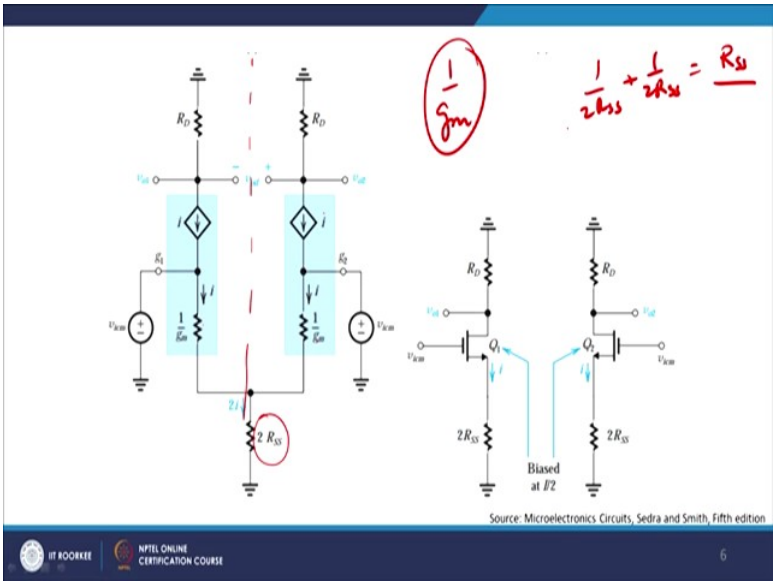
So, Ro is nothing but the square. So if you see r_{op} is proportional to r_{o5} into r_{o7} which is basically if I assume them to be equal I get r_o square, where you do therefore triple Cascode I will get r_o cube. Similarly R_{ON} will be proportional to r_o square because there are 2 transistors in series. So, Q2 and Q4 are in series and they are N MOS and therefore, I get this much. Similarly, Q 6 and Q 8 are again in series and I get g_{m3} multiplied by r_0 square. So what I get is, R_{ON} is equals to g_{m3} multiplied by r_0 square. I get r_{op} to be equals to g_{m5} multiplied by r_0 square. And therefore, simply by choosing higher value of g_{m3} and g_{m5} I actually manipulate the overall resistance or overall gain of the system.

(Refer Slide Time: 17:37)



If you look very carefully therefore that we have discussed in the earlier phases that common mode gain will be always 0 and your CMRR will be always infinitely high. So A_{CM} will be approximately equals to 0 and your CMRR, we have already discussed this point I really should be equal to infinity, right? And that is what I have shown here, that if you have V_{iCM} V_{iCM} I get this and if you do a design than what I do is, I make it R_{SS} assuming that both the currents or i1, i is current flowing I get 2i current flowing here and therefore, V_{od} will always give you a 0 value at the value of common mode signal.

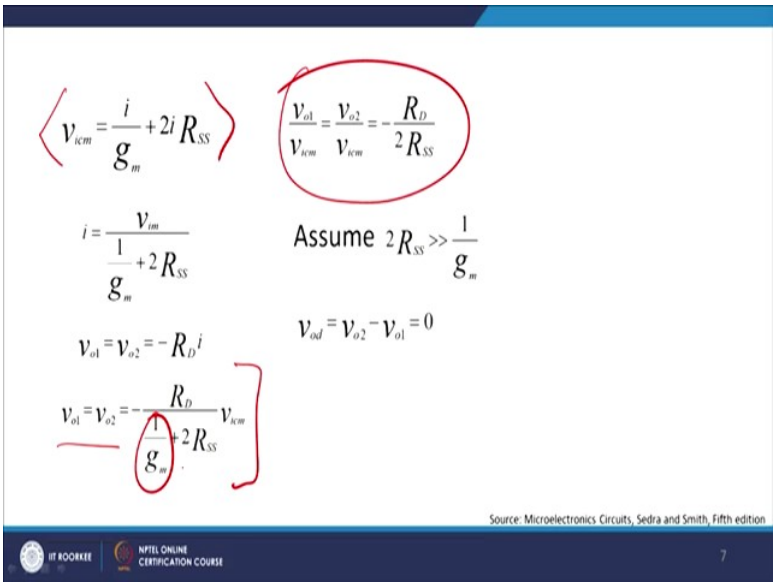
(Refer Slide Time: 18:19)



Therefore, as I discussed with you just now and I was deriving also with you. Do a half circuit here, remember? I remove the MOS device here and show it as a current source in series with 1 by g_m, remember because looking at the source side the amount of resistance offered is actually equals to 1 by g_m.

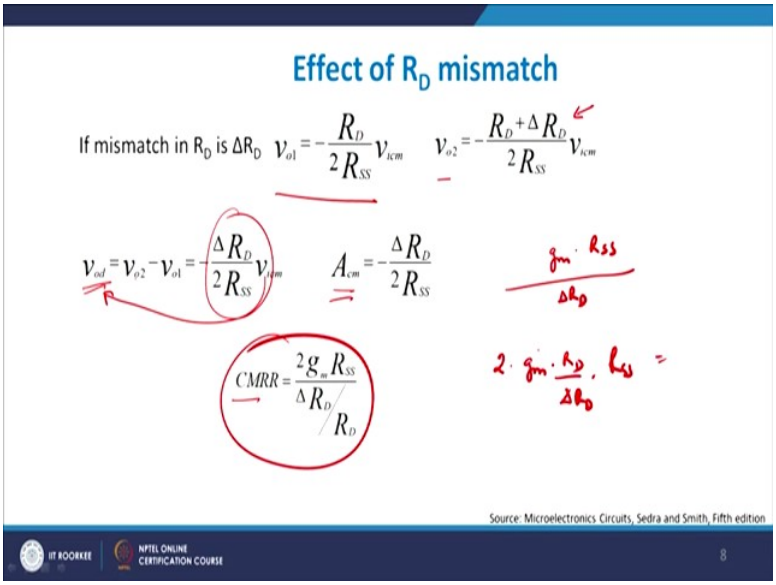
So, I simply do a series connection between the current source and 1 by g_m, current source and 1 by g_m. And then to R_{SS} because one by 2 R_{SS} plus 1 by 2 R_{SS} in parallel will always give you R_{SS} value in more respect and that is the reason when you do a half circuit I get 2 R_{SS} V_{o1} are ready and then I get I buy 2 current is flowing within 2 arms, right? And this is what the general scheme of things are.

(Refer Slide Time: 19:04)



Now, if you see Victim as I discussed with you will be I by gm plus 2i R_{SS}, right? And similarly as I discussed with you just now that V_{01} by V_{CM} plus V_{01} by V_{ic} is our ready by 2 R_{SS}. If I assume them to be equal I get V_{01} equals to V_{02} equals to minus R_D by g_m. What we did was, that 1 by g_m is much smaller and therefore is R_D by 2 R_{SS} the value of your output voltage.

(Refer Slide Time: 19:33)



Let me, therefore, come to the next stage in R_D mismatch, let me explain to you what is R_D mismatch? See what was happening till now, all this discussion was with the assumption that

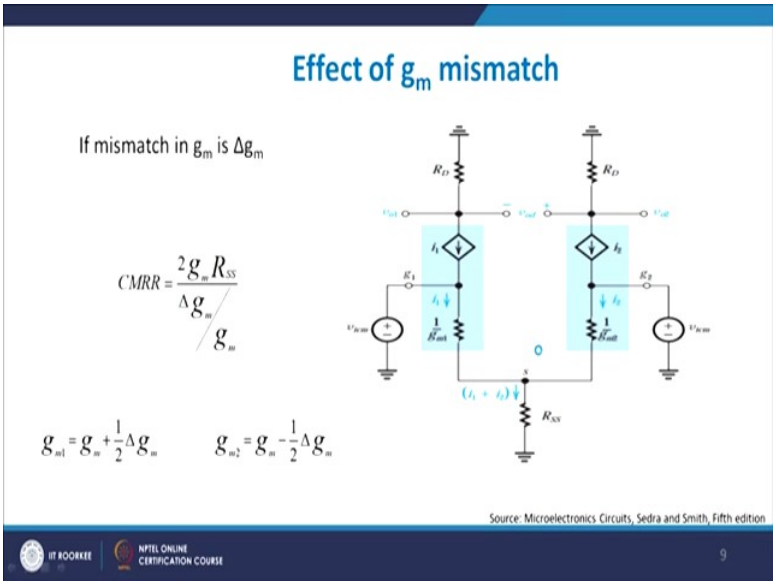
there is no mismatch of the resistances and the transconductances of the device used in the left arm and right of the differential amplifier. They are perfectly symmetrical and therefore all the common mode signals were lost and all the differential signals were magnified.

In reality not true. When you actually fabricate a circuit you will always have a mismatch of the resistors which means that you cannot have a fixed value of register always available with you, they will always vary with each other. So, let us also come to the point that if there is a mismatch in the drain resistance, for example, then how does it influence my common mode rejection ratio?

If you look very carefully if there is a mismatch, as I have discussed with you it is basically our R_D by 2 R_{SS}, remember? We just now saw, V_{01} is equal to R_D by 2 R_{SS} and V_{02} will be equal to R_D plus let us suppose is Del R_D by 2 R_{SS} into V_{icm}. So we have seen the effect of Del R_D and V_{icm}. So, V_{od} output difference is V_{01} minus V_{02} turns out to be this value, right?

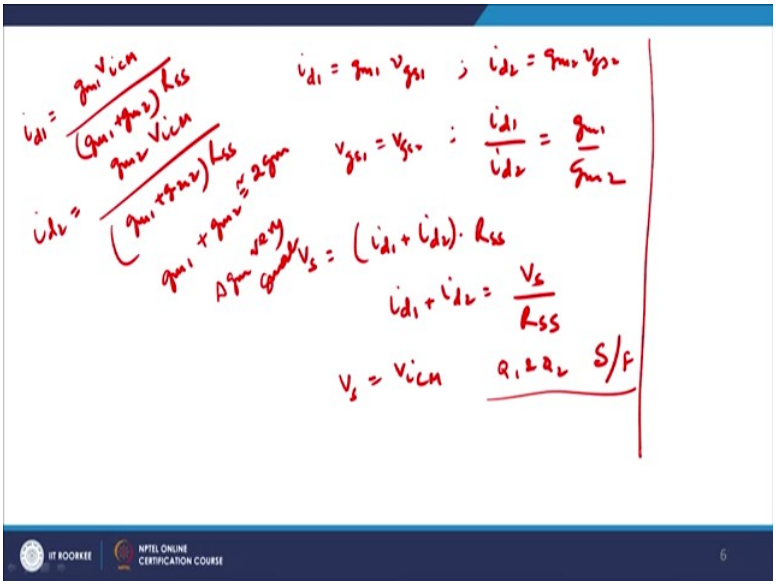
And therefore A_{CM} is basically, so what I do is, I put it into denominator and therefore I get A_{CM} equal to Del R_D by 2 R_{SS}. So CMRR is how much? Will be equal to 2 because if you remember, so you will get Del R_D by 2 R_{SS}, so you will get gm times R_{SS} divided by Del R_D by 2 R_{SS}. This 2 R_{SS} will go to the top and you will get this value of CMRR, right? How much you get? You get 2 times g_m times, right? R_D by Del R_D into R_{SS} as your CMRR.

(Refer Slide Time: 21:34)



Now, if you do a g_m mismatch which is transconductance mismatch. Let us see how it works out in that sense?

(Refer Slide Time: 21:47)

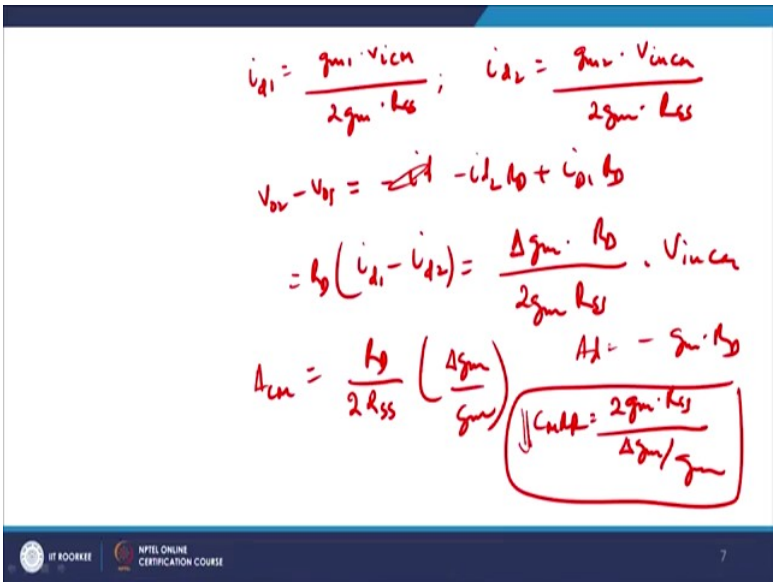


So, if we do a trance conductance mismatch, let us suppose I have got id1 to be equals to gm1 V_{gs1} and i_{d2} to be equals to g_{m2} V_{gs2}, right? And if I assume that V_{gs1} is equal to V_{gs2} and then I get i_{d1} by i_{d2} to be equals to g_{m1} by g_{m2} and therefore I get V_s which is the source resistance to be equals to i_{d1} plus i_{d2} multiplied by RSS and therefore, I get i_{d1} plus i_{d2} to be equals to V_s by R_{SS}, right?

Now, Vs is nothing but ViCM, because that is a voltage difference between the 2, why? Because Q1 and Q2 are basically source followers, so whatever value of voltage you are giving on the gate side appears across the source side. So the difference between them is almost equal to 0 and therefore I get as this thing. So, I get idi equals to g_m times V_{icm} upon $_{gm1}$ plus g_{m2} divided by R_{SS}.

And I get $_{id2}$ to be equals to g_{m2}, for this is gm1 into ViCM upon g_{m1} plus g_{m2} divided into RSS, right? Now, if I assume that g_{m1} and g_{m2}, the difference is very small then I can safely write down gm plus g_{m2} is approximately equals to twice g_m. So, I can write down twice gm here and assuming that Del g_m is very small, it is not 0 but it is very small. So it is relatively very small, right? So if you get this into consideration or you get this into idea. I can write down, right?

(Refer Slide Time: 23:40)

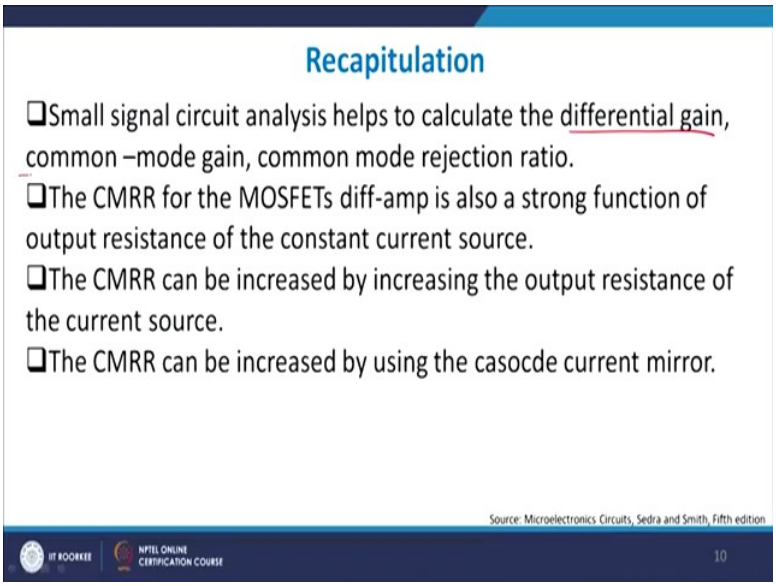


I can write down id1 to be equals to g_{m1} times V_{iCM} divided by $2g_m$ times R_{SS} and i_{d2} to be equals to g_{m2} multiplied by $V_{in}C_m$ divided by 2gm times R_{SS}. So, I get V02 minus V01 is equal to minus minus $i_{d2}R_D$ plus $i_{d1}R_D$ region. So if you solve it, I get R_D (i_{d1} minus i_{d2}) which is nothing but Delta g_m times R_D upon $2g_m$ R_{SS} multiplied by V_{inCM}. So, if you take V_{inCM} in the denominator I get A_{CM} equals to R_D by 2 R_{SS} into Delta g_m by g_m, right?

And since already we know that Ad equals to minus gm times R_D, I can write down CMRR to be equal to A_d by A_c which is nothing but $2g_m$ times R_{SS} divided by Del g_b by g_m, right? So this is for the overall CMRR which we see when we have a g_m mismatch, right? At this gm therefore depends upon the value of Del g_m. So when your Del g_m is typically very large, right?

It tends to lower your CMRR, right? So if your mismatch is low both in terms of R_D or g_m it lowers your CMRR and the reason is very simple, why does it lower it? Physically also you can understand because then the common mode signal itself gets differentiated and gets amplified. Therefore the differential amplifier is not able to distinguish between differential mode signal and a common mode signal because both of them look the same to the differential amplifier and therefore it equally amplifies both the signals together, right? And that's a problem area which people face as far as mismatch is concerned.

(Refer Slide Time: 26:14)



So let me recapitulate what we have done till now and let me see what we will learn in the further. That any small signal circuit analysis where we assume that my transconductance is always there for the device which converts a voltage into a current source. We will be able to calculate the differential gain, common mode gain and the common mode rejection ratio this 3 very-very important.

In fact these 2 are very important automatically this is the third one which comes out of the difference between the differential mode and common mode gain. As we saw that CMRR will obviously be a strong function of the output impedance. The reason being higher the output impedance larger will be the differential mode gain and as a result will get a larger CMRR in that sense.

How can I increase it? I can increase the CMRR by increasing the output resistance of the current source which is very true also. More ideal your current source is better your CMRR is because you ensure that your source resistance of the MOS device is infinitely high, which is typically very high and therefore it sort of acts like a virtual ground, right? Virtual ground means though it is grounded in a sense but current is not flowing out of that particular arm.

And we also saw that CMRR can be increased if I do a Cascoded amplifier which means that I Cascade devises top of each other, stacking the devices as a result my overall output impedance increases and therefore my gain also increases or overall gain increases which

means my differential gain increases not at the cost of the common mode gain and as a result my CMRR goes to a very high value, right?

This we have learned through large number of simulation tools, through large number of understanding. We have also understood that this R_D mismatch and g_m mismatches will lower your CMRR. And it will not improve your CMRR and therefore from fabrication point of view one has to always entertain or one has to always see that you always have the perfectly symmetrical arms available to you.

Most of the time not available then my CMRR falls down from a large value to a relatively small value, right? So, lower your mismatches and try to make the gm of the input devices and the output impedances to be too large in order to increase the CMRR and therefore reject the noise, right? With this let me thank you for your patient hearing and we will discuss other topics in the upcoming tutorials and slides, thank you very much.