Microelectronics: Devices to Circuits
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Lecture 37
Small Signal Operations and Differential Amplifiers-I

Hello everybody and welcome to the next addition of NPTEL online certification course on Microelectronics Devices and Circuits. In our previous modules we have actually seen differential amplifier using bipolar technology and we came to a major important issue that all common signals are being rejected and all differential signals are getting amplified. Common signals primarily mean that noise signals are getting rejected and all your differential signals which are the input signals given will always be amplified.

This results in one important parameter known as Common Mode Rejection Ratio - CMRR which is defined as a ratio of the differential mode gain to that of the common mode gain. So it is basically A_D by A_C. So to just give you an idea about what I was talking in our previous discussion is to remind you because we will be starting from where we left in our previous term and we will see how it works out in this case.

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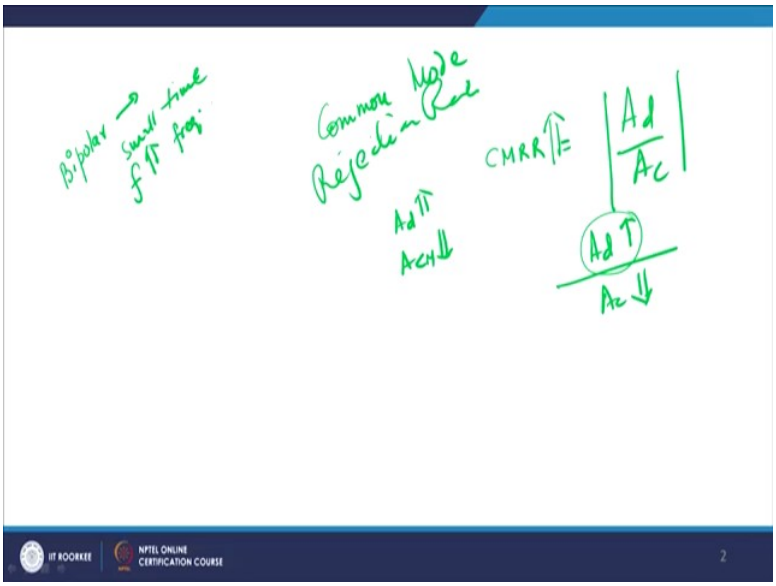

So we had defined another term that is known as CMRR known as Common Mode Rejection Ratio and we saw that this to be equals to A_d by A_c, we do not take the sign of it but it is differential gain upon the common mode gain. Now, typically since A_d is large and A_c is very-very small, right? Because the idea is that the common mode signal needs to be

suppressed and therefore amplified less as compared to differential mode design. And that is the reason your CMRR is relatively very high, right?

So, this is one of the design criteria's we generally follow in an amplifier that especially in differential amplifiers whose CMRR should be high. So we understood to things that A_d should be high and A_c the common mode signal CM should be low, right? To do that we first buyers the device in a BJT in the active region and we do not let it go into the saturation region but we go from active to cut off and cut off to active because we want the switching speeds to be higher.

So if we take a bipolar technology, right? Bipolar technologies have typically very small switching times or its frequency of operation is very-very high, right? Its frequency of operation means the frequency by which the switching can takes place is very-very high and is one of the major advantages of bipolar technology. What we will do in today's lecture is we will replicate the same thing which we did in our earlier design or in our earlier bipolar technology and we will try to have it through MOS technology because CMOS is the standard sort of industrial standards.

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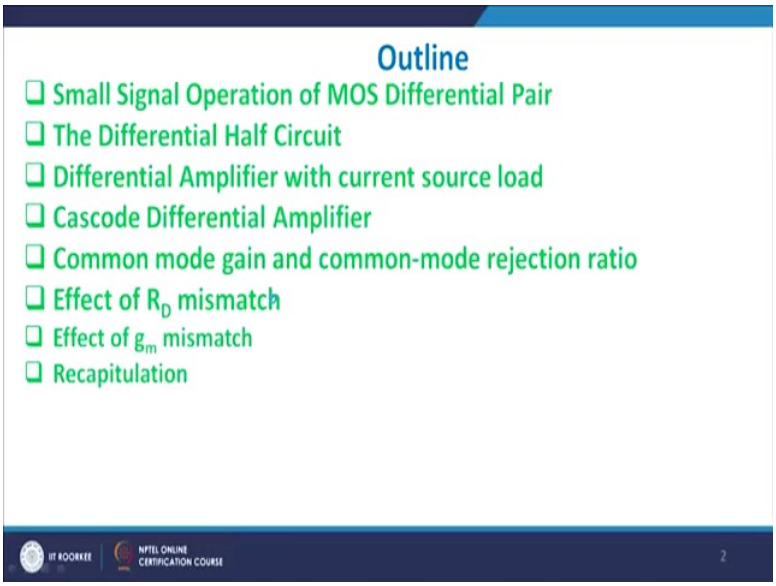

And therefore what we will do is we will just look into the following outline of the talk. We will look into the MOS differential pair, how a MOS differential looks like? What you understand by differential of circuit? We have already seen it but we will see it in details. Then we will put a current source load at the output and see how it works out. Then we will

look at the Cascoded differential amplifier CMRR the meaning of CMRR with respect to CMOS technology.

And then this comes with the fact that till now we were all assuming that the resistances in the left and right arm of a bipolar technology based differential amplifier are exactly symmetrical which means that both the transistors are both the bipolar will have the same value of beta, Alpha, will have also the same value of the drain resistance RD, in such a scenario you are able to reject the common mode noise very easily.

But in reality when you actually fabricate you will always have certain mismatches in the transistors, in terms of its transconductance as well as the drain resistance R_D. So that we will be studying in the next 2 slides or the next 2 sections that is R_D mismatch and gm mismatch. So we will look into these mismatches and see how does it affect our overall picture as far as the small single, small signal operation of MOS device is concerned?

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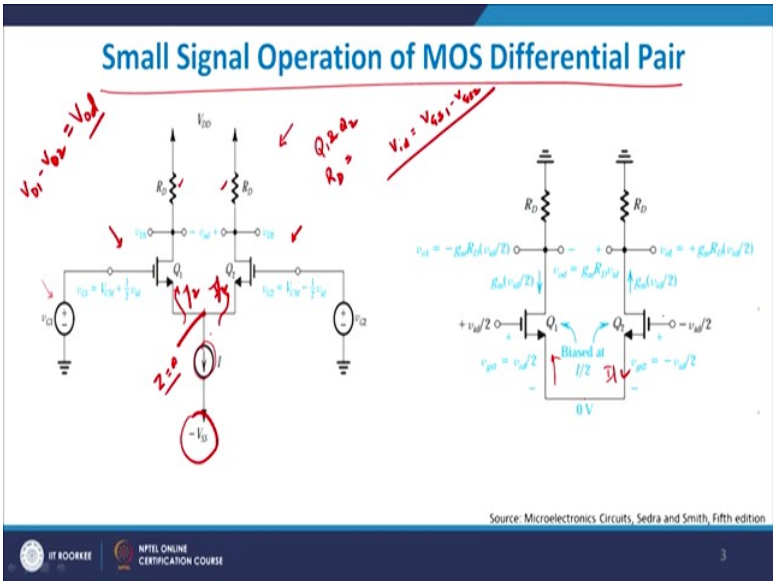

Let me come to the small signal operation of a MOS device and as you can see here what we have done here is that, please remember from our previous discussion that whenever you did have a common mode signal, right? We discussed the fact that a common mode signal will always give you a 0 differential output, right? Another reason was very well known to us because the same current was drawn through both the arms and therefore, the voltage drops at the output were exactly the same, if you subtract 2 equal quantities you always get 0 voltage.

Now, if you look at this left hand side slide, you will see that what we have done is, that we have given a gate voltage onto the gate side of Q1. We are assuming that Q1 and Q2 are 2

symmetrical transistors and R_D is also the same value which is in the left and right arm under such a scenario if I give a differential input then V_{id} is defined as the difference between the V_{GS1} minus V_{GS2}, right?

So different signal is given. So what I do is that, so I divided by 2, why? So the difference signal divided by 2 and we give first one half to this part and the negative half to this part, so that they are 180 degree phase shifted with respect to one another and therefore, I would expect to see maximum gain out of it, right? And we try to find out the value of V_{D1} minus V_{D2} or V_{D2} minus V_{D1} and I get what is known as V_{od} output difference.

So, V_{id} means input differential voltage, V_{od} means output differential voltage, right? Assumption again that Q1 and Q2 are perfect transistors and you have a current source which is basically your i_{ss} or the current source here which is given by i. It is connected to minus V_{SS} on the side and therefore this is basically your high impedance note is the Z equals to infinity at this particular point and therefore whatever current is flowing will be equally distributed across this arm and this arm as I by 2 and I by 2.

With this knowledge let me shown here that since this is basically, the current shows it is terminating here and therefore, what I have shown here is, it is not grounded, right? So it is basically a floating note sort of and therefore the overall current will always remain the same in these 2 arms. So, I by 2 I by 2 provided the amount of voltage given to Q1 and Q2 are exactly the same, right? Then only we will see that the overdrives are equal and therefore the same current will be drawn in a respect.

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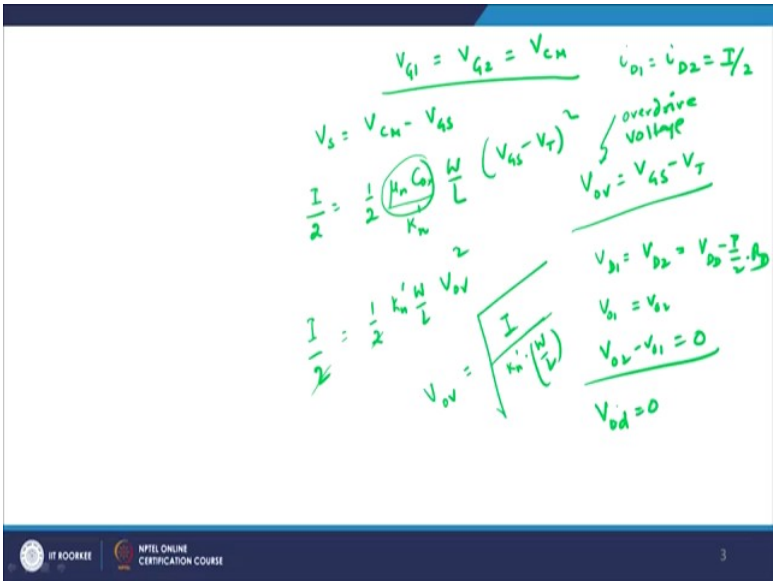

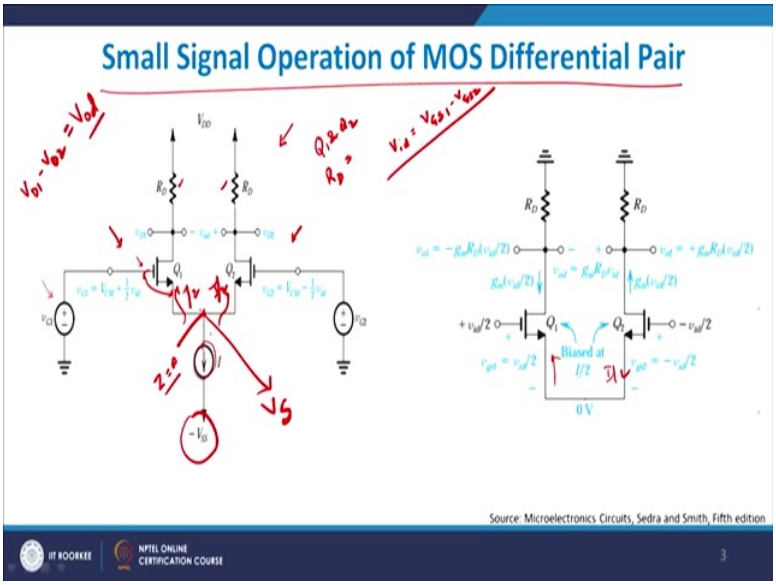

So with this knowledge let me show you how does it work out in terms of working principles. So I can safely say that V_{G1} is equals to V_{G2} equals to let us suppose V_{CM}, right? Let us suppose I have a common mode signal been given whose value is equal to V_{CM} then I get i_{D1} equals to i_{D2} equals to I by 2, right? Because you are drawing i current and then therefore half the current will go to left and half the current will go to right arm.

Therefore, V_S is equal to V_{CM} minus V_{GS}. What is V_S? This point is S, so the voltage at this particular point is nothing but the applied voltage at this particular point minus this difference gate to source will be this voltage. And that is what I have shown here so V_{CM} minus V_{GS} that I get I by 2 therefore current equals to 1 by 2 mu , right? C oxide W by L which is the process trans conductance parameter we have already seen this into V_{GS} minus V_T whole square this can also be written as K_n' me to a larger extent. Where we can write down $V_{overdrive}$ to be equals to V_{GS} minus V_T this is known as overdrive voltage, right?

It is overdrive voltage which is equal to V_{GS} minus V_T therefore I can just replace this and write down half Kn', right. * W by L into V overlap Whole Square this is equals to I by 2. Which means that if you therefore find out I overlap this 2 will cancel out and therefore my V overlap comes out to be equal to how much, you just check it out it will be given as I divided by Kn prime into W by L this thing in square root of this one that I is the current drawn to say. W by L is the aspect ratio and Kn prime is given by mu_n into C oxide, right? And I get $V_{overlap}$ to be equals to root of this whole quantity.

Therefore I can write down in such a scenario when VG 1 equals to VG 2. I can write down therefore V_{D1} equals to V_D to equals to V_{DD} minus I_D is I by 2 into R_D and therefore I get that

which basically means that V_{O1} and V_{O2} are exactly the same and therefore if we subtract V_{O2} minus V_{O1} I will get output voltage to be 0 or I can write down V_{OD} to be equals to 0. So therefore any common mode signal as I discussed in your BJT also. In a MOS device also the common mode signals that is vanished off because its output value is illustrated in this manner.

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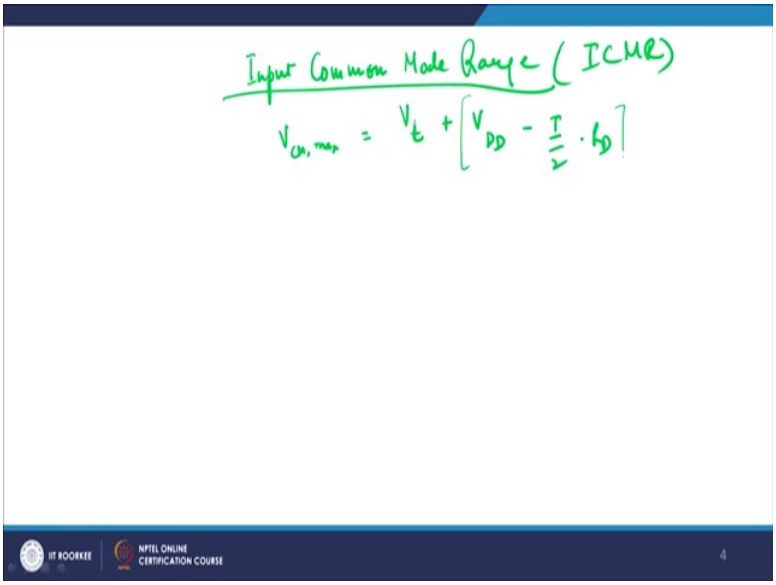

Now, let me therefore explain to you what is known as Input Common Mode Range. So what the idea is, we also refer it to as ICMR. Now ICMR basically tells me therefore what should be the maximum input range to ensure that the transistor which you are working is actually working in active region and going to cut off.

So you have to be very careful that you do not let the transistor go into the saturation directly but right from the active region it goes to the cut-off region and vice versa. Now, let me just write down for you and we will explain this later on that $V_{CM\text{-}Max}$, V_{CM} means the common mode maximum voltage which you can give is basically V_t plus V_{DD} minus I by 2 R_D, you know the reason why, because, you see V_{DD} minus I by 2 R_D.

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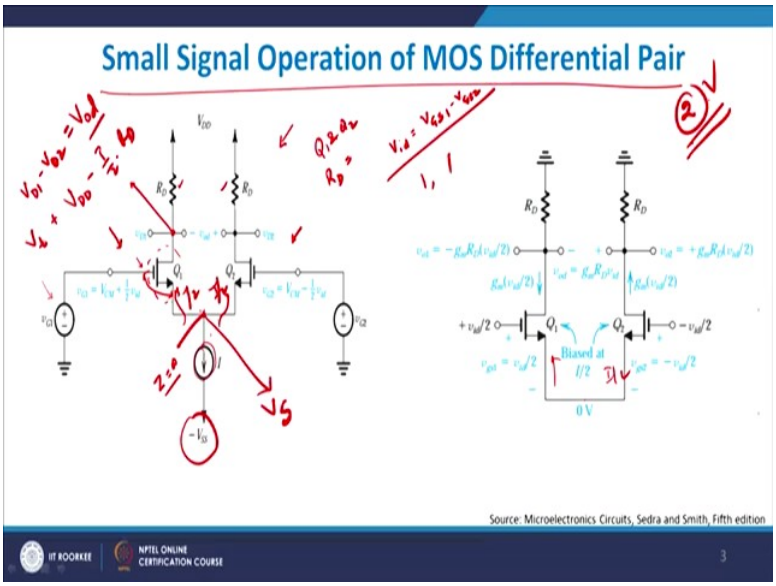

If you look very carefully here is the voltage at this particular point, this is V_{DD} minus I by 2 into R_D is the voltage at this particular point. You are added V_t to it threshold voltage of this device Q1 this has to be the minimum voltage. See, if my voltage falls below this, right? Say my threshold voltage is, my V_t is say 1 volt and V_{DD} minus 1 by 2 R_D is equals to say 1 volt again.

So 1 plus 1 is 2 volts, so minimum common mode voltage which you should give to the input of Q1 or Q2 assuming database symmetric minimum is 2 volts. If you keep the voltage less than this 2 volts then either Q1 will be turned off permanently or you will never get this much amount of voltage drop at the output of your V_{01}, right? And therefore, this is the reason why we define this to be as the maximum value which you see.

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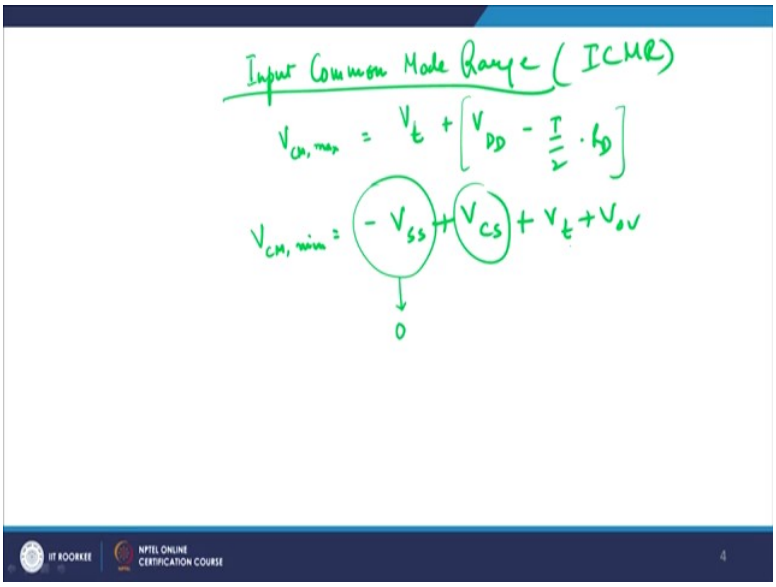

Now, what is the meaning of $V_{CM\ min}$, minimum CM voltage is minus V_{SS} plus V_{CS} plus V_t plus $V_{overlap}$. Now, obviously this could be grounded also, so this can be put to 0 otherwise it is connected to a negative terminal. V_{CS} is this voltage which I will just show it to you.

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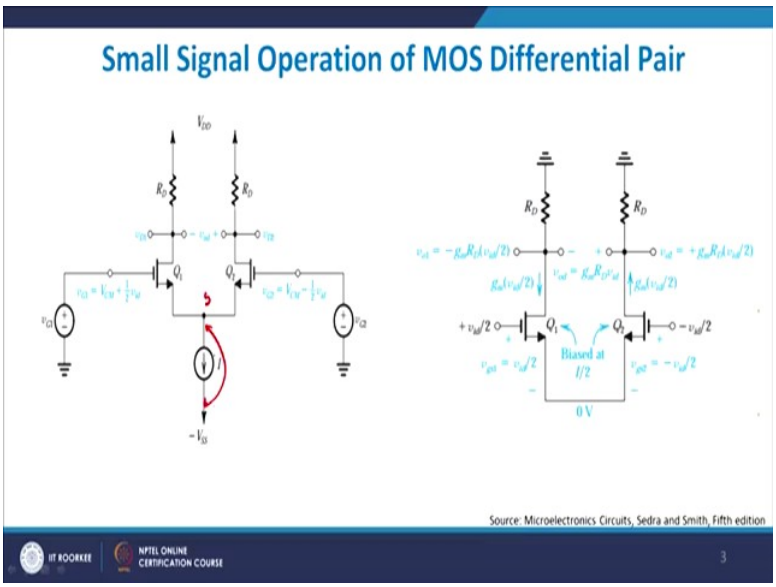

This is the voltage which I discussed with you just now. V_{CS} means this is the S value, right? From this point to this point this is the V_{CS} value which is the voltage across the current source that is the minimum value plus what do you require?

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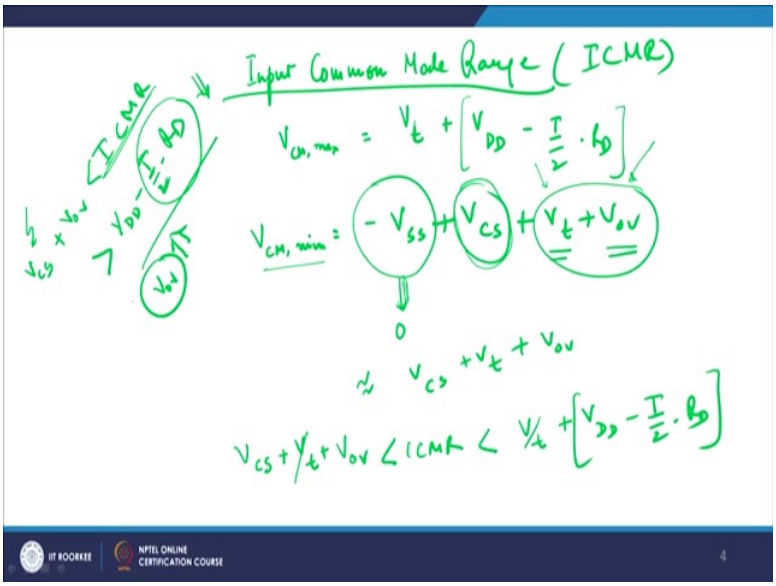

Plus you require V_t threshold voltage of the Q1 transistor and $V_{overdrive}$. You understand why these 2 are kept because otherwise the system will not get on. So your minimum common mode voltage should be this much that it should be able to switch on your device, draw the device into the active region by $V_{overlap}$ and should sustain a minimum value of voltage between the source and through the current source otherwise it will not work fine.

And VSS for all practical purposes always equals to 0 and therefore I can write down this to be typically equals to V_{CS} plus V_t plus V overlap. So the ICMR values which you see, right? The minimum value is this much, assuming V_{SS} equals to be equals to 0 should be greater than V_{CS} plus V_t plus $V_{overlap}$, right? And should be less than V_t plus V_{DD}, right, minus I by 2 into R_D, fine. So this is what we get maximum.

So if we relate these 2 from both the sides because they do not play a role as such I can safely write down that ICMR that V_{CS} plus $V_{overdrive}$ ICMR, right? And it should be greater than V_{DD} minus I by 2 times R_D, right? So you see therefore, if my V_{DD} is high, right? My input voltage should be also going higher and higher. My input Common mode range will also go higher. Similarly if my overlap is high my ICMR will also go high and the reason being in front of you that, it should be at least greater than V_{CS} plus $V_{overlap}$.

VCS is almost fixed because assuming that it's an ideal current source obviously the voltage across the current source will always remain fixed and therefore you add overlap you get ICMR. So ICMR is always greater than $V_{overlap}$ in all respects. If you go on increasing $V_{overdrive}$

you will be increasing the current and therefore what will happen is, this quantity will increase and therefore this quantity will actually decrease, right?

And therefore this will be obviously greater than the decrease quantity, right? So what people generally do is that, they try to make the overdrive slightly larger in order to sustain this relationship in real sense, right? And this is what is ICMR looks like in a real sense of operation.

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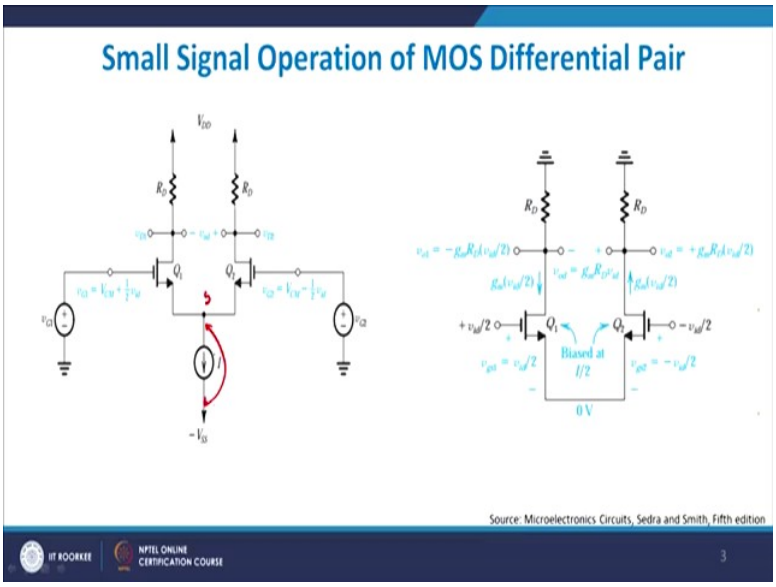

This is again as I discussed with you the small signal model, right? And let us now put a input differential signal and see how it works out.

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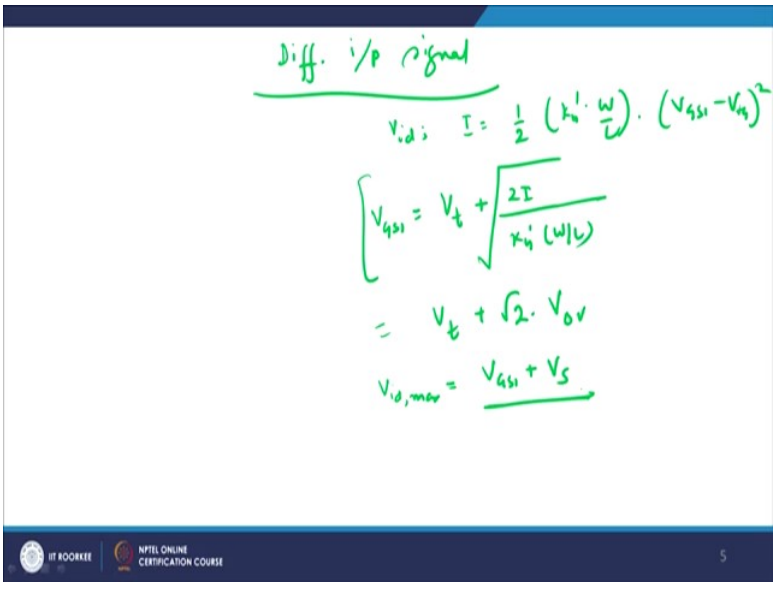

So, what I do I now put a Differential Input Signal and then what I write down is I refer to as V_{id} and therefore, my current is equals to 1 by 2 K_n prime into W by L into V_{GS1} minus V_{th} whole square assuming it to be in the active region. Therefore, V_{GS1} is equal to V_t plus 2 I by K_n prime into W by L root over. This is equal to V_{GS1}, right? So that is nothing but V_t plus root 2 $V_{overlap}$ because if we take to outside than its root 2 into root of I divided by K_n prime W by L that is nothing but $V_{overlap}$, right?

So I get current to be equals to this much. Assuming that have the current is routed through both the arms. Similarly, I get $V_{iD\ Max}$, input voltage difference should be equals to V_{GS1} plus V_S and the reason being that, why it should be greater than V_{GS1} plus V_S is that, V_{GS1} is nothing but gate 2 source of…

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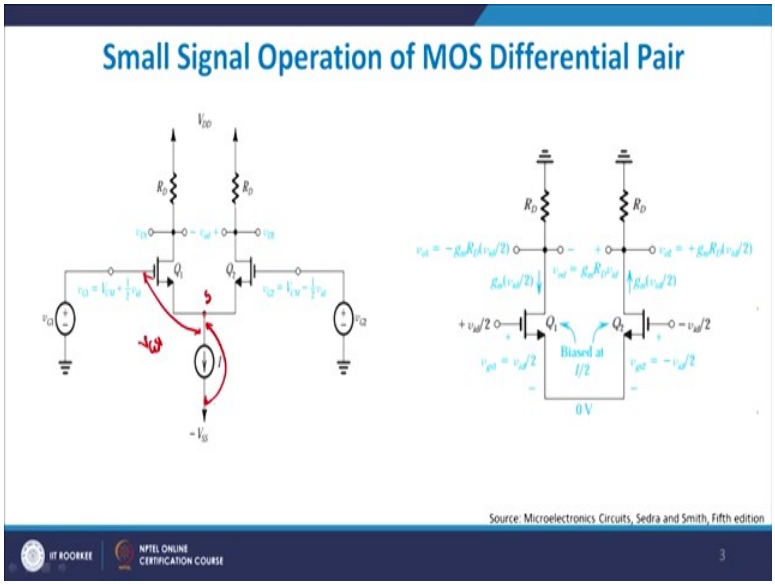

This is V_{GS1}, right? And this is V_S value, so this potential plus this will give you the potential at this particular point.

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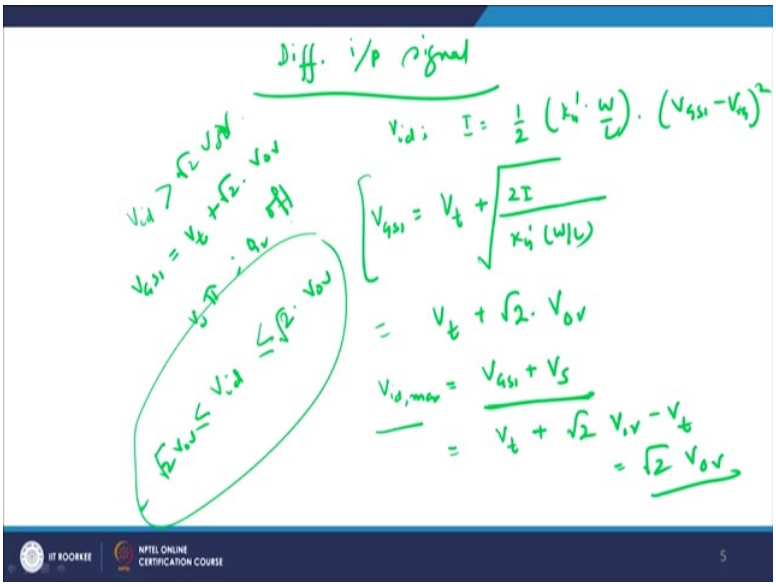

That is what I am trying to say here that V_{GS1} plus V_S should be here. If you solve this and do some small manifestation I get V_t plus root 2 $V_{overlap}$, right? Minus V_t and therefore this will come into root 2 $V_{overlap}$. So $V_{iD\ Max}$ is this much which you get. Now which means that if V_{id}, right? If it exceeds root 2 $V_{overlap}$ then what will happen is that all the current from one arm will be routed through other arm, the other arm will remain almost in the cut of position, right?

And that is the reason you do not like to draw it. And V_{GS1} will be written as V_t plus root 2 $V_{overlap}$ which means that as V_S will go on increasing, right? Q2 will be switched off, why? Because let us suppose your overdrive is increasing, right? And your source voltage is also increasing as you move along. If the source voltage is increasing and you are trained voltage is fixed, right? Then V_{DS} will go on decreasing.

Decreasing primarily means that you are forcing the device to go into the deep triode region but that is not my aim, right? And therefore, I cannot let my V_S fall down drastically below a particular point. And therefore, I do not want the Q2 to be fully off, right? And therefore, the maximum value which can be given to a system differential signal is that V_{id} should be greater than less than equals to root 2 $V_{overlap}$ and should be root 2 $V_{overlap}$, this is the final explanation of V_{id}.

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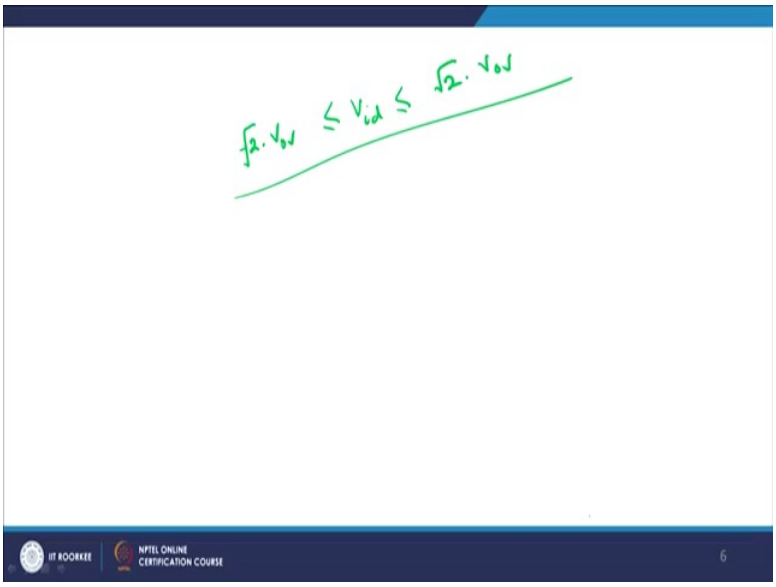

So, the differential signal maximum which you can draw is basically minus of root 2 into $V_{overdrive}$ and this is maximum of root 2 into $V_{overdrive}$, this is the range of input signals which you can give. Now, the idea therefore is that by giving such a signal I am able to sustain it. Anything larger lesser than this, larger then this will force further the transistors to go into cut off and other will not go into cut off in a general sense. So this is the maximum value of signal which one gets, right?

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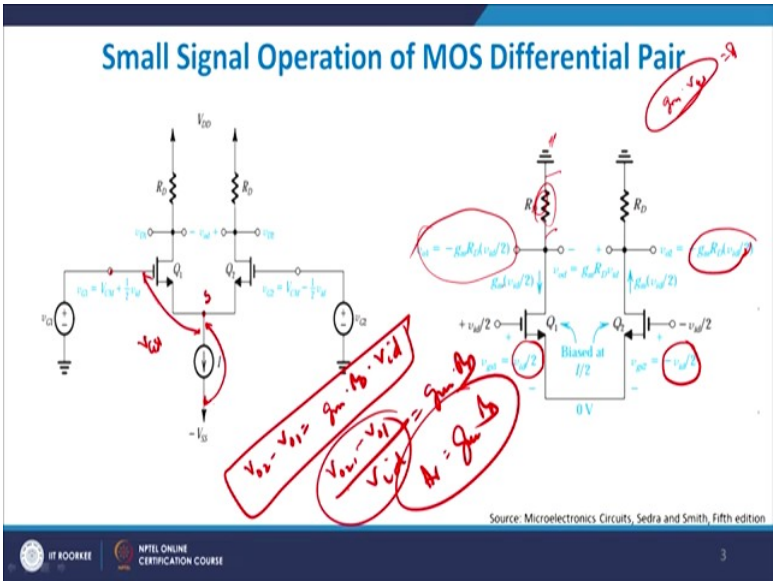

So, let me show to you therefore what is happening here. As you can see a bias state, I have V_{GS1} equals to V_{id} by 2 and V_{GS2} is therefore minus V_{id} by 2, right? And therefore this much

amount of current is flowing through system gm times VGS is basically my ID, so VGS here is nothing but V_{id} by 2. So g_m multiplied by V_{id} by 2 is this current, this multiplied by R_D, right? Is the voltage across this device, since this is already grounded I get V_{01} to be equals to minus g_m R_D upon into V_{id} by 2.

Similarly, if you look at this side you will get gm R_D into V_{id} by 2 which you get, right? And therefore if you subtract this minus this which is V_{02} minus V_{01} I get this plus this and therefore I get gm times R_D times V_{id}, right? Therefore, V_{02} minus V_{01} by V_{id} is nothing but gm times R_D and this is only for the voltage gain because this is the output voltage is difference divided by input voltage difference turns out to be therefore g_m times R_D, right, which is exactly what we have already derived in our previous discussion and slides.

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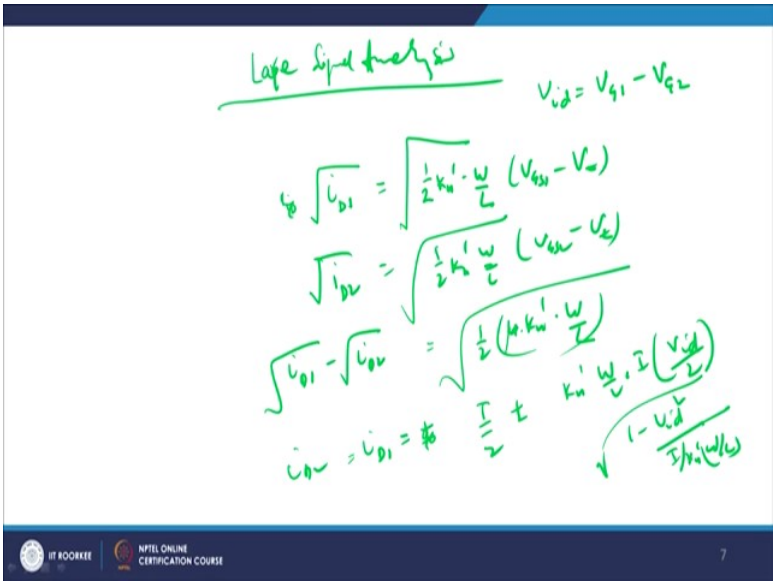

So, with this knowledge let me show to you the large signal analysis here. In the large signal analysis what I can write down is, I am assuming that V_{id} equals to V_{G1} minus V_{G2}. So, if I solve it I get root of i_{D1} is equals to 1 by 2 Kn' W by L root over into V_{GS1} minus V_t. similarly root i_{D2} to be equals to 1 by 2 K_n prime W by L into V_{GS2} minus V_t, fine. So if you subtract i_{D1} minus i_{D2} square root of that, right?

Something will cancel out and I get root of i_{D1} minus root of i_{D2} equals to half Kn' into W by L, right? This is what you get as the overall i_{D1} minus i_{D2} and if you do a small manipulation I get i_{D1} to be equals to i_{D2} equals to, right, I by 2, right? Plus minus, so this is plus minus Kn prime W by L into I into V_{id} by 2, right? And then square root of 1 minus V_{id} square divided by I upon Kn' W by L.

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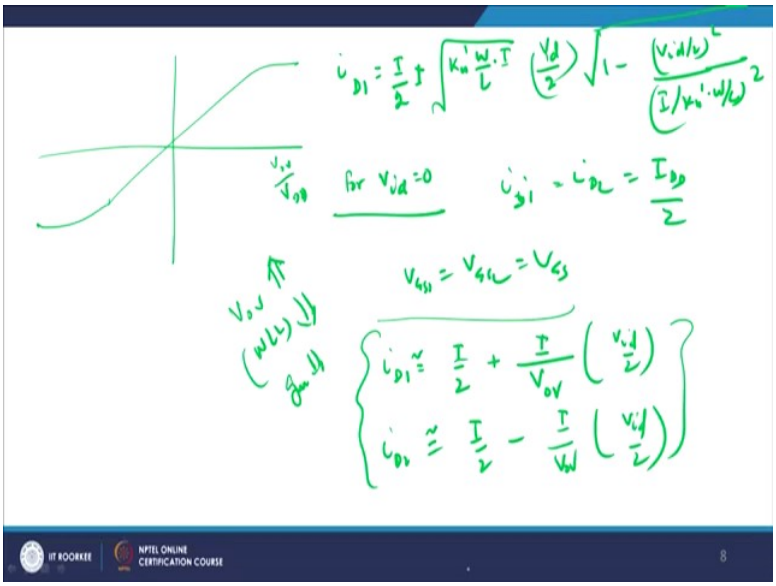

So, I will just write down for your information said what I got. I got i_{D1}, right? Equals to I by 2 plus I by 2 plus minus root over (Kn prime into W by L into I , right? This is into Vid by 2, right? And this is root over 1 minus Vid whole square divided by I divided by Kn' into W by L whole square. This is your i_{D1}, similarly i_{D2} will be with the negative sign of course here.

Now, for Vid equals to 0 which is then there is no differential signal implies that your i_{D1} will be exactly equals to i_{D2} equals to I_{DD} by 2, half the current will flow through this arm. Now in that case V_{GS1} equals to V_{GS2} equals to V_{GS} gate to source of first transistor, right? And that gives me a proper idea about where you will be biasing your device in order to get such a figure.

So, what I get from this figure, all this discussion is finally I get I by 2, right? I by 2 plus I by $V_{overlap}$ into V_{id} by 2 right? And then I get i_{D2} to be approximately equals to I by 2 minus I by $V_{overlap}$, right? V_{id} by 2 I get which means that the currents which I see they are separated by each other by 180 degree phase shifts, right? So this is another issue which we have also dealt in BJT when we are plotting the current versus $V_{overlap}$ by V_{DD} and you will see that all of them crosses through 0 and then they get something like this.

So the gain actually starts to roll off at higher values of overdrive. So if you want to sustain a large amount of linearity that is always advisable to keep your $V_{overdrive}$ to be as large as possible, right? Which implies the W by L should be as small as possible, right? And therefore the trans conductance will be a small as possible.

The reason being that g_m when you keep overdrive voltages very large, right, which means that V_{GS} minus V_T is typically very large which also sustains that your g_m will be also large and therefore gm times R_D becomes large which means that the overall gain of the system actually increases drastically. The cost you pay for it is heavy nonlinearity in a real sense. So that is very-very heavily non-linear and gives you a difficult time in terms of understanding the theory behind it and it is really difficult to get the whole of it.

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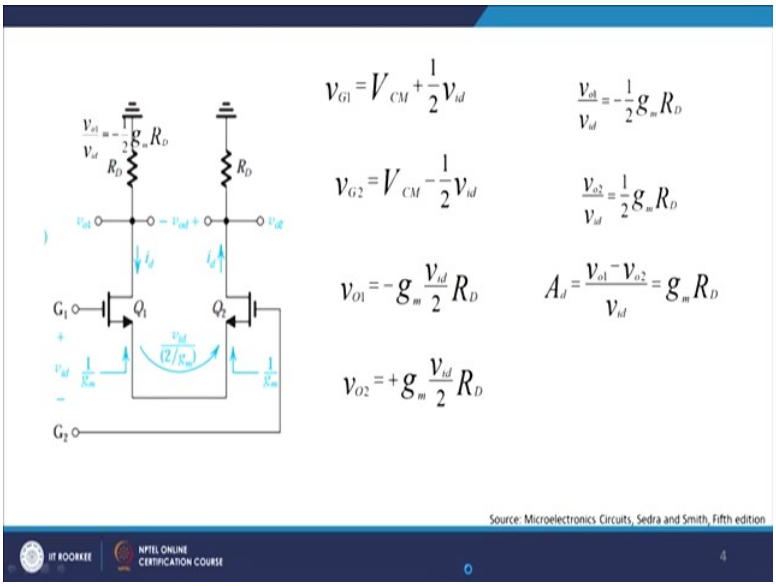

So what I do, as I discussed with you just now that if I do a simple design here which is basically even your half circuit design, this is basically a half circuit design, I can show to you that using this half circuit design we can actually do it. What is half circuit? Well, half circuits are very standard methodology used in analog circuit design or mixed signal design where we assume that since the ground and power supply are the same for both the arms.

I can divide the 2 arms into 2 parts and then just fine for one something, some important term and do a complimentary equation for the second one assuming that they are perfectly symmetrical with respect to each other and these are known as differential half circuits.

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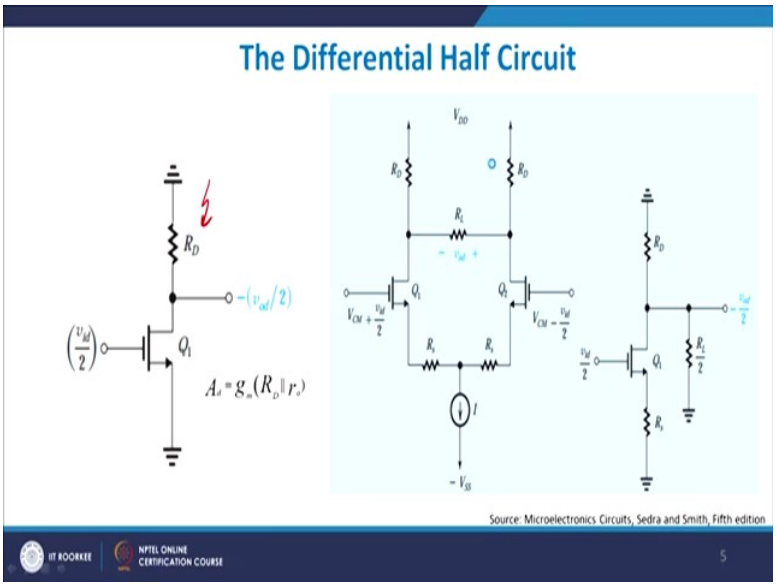

Maybe, I can show you, yes. As you can see it is a differential of circuit, right? So this is the differential half circuit which you see here, right? And we will discuss this in detail as we move along. But this is what your differential amplifier based design, right?

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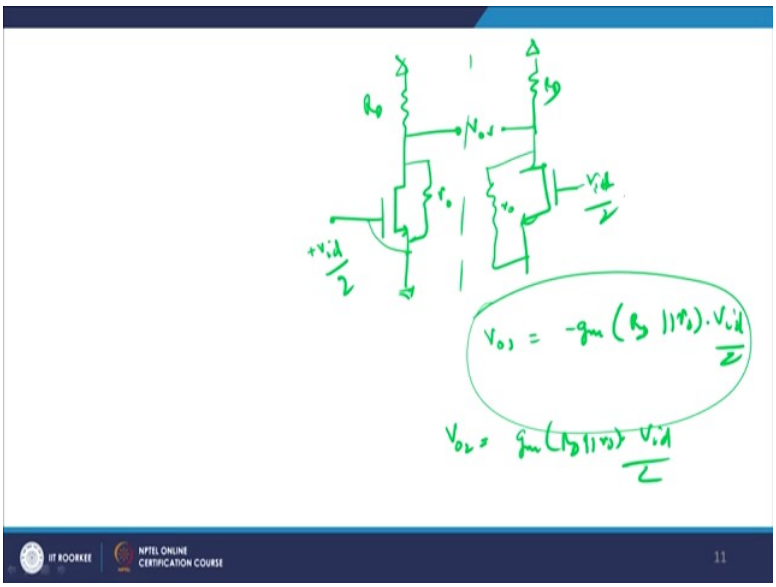

So with this knowledge or with this idea let me come to differential half circuit and explaining to you how it works out, right? So the differential half circuit, does what? It divides the whole phenomena or the whole devices or the whole material or the circuit into 2 parts. The first part is basically your R_D, right? And of course this is the plus V_{id} by 2 half the value of the difference then what you do is you grounded first of all.

And then assume that across the gate to source you have r0 here and you have RD here and then you have V here and then you have R_D here, right? And this is grounded, this is also grounded then as you come down to enter into this thing, so this is my minus V_{id} by 2 because they are perfectly anti-Semitic with respect to each other, right? And therefore this will also have resistance which is basically given as r0 also in this case.

So this is the half circuit which you see, right? Half under this side, half under the side therefore I can write down V01 to be equals to minus gm times R_D, right? Parallel to r0 multiplied by V_{id} by 2 because this is grounded, so V_{GS} is nothing but V_{id} by 2. So, V_{id} by 2 minus that threshold voltage of the device is the overdrive and from there I get V_{01} to be equals to this value which you see. And similarly V_{o2} hour output voltage 2 will be given as g_m times R_D parallel to r_o into V_{id} by 2 of course just with a negative sign changes there.

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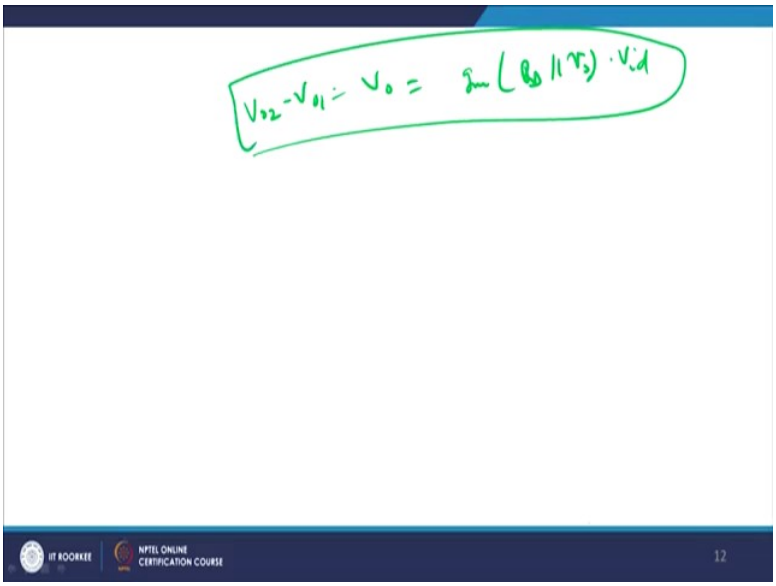

With this knowledge I can safely write down V_{02} minus V_{01} which is V_0 to be equals to g_m times R_D parallel to r_o, right? Into V_{id}, right? So therefore if I do a pure differential analysis or pure differential analysis as such then what we get is that we get the output voltage difference to be equals to gm times R_D parallel to r_o into V_{id}, right? And therefore higher the value of g_m more is the gain which you get at the cost of linearity.

So, linearity is always adversely getting affected by high gain because when you do a high gain you primarily also increase the non-linear distortion as compared to your signal like both of them increase and therefore it's sort of losing out the whole thing as far as design is concerned. In our next segment of slide we will do some mismatching of R_D and g_m which we

were supposed to do in this part and then we will discuss about differential amplifier cascoded and then common mode games we will discuss, right?

So, I think we will stop here at this stage and in the next module we will discuss the R_D and gm mismatch as we will also discuss about CMRR and the Valley of A_{CM} for CMRR equals to infinity, thank you. Okay, thanks a lot, thank you very much.