Microelectronics: Devices to circuits
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Lecture 36: MOS Differential Amplifiers

Hello everybody and welcome to the NPTEL online certification course on Microelectronics Devices to Circuits. We start from where we left in the previous module. We had initially done the work on MOS differential amplifier and we saw that the overall gain of an amplifier depends on the value of your transconductance of the driver transistor and the drain resistance.

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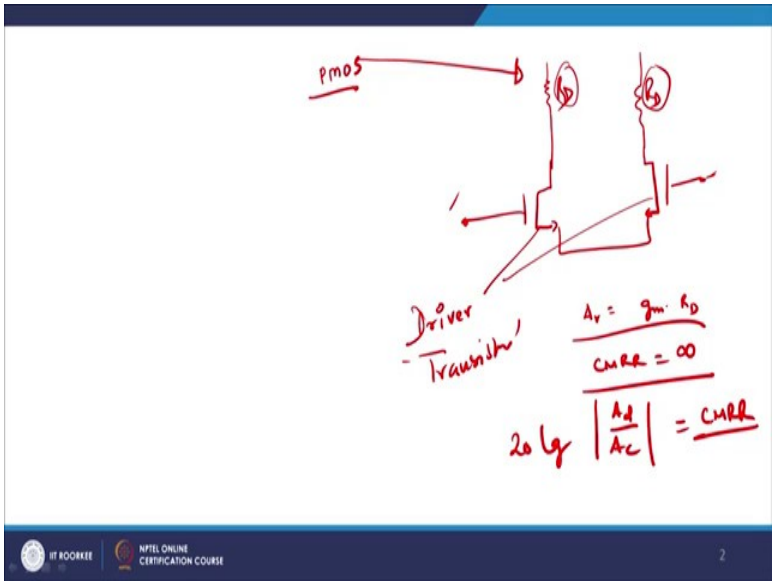

So if we, if we discuss the previous term what we saw was that if you, wherever you are giving the input, please understand, wherever you are giving the input voltages this is the input voltage right this one, this one, these transistors are known as driver transistors, right. Further if you remember we had R_D here which is the drain resistance right R_D, this is the R_D value.

But in reality when you do it on IC or on a chip when you want to fabricate it this resistance is will be performed by MOS devices. Typically if we use a PMOS device here you have a larger resistance being offered at this particular point. So we will see as we move along a lot of how it works out, but typically you have learnt 2 things as the gain is given as g_m times R_D by CMRR is infinitely high because of the fact that you are A_d it is basically defined as the A_d by A_c right.

If you take in db then it will be 20 log of A_d by A_c and this is equals to your CMRR, right and this is typically very high quantity which you get, approximately 10 to the power 5 or 6, ideally this should be infinitely large. What we will do today is we will actually look into MOS differential amplifier part 2 where we will be actually replacing those R_D the drain resistances by the typical PMOS.

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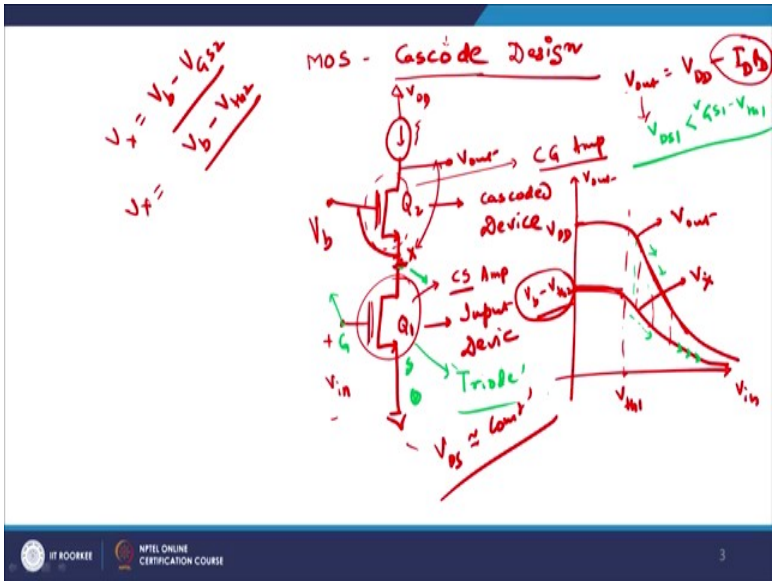

Before we go there let me just do one more amplifier design. That is known as MOS CASCODE design, please understand it is not cascade it is CASCODE, right, so you have a O here, CASCODE design, right, you have a MOS CASCODE design. So, let me draw for you how, this is but please understand this is we are slightly moving away from differential amplifiers. Differential amplifiers, you are feeding signals in a differential fashion to both the inputs of the gate.

Here, it is single stage amplifier it is not a differential stage, so, but, we will see what the advantage of it is as far as designing is concerned. So we apply at voltage source or current source here and then there is (03:03) V_{DD}, right and then, what we do is, this is quite interesting, that this is Q1 this is Q2 and this is plus minus V_{in} we apply the voltage here V_{in} and we apply a fixed bias here V_b, this Q2 is known as the CASCODED device and this is your input device, you are feeding the input to this and you are taking the output from here, right.

Now, you see this is if you look very carefully this Q1 is basically a common source a design, so this is a Common Source (CS) amplifier, whereas this one if you look very carefully is basically a Common Gate (CG) amplifier, so when common source amplifier and common gate amplifier are stuck together or they are made together, then we defined that to be as a CASCODED amplifier, right.

So what is a CASCODED amplifier you have a common source amplifier you have a common gate amplifier and when they are, when they are, when they are attached like this such a manner that the source of one is connected to the drain of the common source and then we define that as to be a CASCODED, CASCODED case. Now, if I, if I try to plot the V_{out} versus the V_{in} to get the transfer characteristics curve here. Right let us suppose this point is x, right, then if I this is V_{out}, then I get something like this.

This is your V_{th1}, this is V_{dd}, right, and this is V_b minus I will explain to you, V_{th2}. If you see as my V_{in} happens to be very low, right, when my V_{in} is very, very low I can safely say that my Q1 is cut off, right. So, I am just finding out the voltage at this particular point. Then if this is cut off, which is in the off state, if this is the V_{in} is very, very low in the off state then you automatically get what that, this is for, this is for, sorry this is for, this is for V_{out} here and this is V_x, so V_x is plotted in this manner and V_{out}.

So let us look at V_{out} first, when Vin is very very low, right, as I discussed with you, you can safely assume that Q1 will be cut off and therefore even whatever be the case V_{out} will be lashed to V_{dd}, because you do not have any current flowing through the system and therefore V_{out} will be latched to V_{dd}. As you start to increase your V_{in}, as you start to increase your V_{in} you draw current from Q1, because this is the threshold voltage of the device.

Till V_{th1} the output will be latched to V_b minus V_{th2} what is V_b, V_b is this much, V_{th2} is the threshold voltage of this device. So remember your V_{GS} minus V_{th} was the overdrive, right. So, so this if you look very carefully, this potential here will be nothing but V_b minus V_{th2}, right. So this is your, this is your V_{GS2}, right. So if you look very carefully V_x will be nothing but V_b minus V_{GS2}.

But, for the device to be on V_{GS2} will be typically equals to V_{th}, so V_b minus V_{th2} will be the value of V_x, and that is what you are getting here. Till a point, till what point, till the point when the input voltage is just crosses the threshold voltage of the device, which device the common source device which is the Q1 value. As it just crosses the device which is on and

both the currents, and the currents starts to flow through Q1 and Q2 because they are in series. And as it starts to flow the voltage at output starts to fall because V_{out} will be referred to as V_{DD} minus IDRD, say it is the resistance is also here available with you.

So when I_D, so initially what was happening I_D was 0, so you had what this was 0 and therefore V_{out} was equals to V_{DD}. Now, when the I_D starts to flow the V_{out} starts to fall down and that is what is falling down here, right. Similarly, your V_x will also since your V_{out} is falling, your V_x has to also fall, so that V_{DS} between this and this of Q2, V_{DS} of Q2 is almost constant. And therefore you see it is almost the same drop is there between the two initially, initially when the V_{in} is relatively just larger then V_{th1}, right.

I will just explain to you once again what I just not talked about it, what I talked about it is initially when your V_{in} is very low less than threshold voltage device, Q1 is in the cut off mode, when Q1 is cut off mode no current is flowing through this CASCODE structure as a result what will happen is your I_D will be equals to 0, therefore your V_{out} will be latched out to V_{DD}, standard case and your V_x will be equals to V_b minus V_{th2}. And we explained why it should be like that, it should be V_b minus V_{GS2}, but V_{GS2} equals to V_{th2} because that is the on state of the device and therefore that is the overall voltage which you will get here.

Now, as the input voltage crosses threshold voltage of the first device, the device gets on current starts to flow and when the current starts to flow through Q1 it the same current flows through Q2, and therefore the V_{out} starts to fall down, right, and therefore the V_{out} starts to fall down, as I discussed with you just now, the V_{out} starts to fall down, so V_{out} will fall down as you can see.

But as the V_{out} falls down you, you have to ensure that Q2 is in saturation and therefore V_x also starts to fall down and the difference almost remains the same till few values of Q_h. As V_{in} further goes on increasing, Vin further goes on increasing this value goes on still further increasing, right, as it goes on increasing, this is, this is basically a gate and source, right. And this is always grounded.

So, V_{GS} is becoming very, very large which primarily means its over drive is increasing, current is increasing, as a current increases then it forces this voltage to further go down, so that is the reason it is going down and down, right. Ensure it at one point of time it might also happen that V_{DS} of 1 might be even smaller then V_{GS} of 1 minus V_{th} of 1 and forcing the Q1 to enter into triode region, fine.

So, so what I wanted to tell you from this whole, whole, whole idea is that by doing so there is a problem here that common source if you remember was very good amplifier and common gate was a very good a impedance matching purposes. So CASCODE structure helps you to do both of them together that it helps you to match the impedances as well as gives you a improved gain with the with much better gain available to you.

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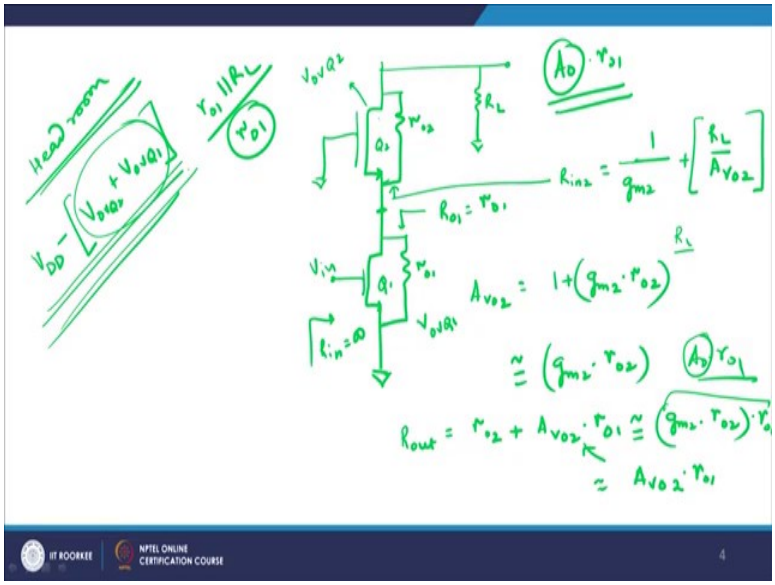

So if I draw the impedance diagram here or if we draw the small signal diagram here and external load is R_L and let us suppose Q2 is the input current and Q1 is the driver CASCODED current, then R_{01} and R_{02} are basically the, the resistances offered by those devices, if I assume this is Q2, if I assume this is Q1 and then I am giving a voltage here V_{in}. So if you look from this side, Rin will obviously be equal to infinity, fine. And, and if you from therefore if you look from this side affectively value of R01 will be equals to R_{01}. So from this point if you want to look inside affective resistance offered will be equals to R_{01}. I think I need not to explain it to you why is it like that.

Similarly, if you look from this side, right, and that is quite interesting then R_{in2} resistance, input resistance of this one will be from source side, is 1 by g_{m2}, right plus R_L by A_{V02} I will explain to you what do I mean by that. If you remember the whole discussion was that even by inspection also you can predict the value of input impedance, how did you do that just look from the source side and from the source side if a the input impedance will be 1 by transconductance of the device, so that is what we have written here 1 by g_{m2} and if you why do you add this R_L plus A_{V0} because A_{V0} is basically the voltage gain right.

Now, so if you divide R_L by the effective voltage gain I get the input impedance at particular point because R_L is the external load resistance which you see, which you see here, right. A_{V02}, A_{V02} which is the open circuit voltage gain of the second transistor the common gate one is given as the 1 plus g_{m2} multiplied by r_{02}, right. Now, of course this could be approximately return as g_{m2} into r_{02}, the reason being that a g_{m2} into r_{02} is much larger then 1 and therefore A_{V0} is equal to g_{m2} into r_{02}. Why g_{m2} into r_{02} very straightforward $g_m r_d$, so r_d is the resistance offered by the device g_m is the transconductance of the device.

Now, if you find out R_{out} and I am not deriving it, it here lot of scope it will be given as r_{02} plus A_{V02} into r_{01} and if you find out this will come out to be g_{m2} into r_{02}, right, into r_{01} and this is nothing but A_{V02} into r_{01} which we just found out here, right, A_0 into r_{01}. So if you look very carefully on this profile here what does it tell me that the output impedance is raised by a factor of A0, so suppose, suppose you did not have any CASCODE, you did not have any CASCODE device Q2 was not there, then I would have seen r_{01} parallel to R_L now since R_L is very very large as compared to r_{01} the output impedance would have been r_{01}.

Now, when you place a transistor Q2 CASCODED over Q1 you actually increase the impedance by a factor of A_0, where A_0 is the gain of my Q2, so you multiply this with r_{01} to get the overall gain R_{out}. So CASCODE structures, so CASCODE structures improves the gain by a factor of A_0 into r_{01} and, and gives you a very large value of your output gain, right. So this is a, a brief introduction or a structure of, of CASCODED structures, right, and we will revisit this maybe at a later stage, when we come back. Two things to take away from this discussion on CASCODED important for impedance matching as well as for high gain.

The cost we pay for it is that now you have 2 transistors in CASCODE therefore if you look at this very carefully this will be $V_{overlap}$, overlap, sorry $V_{overlap}$ Q2, and this will be $V_{overlap}$ Q1. So the available headroom for me will be, will be affectively equals to if you look very carefully will be V_{DD} minus right, $V_{overlap}$ Q2 plus $V_{overlap}$ Q1, right. So this is the available headroom to you in the, in the output side. Which means that if you want the gain to be high for the CASCODED structure you end up having a reduced headroom, so this is basically the headroom, headroom associated with this, right.

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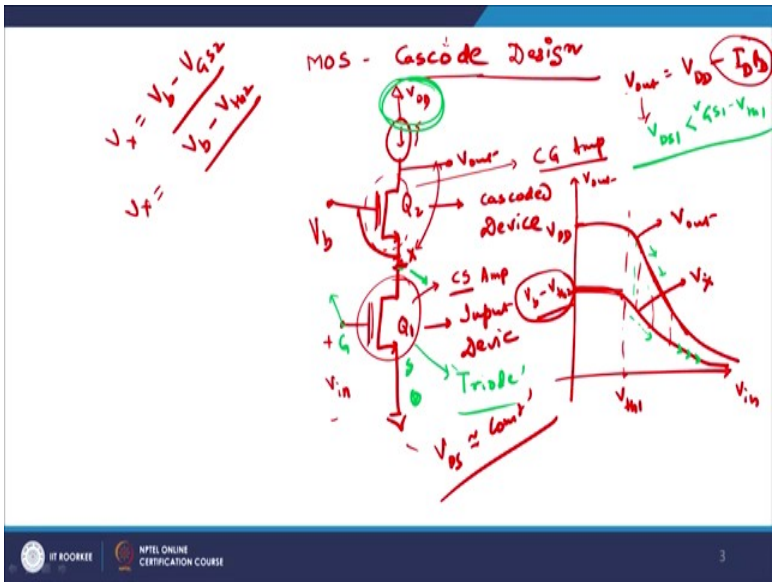

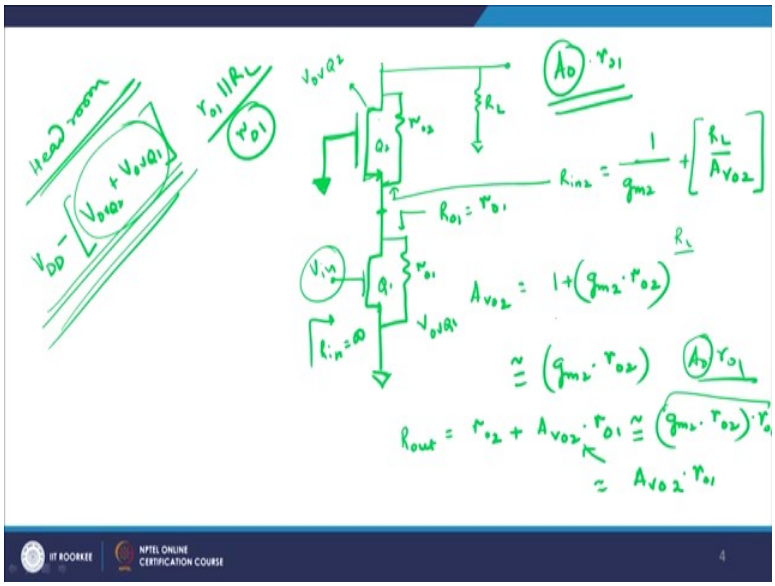

Which means that, so this is connected to so if you look very carefully, if you look at the, this was connected to the V_{DD} remember, connected to V_{DD}, which means that it is V_{DD} minus the sum of the over drives which you see. While looking at this point you please see that the while, while deriving this all quantity you please see that the base of the gate of Q2 has been grounded, right, whereas, I am giving an input signal to Q1, right, please find out why is it like that, why have we grounded Q2 and why we have taken out the signal through Q1 here in this case, right. This, this is to rather extent explains the overall features of CASCODED structures using MOS devices.

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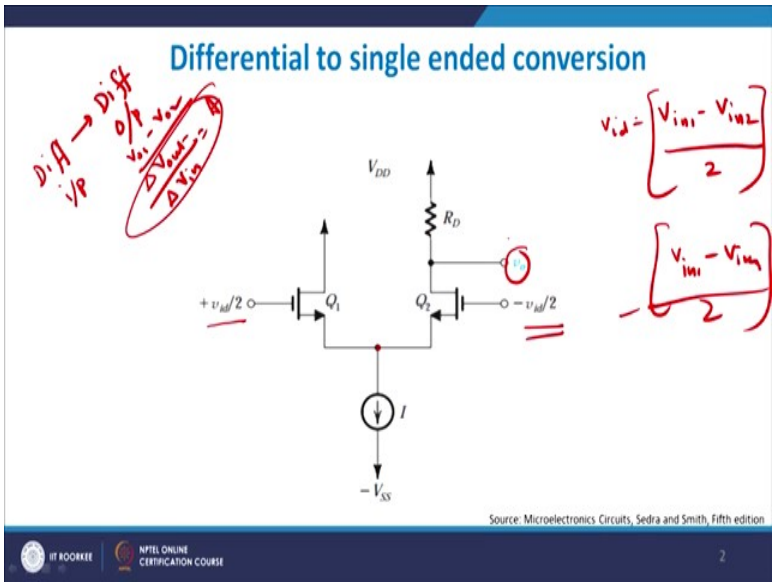

Let me come to the differential amplifier and let me see how can we change because till now we were what we are looking we were looking in the fact that we had a differential we had a differential 2 differential output. So, I have a differential input and I have a differential output and then what I was doing was I was subtracting V_{01} from V_{02} or vice-versa. And this is this was del V_{out} right and already I had del V_{in} and this was your overall gain which I solved. This is what we are doing till now, we also require to sometimes have a differential to single ended conversion.

So this is the diagram for that, that you apply signals here v_{id} by 2 so the difference divided by 2 plus and then the difference divide by 2 minus we already know what is v_{id}. So vid is basically v input 1 (v_{in1}) minus v input 2 (v_{in2}), let us suppose, so it is basically this by 2 on this side and then you apply v_{in1} minus v_{in2} by 2 with the negative sign on this side perfectly differential signals. As you may, as you mean infinitely high impedance. Then we find put the output impedance at this particular point V_0, right, and a straightforward way of saying that conversion of a high from a, from differential to single ended input.

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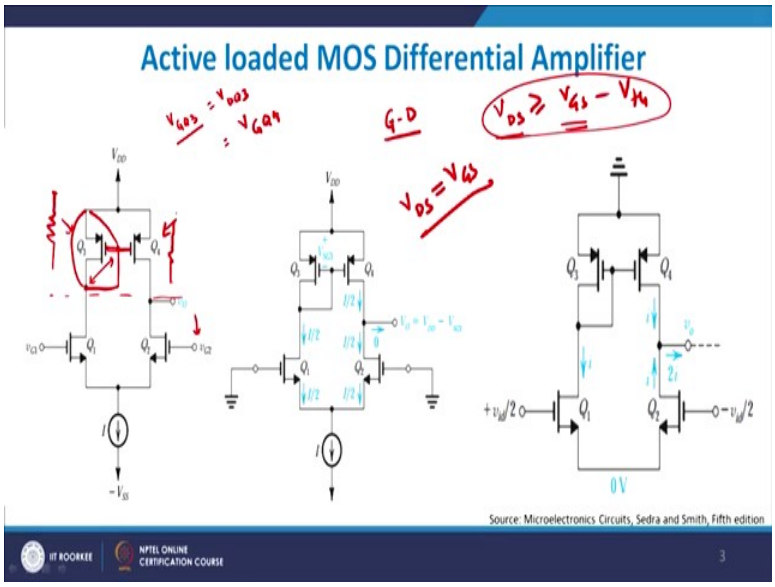

As I discussed with you in the previous turn, what we were doing was that we were, we need not to replace the R_D, the drain resistance by load, actual PMOS load. So what people thought was that let us apply PMOS load in place of R_D, the reason was PMOS is effectively having giving you a larger resistance because of lower mobility of holes, for the same dimensions of W by L. For the same aspect ratio the resistance offered PMOS will be 3 to 4 times larger as compared to NMOS of the same dimensions. So, if you look, this is exactly the same this below side is exactly the same if you look at the top, R_D is replaced by Q3 and Q4, right, and these are PMOSs.

And quite interesting what we have done one thing is that we have connected the gate of Q3 to the drain of Q3. So, now if you say V_{GQ3} right is exactly equals to V_{DQ3}, right. So gate of, gate of Q3 and drain of Q3 are exactly the same which is also equals to V_{gate} of Q4 (V_{GQ4}), which means that now, gate to source of Q3 and gate to source of Q4 is exactly the same. If I join these 2 then it ensures that gate to source of Q3 and gate to source of Q4 are exactly same which means that, which means that if I assume that Q3 and Q4 are perfectly symmetrical their over drives and resistance will also be equal to each other.

What happens when we join the drain to the gate side of it, right? When you join drain to gate you ensure that the device is basically moving in to a saturation mode and behaving like a resistor, right. If you, if you short gate and drain this is the reason the reason being, remember what was the reason V_{DS} should be greater than equal to V_{GS} minus V_{th}, right. Now, V_{DS} is this

much, V_{DS} is this difference and V_{GS} is this difference. Now, if these 2 are equal then V_{DS} is always equal to V_{GS}.

V_{DS} drain to source will always be equal to V_{GS} get to source, agree, so drain to source will always be equal to get to source because your gate and drain have been shorted with respect to each other. Which ensures that which, which is quite interesting that which means that this condition can never be applicable which means that my device can never go into saturated region at all, right, but in triode region behaving like a resistor. So this can be replace by a simple resistors. If you look back since this is a symmetrical Q4 will also look like a resistor.

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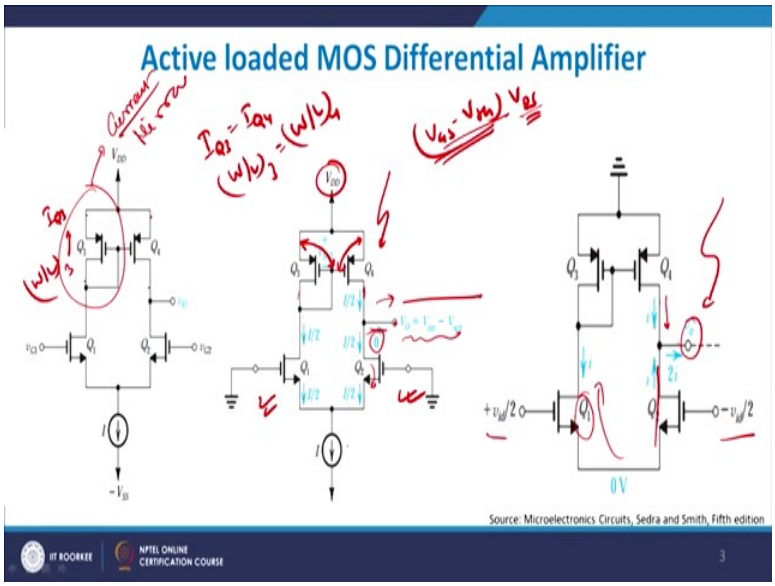

This action is basically known as current mirroring, this, this is known as current mirroring, because this, I will explain it to you later on maybe current mirror. The reason being that the current flowing through Q3 will be exact if the W by L ratios of Q3 and Q4 are same the current flowing through Q3, suppose this is I_{Q3} will be exactly equals to I_{Q4} provided W by L of Q3 is exactly equals to W by L of Q3 is exactly equals to W by L of Q4.

The same current will flow, why because remember current is depending on V_{GS} minus V_{th} whole square, right, it also depends upon the value of V_{DS}, if you, if you find out, in the triode region, if you are trying to find out, it depends on the value of V_{DS} is V_{GS} minus V_{th} multiplied by V_{DS}.

So if I am able to ensure over drive to be equal and V_{DS} to be equal and everything else taken care of my current will also equal, right. So if you look very closely this difference between

this point and this point will also be equal to the difference between this point and this point. And therefore V_{DS} will be also equal my over drive will be equal and therefore they will behave like exactly symmetrical structures.

With this knowledge let me say we have this structure available here, so I have, so I, so as I discussed with I have a current source I, it divides into I by 2 here, I by 2 here, so this is I by 2 here, since this is I by 2 as I discussed with you, you will obviously have I by 2 flowing here because it is a current mirroring action here. As a result the current flowing through these will approximately equals to 0 because all I by 2 have has to be routed through Q2, so the net current flowing here will be 0, so that is what is written here.

And therefore V_{out} will be equals to V_{dd} minus V_{GS3}, why, V_{dd} this voltage minus gate to source, source to gate this to this. So if you subtract this voltage or even if subtract this voltage I get the voltage available at this particular point (())(21:55) Kirchhoff's law. And as a result you will see this. This is for the case when both your Q1 and Q2 are either shorted or having equal dc bias.

Let us come to this point you will have differential voltage given, so I will have I, so this is minus V_d, minus V_d by 2 and this is plus V_d by 2 all current will be routed here. So this is the current flow here, so the other current flowing is here, so net current flow was I plus I 2I and therefore V_{out} will be having 2I available to you, right. So this is what you get from the, this active load.

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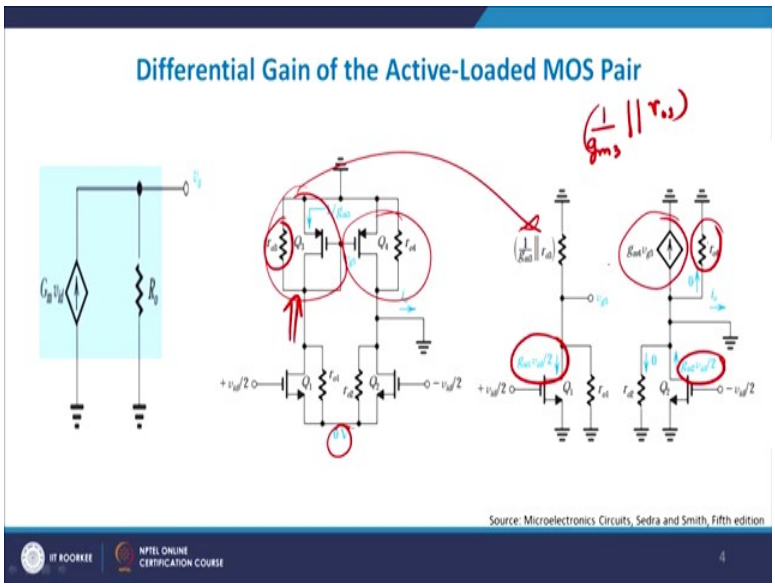

Now, therefore if you look here which is what I have done here is I have broken the Q3 Q4 Q1 & Q2 with the effective transient resistance. Where r_{01} is the drain to source resistance of Q1, r_{02} is the drain to source resistance of Q2, so are and so forth. And I have sort of grounded so 0 voltage is given to the input side to the source side, right. So I will assume that since it is 0 grounded any voltage above them with the threshold voltage of the device give to you gate side will switch on the device, right, switch on the device.

Now this is r_{03} and this is r_{04} and so on and so forth. So, if you look from if you look from this side towards this side the effective resistance offered will be r_{03} is parallel to Q3. And Q3 as I discussed with you if you look from the drain and source side the amount of is given by this, this is the resistance offered. So this resistance is in parallel to r_{03} and that is what I have written here. So this is replaced by this quantity, right. Whereas if you look where carefully at this one this is basically again a Q4 is basically a V_{CCS} a voltage control current source.

And therefore gm4 multiplied by V_{G3} is the value and R4 is therefore the, the resistance offered between the two, between the two. Assuming that this is the perfect current source I am assuming that there will be no current flowing through r_{04} as such, right. So what I see is, if v_{id} by 2 is the voltage given to the left arm and right arm and I can safely write down g_{m2} into v_{id} by 2 as the current flowing here, and gm by v_{id2} opposite direction current will be flowing here, right, and this is what we get.

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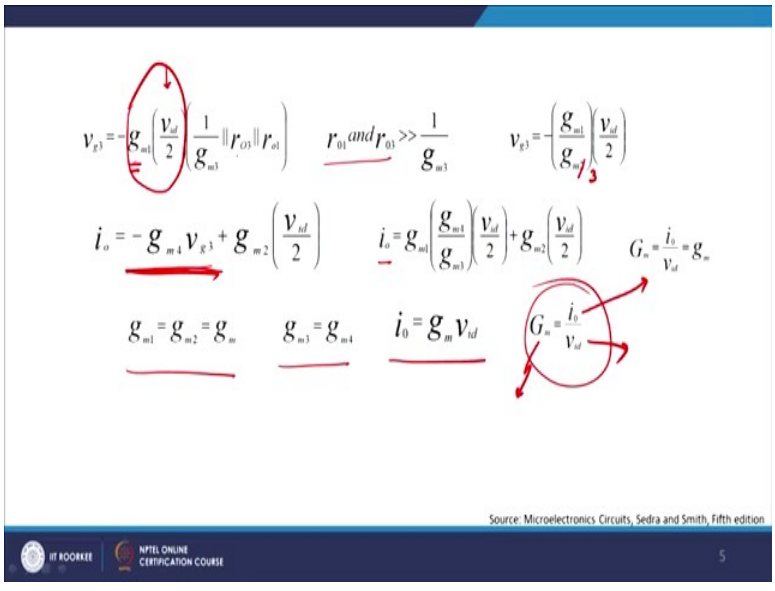

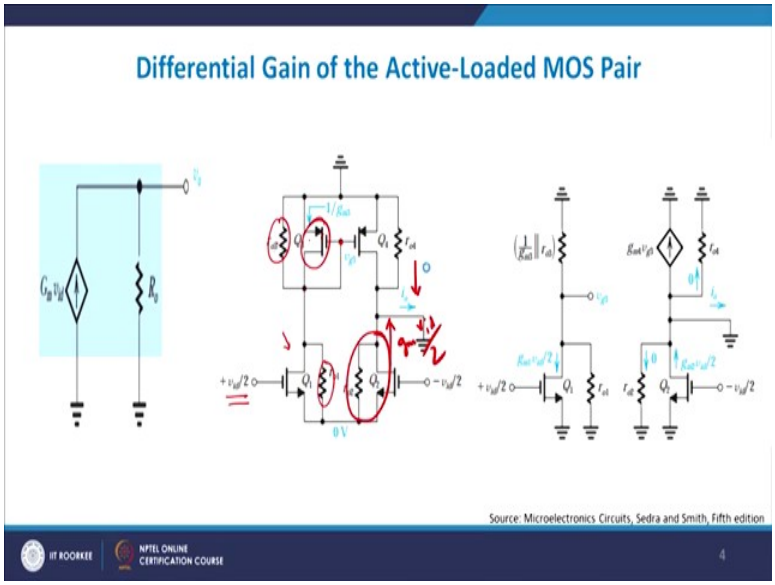

Now, let me come to the mathematics of it, so if you look very carefully V_{G3} and this will require some amount of flipping of the power point presentation, V_{G3} is minus gm times v_{id2} into the sole quantity. What is V_{G3}, V_{G3} is, let me rub this to make it clear, V_{G3} is nothing but the voltage at the gate of third transistor, right it is nothing but g_{m1} into v_{id} by 2, why it is g_{m1} into v_{id} by 2 see g_{m1} is the transconductance of Q1 into vid2 is the current which the transistor will allow it to flow, so the same current will flow to Q3, so that is the, sorry, so that is the Q3 current here right, I am sorry.

So I get g_{m1} into v_{id} by 2 is the current this if you multiply with the impedance that will give you the voltage, what is the impedance, impedance is nothing but 1 by g_{m3} because of this one and ro3 this one as well as r01 because you see this, this and this these 3 will be in parallel to each other. As well as you will get g_{m1} into v_{id2} into 1 by g_{m3} in parallel to r_{03}. Now r_{01} and r_{03} is much, much larger as compared to 1 by g_{m3}. So, what I can safely write now gm1 by g_m, g_{m1} by much larger then g_{m3}, sorry this will be gm3 I think, this will be g_{m3} so I will make a correction.

So g_{m1} by g_{m3} into vid by 2, right, now i_0, i_0 is the output current right, output current in g_{m4}, if you look very closely g_{m4} into V_{G3}, why, V_{G3} is the same voltage you are applying on to the fourth transistor Q4 right. So V_{G3} multiplied by g_{m4} is one component of the current and another component of the current is coming from this transistor g_{m2} multiplied by v_{id} by 2. So one current component is coming from here another is this one.

This one is g_m multiplied by v_{id} by 2 and this one is basically yours, sorry, this one is basically yours g_{m4} into V_{GS} by 3 with a negative sign, right. So if you do a small manipulation I get i_0 equals to g_{m1} into g_{m4} by g_{m3} into v_{id} by 2 plus g_{m2} v_{id} by 2, as you mean that g_{m1} and g_{m2} is equal to g_m and g_{m3} and g_{m4} are equal I can say i_0 is equal to g_m times iv.

And therefore capital G_m is equal to i_o by V_{id}, what is i_o, it is the output current, V_{id} is the input differential voltage and therefore I use a capital G_m, capital G_m is therefore the effective transconductance for the differential pair, fine, so capital G_m is the effective transconductance of the differential (())(27:04), whereas small gm is the transistor level transconductance, fine, so this is the difference between the two.

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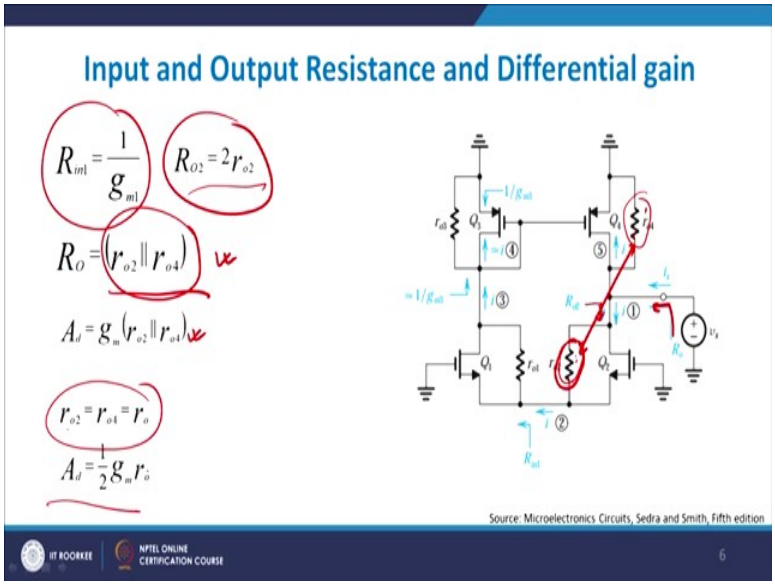

Let us look at the input and output resistance of the differential pair if you look input resistance will be given as 1 by g_{m1} we have already looked into the fact that, that input resistance given by here is g_{m1}, R_{02} will be 2 times r_{02} the reason being that if you look from this side, if you look from this side you have r_{01} coming from here, one resistance is coming from here and another one is basically coming from here, so they are equal and therefore assuming to be true.

And therefore, R0 though effective resistance seen at this particular point these two are in parallel, these two are in parallel and therefore I get r_{02} parallel to r_{03}, right. We will explain to you this why R_{02} is actually equals to $2r_{o2}$, r_{02} which is looking from this side you will have 2 times r_{02} right, and looking from this side you will have this these 2 in parallel that is what

you get here, and therefore the differential gain will be nothing but gm times r_{02} multiplied by r04 assuming r_{02} equals to r_{04} equals to equals to r_0. I can safely write down Ad to be equals to 1 by 2 g_m r_0, fine, because they are in parallel, write so this is what you get parallel.

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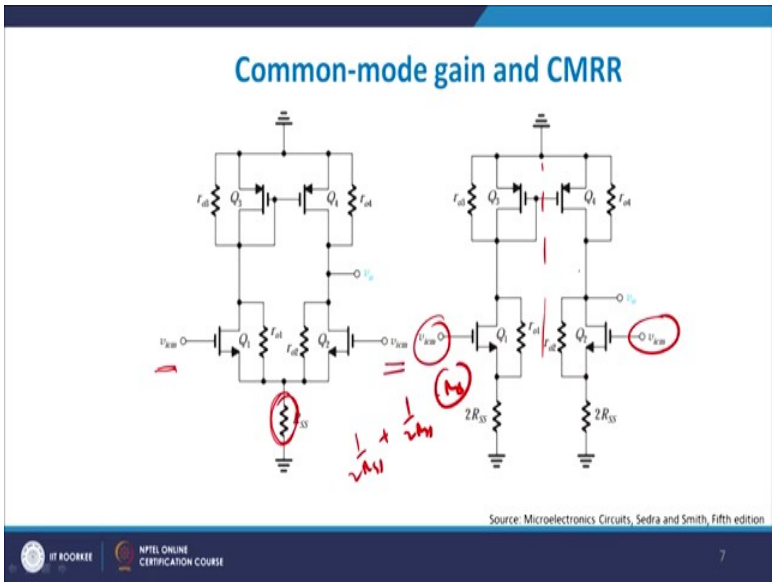

Now, we will look into common mode and differential gain so common mode gain if you remember what we did we inserted V_{icm} as the input mode voltage and I replace my current source by R_{ss}, R_{ss} is of the very large value of your resistances being offered here. It is a quite a large value of resistance because output impedance of the, of the current source will be typically very high. And then what we do, we do a half circuit realization and we divided into 2 parts and we give V_{cm} here, V_{cm} here and then this is parallel so 1 by 2 R_{ss} plus 1 by 2 R_{ss} will give you R_{ss} and that is the reason we divided into 2 parts and we just separate it out, right, for calculation purposes.

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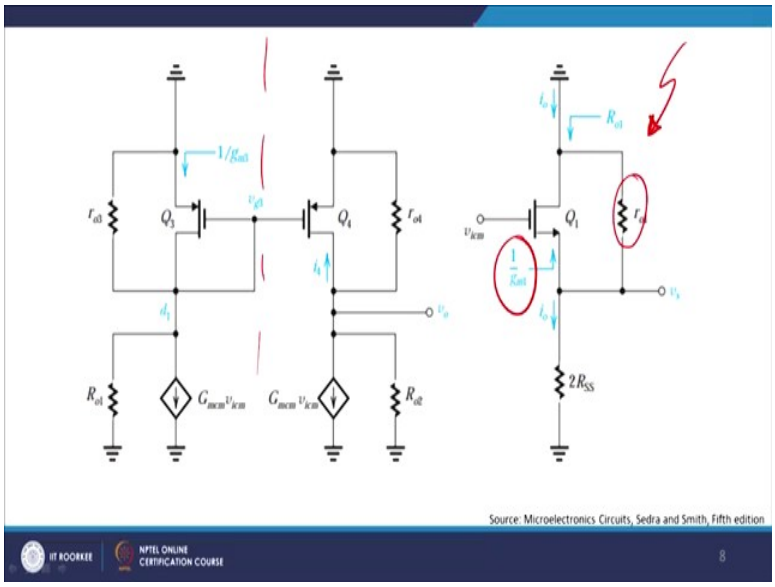

Similarly, when we look in to the, the overall transconductance features here so, so this basically one of the half circuits. This is one of the basically the half circuits. So if you look at the half circuit it is Q1 with 2 R_{ss} here and r_{01} as the drain to source resistance offered by this thing and therefore looking from the source side is 1 by G_{m1} is the effective resistance offered, offered by the device, right. So what we have done is that we have just broken up in to half circuit and explain it to you this basic idea.

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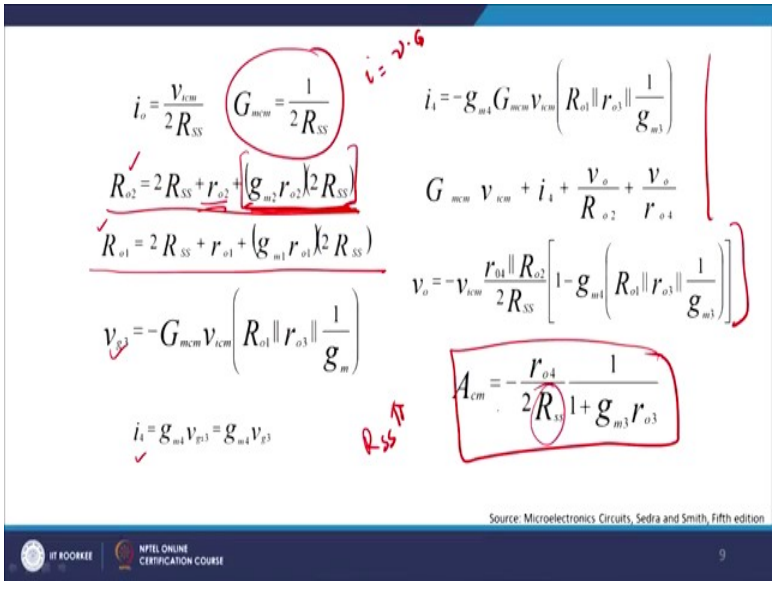

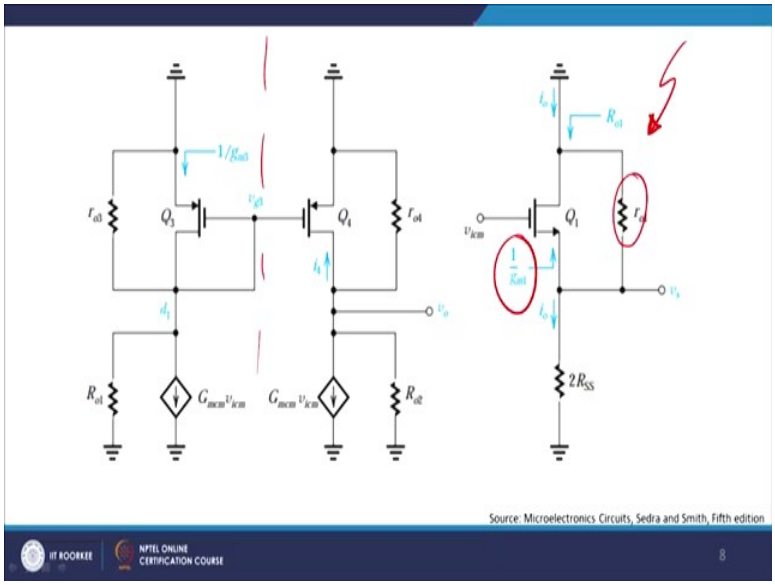

So, let me come to you and explain to you each one of them individually, so i0 will be equals to v, so i0 will be the output current is V_{icm}, why it is V_{icm}, V_{icm} is, V_{icm} is basically this V_{icm}, this divided by 2 at twice Rss because twice R_{ss} is the resistance offered by it, whereas, G_m, therefore G_m cm will be 1 by 2 R_{ss}, right because current is equals to G into so if you remember current will be equals to, therefore voltage into G, G is the transconductance.

And therefore, I can safely write down G_{2b} equals to 1 by 2 R_{ss}. R_{02} is given by this formula, R_{02} is the, R_{02} is basically the resistance at this particular point at Q2, this is r_{02}. Looking from this side this is R_{02}, right, R_{02} if you look at this is $2R_{ss}$ why $2R_{ss}$ because you will always have $2R_{ss}$ here, right you will have r_{02}, the resistance plus g_{m2} r_{02} into $2R_{ss}$, what is this quantity g_{m2} into r_{02} into $2R_{ss}$ into $2R_{ss}$ will give you the overall resistance offered by the device, right.

Similarly, R_{01} by symmetricity you will get this, similarly if you (multi) therefore, R_{01} and R_{02} are known to you, you can predict the value of i_4 and V_{g3} and from here, I will get common mode signal value to be equal to A_{cm} to be equals to this much. Please do it yourself these internal I am not doing it in the lecture module, but, please solve these yourselves to get these values and you will get r_{04} by by $2R_{ss}$ by 1.

So if you want your A_{cm} to be really, really small, right, keep your R_{ss} infinitely large and that is the reason why we require a almost an ideal current source here to make my R_{ss} as large as possible, right. That makes my A_{cm} very small and therefore by CMRR will also be very large.

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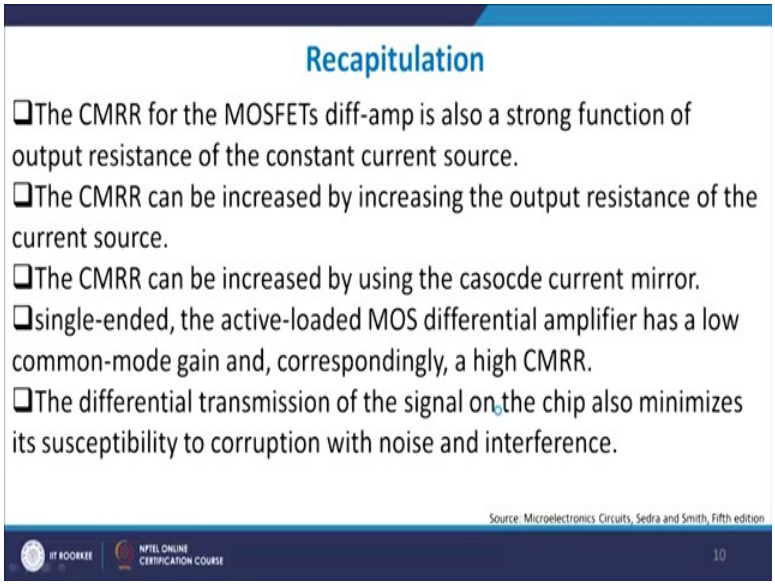

So, let me recapitulate what we did today in this, in this thing, the CMRR MOSFET is a strong function of output resistance we have seen that, and therefore, we have to ensure that it is a constant source or an ideal current source. How can you increase a CMRR by increasing the R_0 value that we have also seen in the previous discussion. If you use a CASCODED current mirror your CMRR will increase because your A_{cm} will decrease and A_d will increase.

We discussed that point today also that the differential voltage gain will be much higher in a CASCODED current mirror design. Then, the single ended active loaded MOS differential amplifier as a low common mode gain, and correspondingly high CMRR and the differential transmission of single on the chip also minimises the susceptible corruption with noise and interference. This is quite interesting the last one which take me that if you do have a chip in which you have got large impedances R_{out} is typically very large, it is actually a very good rejecter of noise also.

So noise resistance capabilities of differential amplifier is typically very high, we have already discussed this point, but not only because differential operation but because also of high impedance nodes in those devices, right. So with this we finish of this module and from next module we will take up another subject, right. Thank you very much.