Microelectronics: Devices to Circuits
Professor Sudeb Dasgupta
Department of Electronics and Communication Engineering
Indian Institute of Technology Roorkee
Lecture 35: MOS Differential Amplifiers 1

Hello everybody and welcome to the NPTEL online course on Microelectronics Devices to Circuits. In our previous module we have understood a differential amplifier implementation using a bipolar transistor and we saw that that differential amplifier has gotten an added advantage that it is a very good rejecter of common mode signals which means the signals which are common to both the inputs they will reject it and the differential signals are getting amplified.

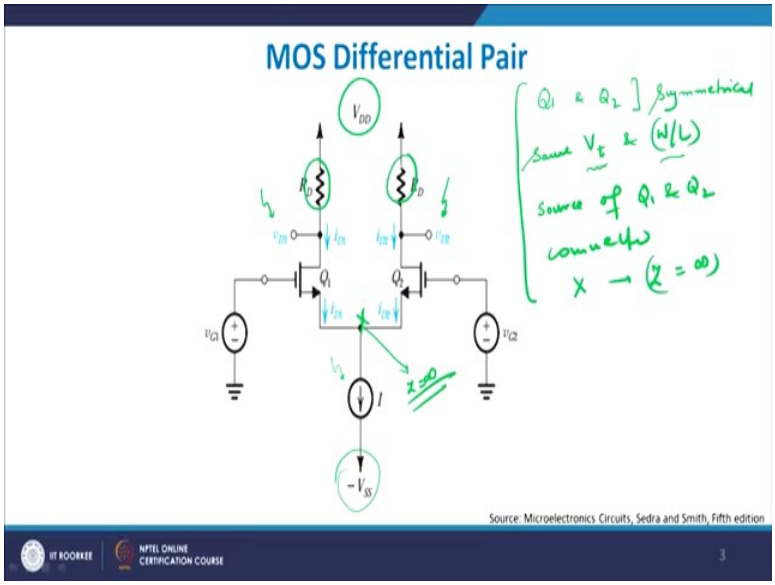
So as long as the signals are phase shifted with respect to each other by 180 degree. I would expect to see a large amplification taking place in the output whereas a common mode signal will relatively have almost 0 amplification and we also therefore, saw that common mode rejection ratio which is basically the differential gain upon the common mode gain A_{DM}/A_{CM} is actually infinitely large for a ideal differential amplifier.

So we also saw that it is commonly used for operational amplifier, the differential amplifier is the first stage in an operational amplifier where gain is where gain has to be very high. Of course, the price you have to pay for is, of course, higher power dissipations because you are working with current source, you are also working with three to two input devices and to load devices and so on and so forth. So, switching activity will be higher and therefore your power will be also very large.

We also saw in the previous discussion that you do not allow the device to go into the saturation mode, you let it go from active to cutoff and cut off to active, and the reason being when you put it into saturation mode and you want to move away from saturation mode you have to remove large amount of charge from the base side, and therefore, the time taken for you to switch from cutoff to active and vice versa will be relatively large.

So, therefore BJT switching speeds are relatively very high right but the loss which you get is a larger power dissipation, right. So what we will do today is have a look at most differential amplifiers so what we did in the previous turn was a BJT or a bipolar transistor based MOS amplifier, this time you will be looking into a CMOS or a MOSFET based amplifier.

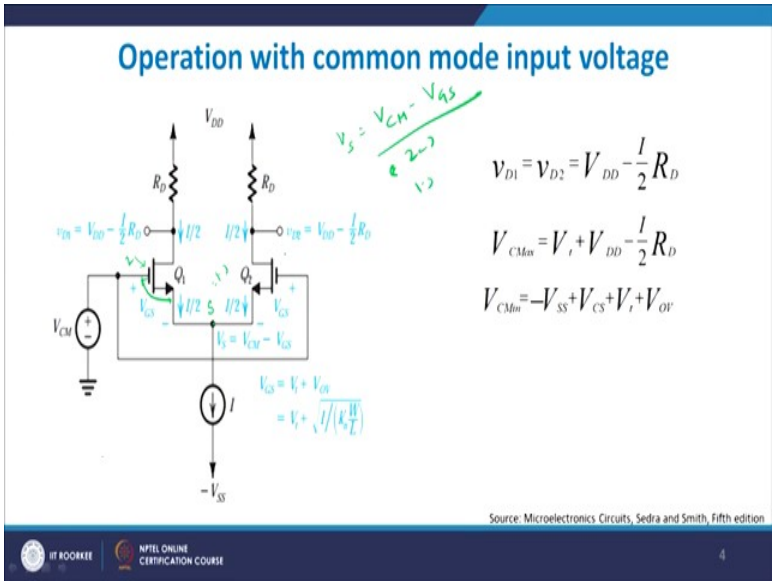
(Refer Slide Time: 3:06)



So the topic of this discussion is the outline of this slides of this module is we will first look at a MOS differential amplifier, just as we did for BJT we will first look at the common mode and then with differential input signals. We will look at the last signal operation and then we look into differential to single end conversion. We will look at active mode MOS differential amplifier we will also look into the active mode differential gain, and then look into input resistance, output resistance of a differential gain and then look at the CMRR and then finally we capitulate the whole thing right.

So, this will be the flow of today's lecture and so we will be first looking into a MOS as a differential pair. It is exactly the same like a BJT design, only thing is here only thing which you should remember at this stage is that when the gate voltage crosses a threshold voltage of the device, the device is in the on stage and it draws current from the power supply, so this is the only thing which is which is not there in a BJT. In a BJT you need to have we have your base voltage at least 0.7 larger than your source voltage for the base emitter voltage to be forward biased. Here you need the gate voltage to be at least larger than the threshold voltage of the device and therefore, that will ensure that you are into the active region of operation.

(Refer Slide Time: 4:29)



Let us look at the differential most differential pair so this is basically a small differential pair which you see this most differential pair is primarily made up of two transistors Q 1 right and Q 2 right and we are assuming that Q 1 and Q 2 are both symmetrical which means that they are exactly same having the same V_T and W / L right. So they have exactly the same threshold voltage and same aspect ratio and we applied two gate voltages V_{G1} plus V_{G2} are the two input signals.

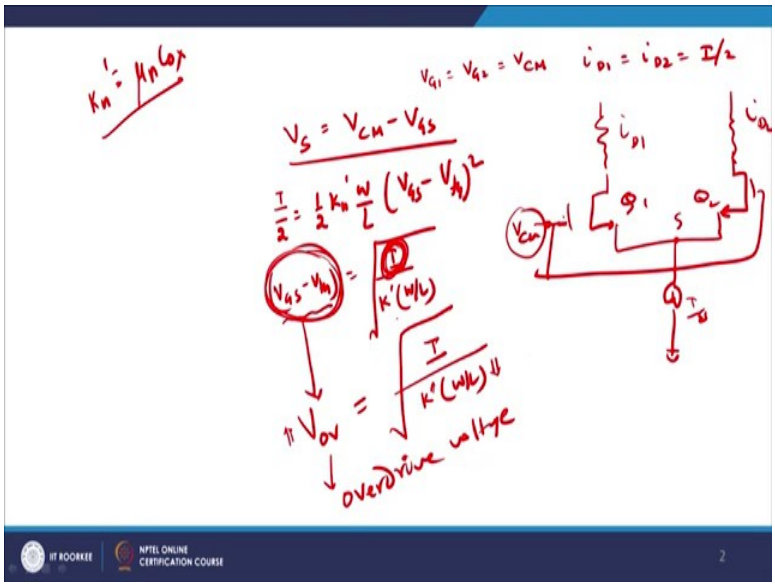
We also have a current source here I which is connected to a negative power supply minus VSS and this eye is basically current source which primarily meaning that this impedance here is typically very high. So, here if you want to find out the value of Z it will be approximately equals to infinity because it is terminating on a current source. We also have a load here Rd so there are two loads here R_d and you take two differential outputs V_D one is one differential output and V_D two is another differential output, right.

As I only discuss with you this potential let us suppose this we name it as X right X will obviously have the same potential and therefore so if you look very carefully the source of q1 and q2 are connected together so what we are doing is that the source of q1 and q2 are connected right the source of q1 and q2 are connected. And we can always say that that this part X right since its Z is equals to infinity high impedance node I can safely say that whatever current is flowing is basically by virtue of the charge carriers available in the MOS device right and that makes our life or calculation easy, relatively easy.

It is not connected to V_{DD} which is the basically the power supply and I have a here you have got that here I have got the source which is available here. Now, let me explain to you therefore with the knowledge with the basic concept or knowledge here let me give to you an idea about two things. Firstly, is that let us assume that you have a common mode operation so if you see here this is the common mode operation right so what we what we will be looking into is that up with common mode input voltage so if I have a common mode input voltage how does it work out.

So if you see here what I have given here is I have given an the V_{cm} is the common-mode voltage, a DC bias which is given here and I am giving a the same DC bias exactly at this particular point V_{CM}. So if you look it (trans) clearly V_{gs} will be nothing but V_{CM} – or this this protects oppose this this point is then vs will be equals to V_{CM} - V_{gs} right because if this is 2 volt V_{gs} is say 0.7 then 2 minus 0.7 is, 0.2 - 0.7 is 1.3 so as will be equals to 1.3 volts. So this is what we what we get from here.

(Refer Slide Time: 7:46)



With this knowledge we can write down therefore right we can write down that let us suppose V_{G1} equals to V_{G2} equals to V_{cm} right and therefore I_{D1} equals to I_{D2} equals to I / 2, i_{d1} and i_{d2} are basically the current flowing through. Let me draw for you the diagram here once again so this is the current which is there. This is Q1 Q2 and this is I_{D1} and I_{D2} is the current flowing through it and this is basically your Vcm which ever applied + V_{cm} here and same + V_{CM} is applied here and then you have a current source here which is basically i_{ss} and this is what you get.

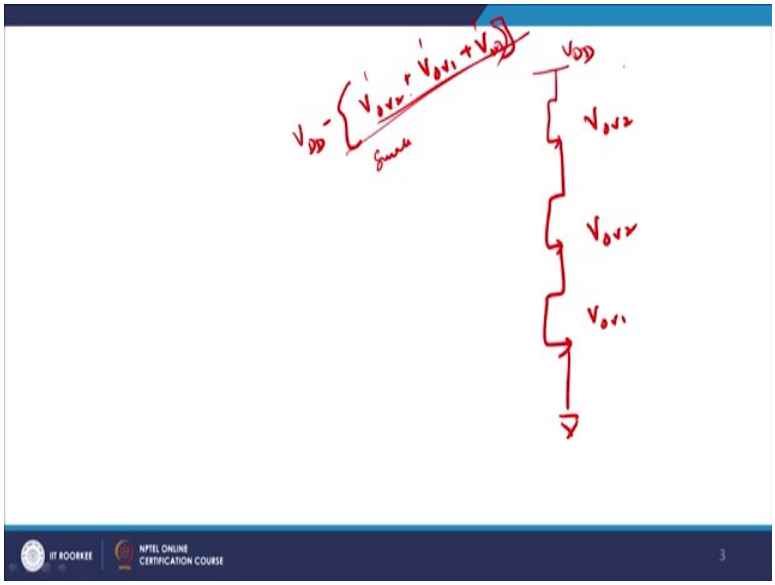
So if you if you this is point S, so I what I get is that V_s will be equals to V_{CM} - V_{GS} right so I can safely write down if I assume that Q 1 and Q 2 are perfectly symmetrical and I apply the same value of voltage V_{cm} to both both the base of the transistor here other gate of the transistor here then I can safely write down that I / 2 is equals to 1 / 2Kn' W / L (vgs – vth)^2 where K_N' is equal to mu * C oxide.

Fine, I get this into consideration and therefore I can write down vgs - vth to be approx. equal to by K' W/L which means and if you look very carefully this is nothing but $V_{overlap}$ so $V_{overlap}$ is overdrive sorry $V_{overdrive}$ is nothing but 1 / K (W / L). This is known as overdrive voltage in a MOS device. So what drive voltage is difference between the gate to source voltage and the threshold voltage of the device right and we define that to be as equals to I / K' * (W / L).

Which means that if you make it W / L small right please understand you make it overdrive large. Overdrive large means here V_{gs} - V_{th} is large implying that your current is large right which we so sorry your V_{gs} - V_{th} is large primarily meaning is a current is large but when your current is large you also therefore end up having a larger gain.

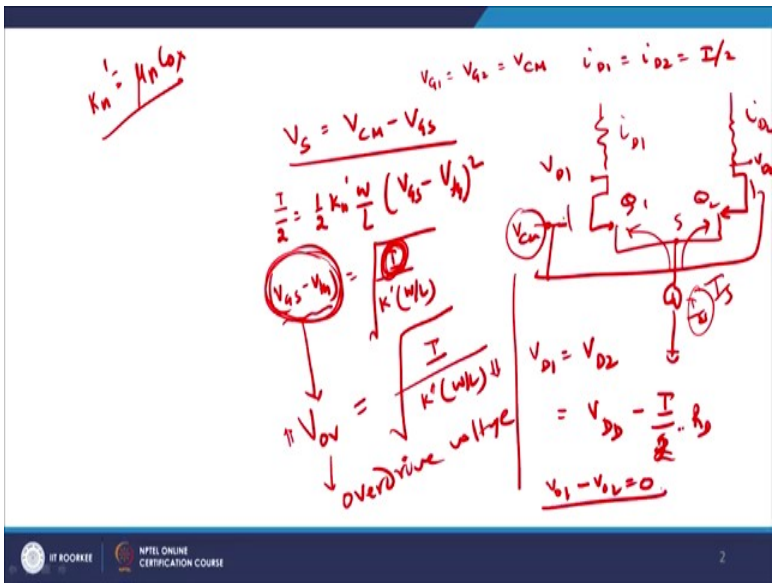
So that is how so what drive is related to gain in such a manner right we will see later on that this what is the drawback of such a scenario is that higher the overdrive is do again is high but your head rooms as I discussed in the previous turns is reduced right. So, if you have a stacked transistor each with head rooms of each with over drives of X Y then your overall head rooms will reduce by X plus y right. I will just try to explain to you what over drive mean to say by that.

(Refer Slide Time: 10:41)



Let us suppose I have got three transistors available here right and the three transistor this is grounded and this is $V_{overdrive1}$, $V_{overdrive}$ to and this $V_{overdrive3}$, then the available headroom at the top will be $V_{overdrive2}$ plus $V_{overdrive1}$ plus $V_{overdrive}$, sorry $V_{overdrive3}$. Which means that higher these values are because you want again to be high more these values will be and then 1 minus V_{DD} minus that quantity will be typically very small. So you will be not left with much room to play with either the near V_{DD} or near V_{SS} right and that's the price you pay typically for the purpose of design itself.

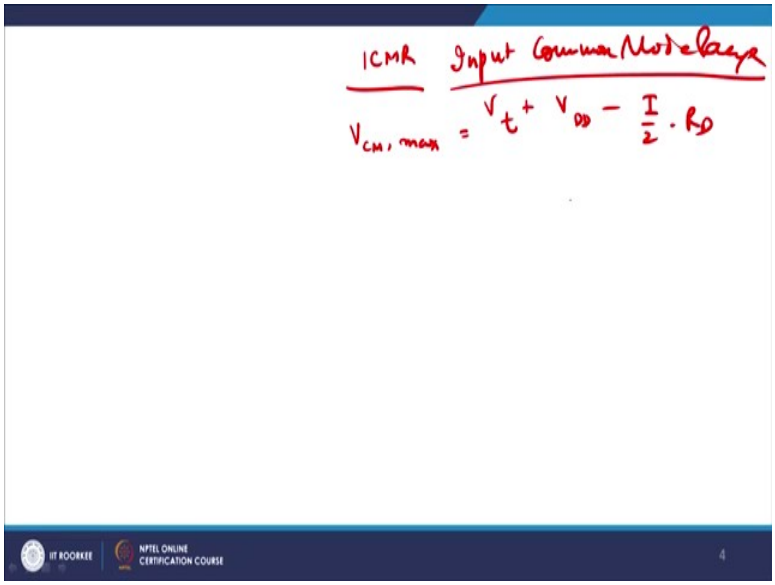
(Refer Slide Time: 11:31)



Therefore, what we can write down all these discussion is that I can write down so V_{D1} equals to V_{D2}, V_{D1} V_{D2} are where, this is V_{D1} right and this is V_{D2} right, so we do 1 equals to V_{D2} equals to V_{DD} minus I guess by 2 into R_D, understood why I_S by 2 because this is this is the total current is basically, Is so this will move to half on this side and half on this side, so I / 2 right, I / 2 , V_{DD} - I/2 * R_d this much is your V_{D1} and V_{D2}

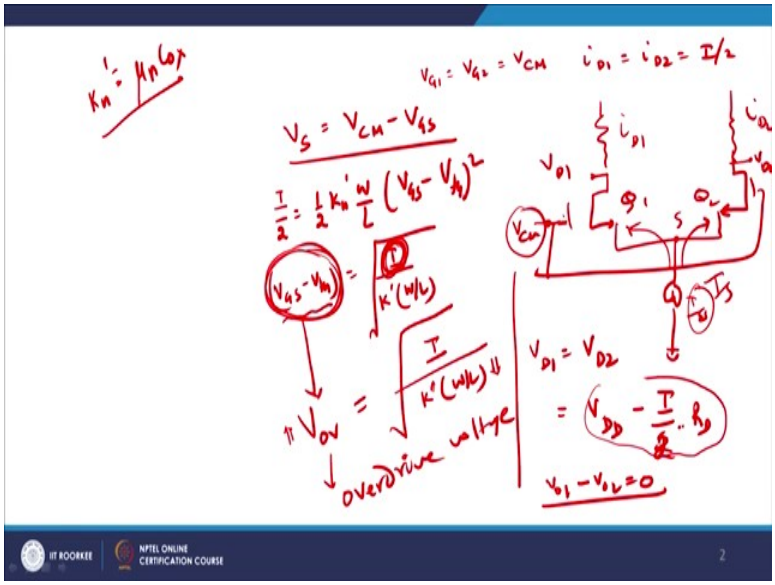
Now, if you since you've applied the same potential on the gate side of the MOS device which is basically V_{CM} therefore subtract V_{01} minus V_{02}, i will get 0 which means that if you have a perfectly equal signal being applied to the gate side of the input transistors you do not get any output available right and that is quite an interesting one.

(Refer Slide Time: 12:28)



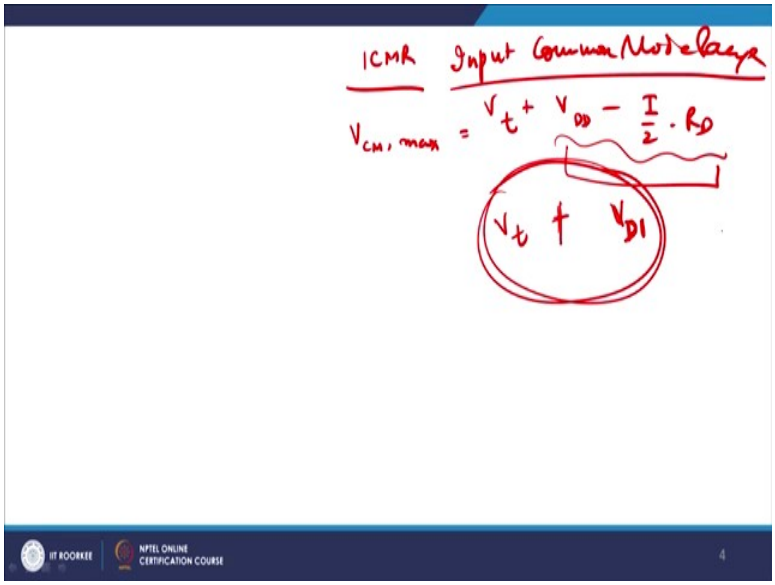
Let us look at therefore the ICMR which is also defined as input common mode range. The right and what do I mean by that I mean to say that what is therefore the minimum and the maximum value, so therefore, so I have applied, we see this, this is what I am trying to say that once you apply input, positive input voltage I need to figure out what is the maximum value of that input bias and what is the minimum value of that input bias right. So, that is my next aim as far as designing is concerned. The next time therefore if so we write down V_{cm} common mode max, which is the maximum value which you still get is V_T plus V_{DD} minus (I / 2) * Rd.

(Refer Slide Time: 13:24)



So if you go back to your previous discussion you saw that your the drain voltage which we are giving was V_{DD} - I / 2 * R_d right.

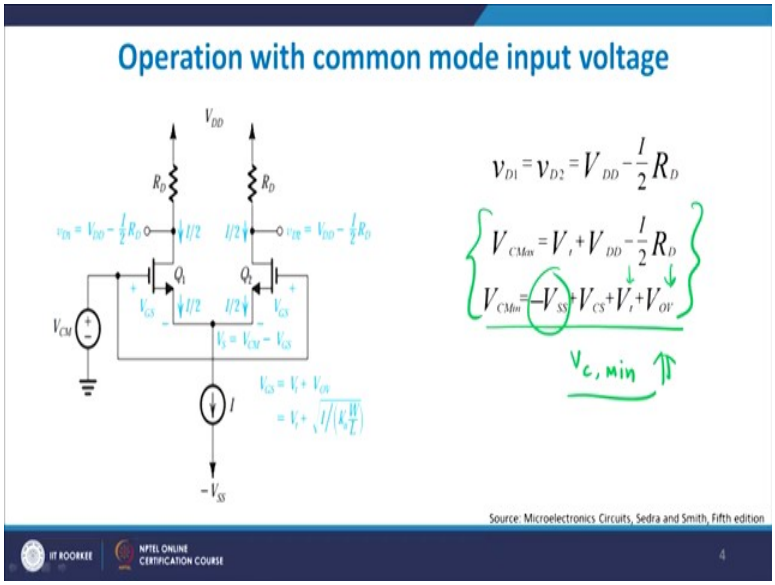
(Refer Slide Time: 13:35)



So it is V_{DD} minus so this is what you get so you get this this is what's the value of V_{D1} is right and we say V_{Tmax} - because this much why because you see when you apply a DC bias it should at least switch on the devices because if it doesn't switch on the device we will never be able to achieve the switching or we will never be able to steer the current to south to left arm or writer arm.

So you want the device to should get switched on. Now to get it switched on the minimum voltage required on the gate side is basically equal to the threshold voltage which is V_T and that is the reason I write V_T here. Plus the same DC bias should able to give a particular value at the output side, of the drain side which is basically V_{D1}. So, until and unless you maintain a common mode DC bias of $V_T + V_{D1}$ right, $V_T + V_{D1}$ minimum value I will not be, V_{D1} is the output in the drain side, right, you will not be able to get this much amount of signal in the output nor you will be able to switch on the transistor fully right.

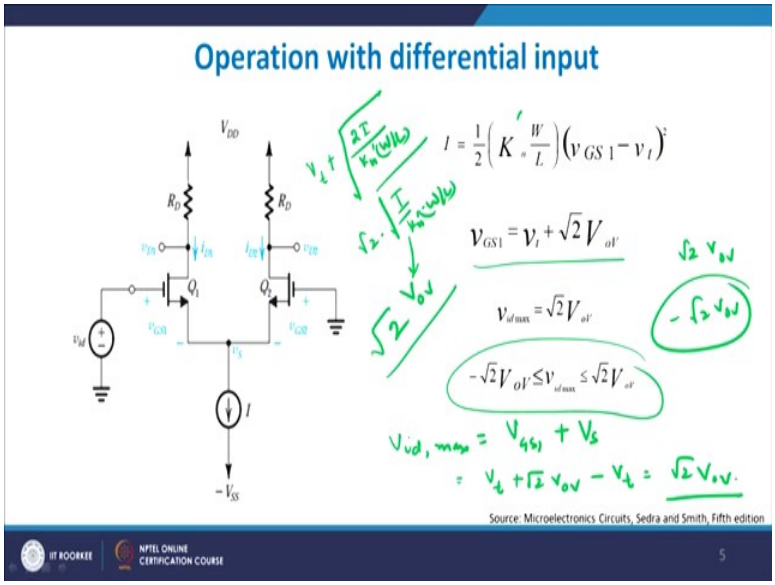
(Refer Slide Time: 14:41)



What is the minimum value which you see, the minimum value is given by this and therefore, you have to ensure that this minimum value which is equals to minus V_{ss} + V_{cs} + V_T + $V_{overlap}$, if anything, if the carbon mode signal goes below any one of them your it might be even true that the current source which we are using might be switched off right and therefore, I will not be able to get any amplification out of it and that is the reason you always apply a minus V_{SS} in the input side plus threshold voltage plus overlap voltage here for V_{CM} right.

So you see if I increase the value of $V_{overlap}$ going on increasing it the price I pay is that my V_{cmin} is actually going high right and that is where pretty difficulty should cover because I want my overall up to be high for my gain to be high but once my gain is high, my overlap is high my common mode signal minimum also starts to become higher. So, I cannot play with large amount of DC biases I_C bias is the input side for a longer duration of time right. So this is what we have done or what we have understood from this basic implication.

(Refer Slide Time: 16:00)

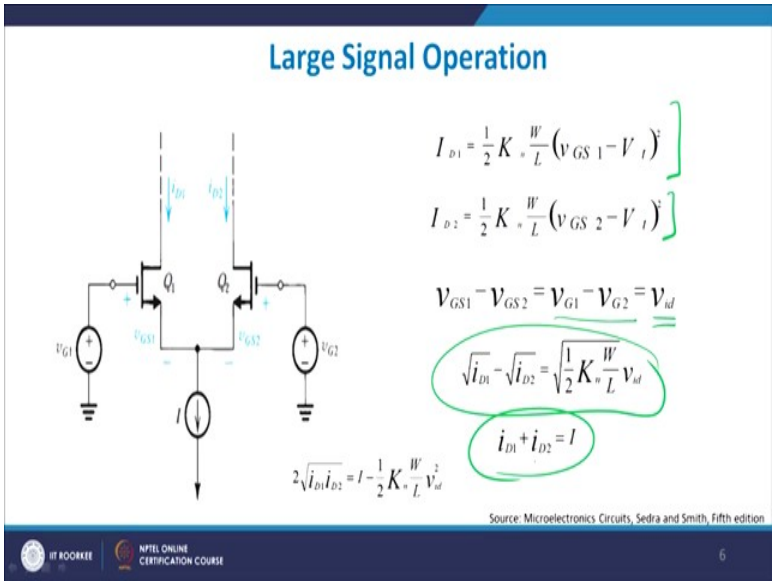


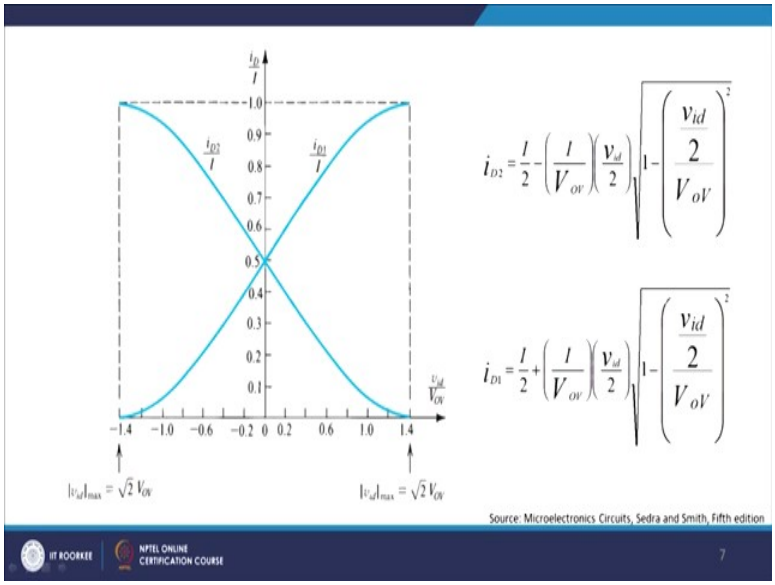
Let me come to the differential mode of operation. The device so as I discussed with you current will be equals to 1 by 2 K_N' , this is(K_N' * W / L) * $(Vgs1 - Vth)^2$ right. So, if you find out Vgs1 it will be Vt + root(2) Voverlap, why Voverlap because shall tell you. If you if you solve it you solve it I get V_T + root (2i / K_N' * (W / L)) and then if you look very closely it is nothing but root (2)* root I / (K_N' * W / L) and this is nothing but Voverlap.

So it is root(2) * $V_{overlap}$ right. So, what I get from here is that my Vgs1 should be V_T + root $2V_{overlap}$ right and if I remember V_{idmax} differential voltage max should be equals to Vgs1 + V_s why this is true because gate to source is nothing but the applied common mode signal minus Vs so if you take V_s of the right hand side it becomes plus V_s so they get V_{Gs1} plus Vs. So if you plot it I get V_T + root 2 $V_{overlap}$ - V_T and this comes out to be root 2 $V_{overlap}$ right, and therefore the minimum and maximum value of V_{ID} is just root (2) $V_{overlap}$ in the positive side and minus root (2) Voverlap at the negative side.

Which means that if my V_{IDmax} goes beyond root 2 $V_{overlap}$, it goes beyond VD root (2) $V_{overlap}$ then I might enter into a nonlinear region of operation of the device right and as a result I might even intend to try out digit of operation and there will be heavy non-linearity associated with the device. So, I restrict myself to root (2) $V_{overlap}$ both sides negative and positive right and that is a quite an interesting formulation which we see.

(Refer Slide Time: 18:14)



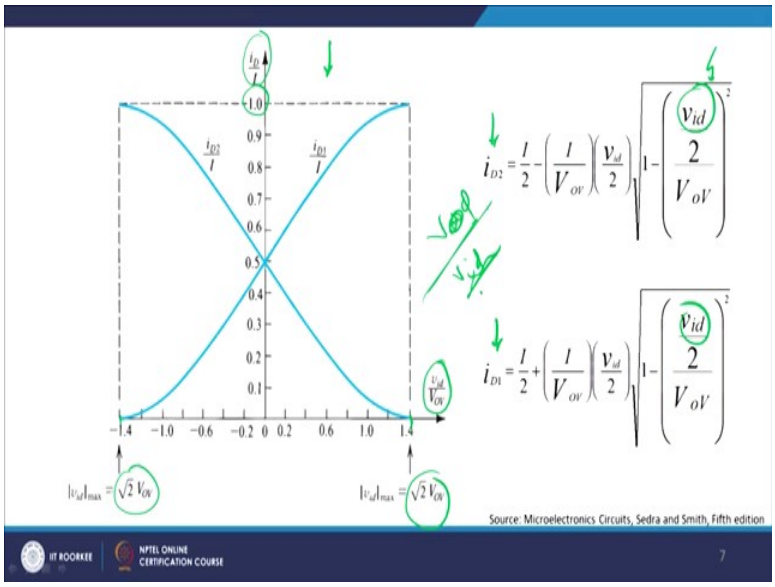


Now with this knowledge which you have gained till now we will do a small not signal analysis here and last signal analysis is required that we have both the transistors here q1 and q2 they are charged with an external voltage source of V_{G1} and V_{G2} and there is a current source here which is basically behaving like an ideal current source, which is giving a current I, right.

And, therefore, I can safely write down that I_{D1}, I can write down so I get yes this I_{D1} equals to 1 / 2 k_N W / L (V_{GS1} - V_T) and I_{D2} is nothing but (V_{GS2} – V_T), right, so if you subtract V_{GS1} V_{GS2}, I get V_{G1} - V_{G2} and that is equals to V_{ID}, because source voltage is common to both of

them. So, if I take square root of that I get this into consideration and I with the constraints that I_{D1} plus I_{D2} equals to I. We can safely write down I_{D1} I_{D2} as these quantities that I / 2 - I / $V_{overlap}$ $V_{I\,D}$ by 2 into this quantity and you have got another this quantity here.

(Refer Slide Time: 19:21)



Now you see quite interestingly that I_D both the currents $I_{D\,1}$ I will come to this graph later on but look at both the currents with the currents as such now if you look if we look at both the currents then $I_{D\,2}$ and $I_{D\,1}$ both are basically a function of V_{ID}^2 right and that makes my gain which gain will be obviously $V_{I\,D}$ by sorry $V_{I\,D}$ which is the sorry $V_{\,OD}$ / V_{ID} V_{OD} is the output difference voltage divided by input difference voltage.

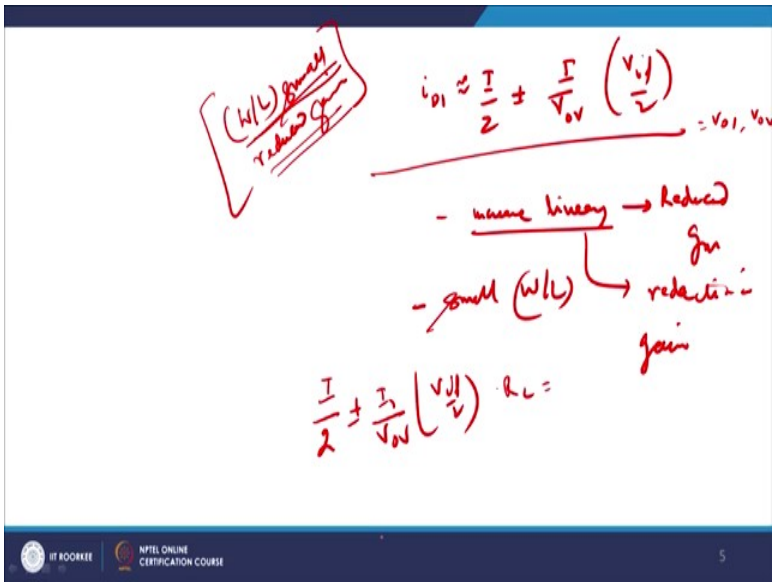
But you see the currents $I_{D\,1}$ and $I_{D\,2}$ are by itself nonlinear function of V_{ID} because V_{ID}^2 is here right, so it will be a parabolic term which will be there and therefore, $I_{D\,1}$ and $I_{D\,2}$ will not be a linear function of V_{ID} but will have a nonlinear term because it's square tower a parabolic term available here.

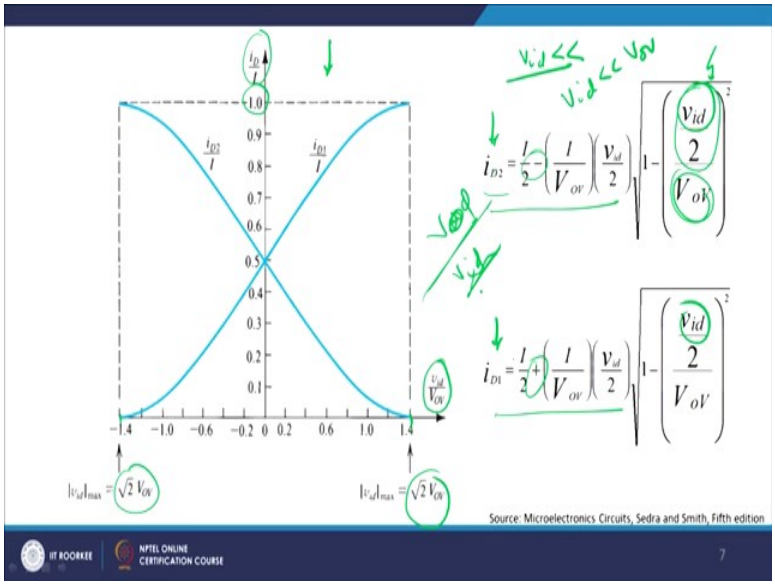
So with this knowledge if you just look at this graph which you see in front of you so you see I have plotted exactly like the previous turn we have plotted I_D / I on the y axis and we have plotted V_{ID} / $V_{overlap}$ on the x axis right this V_{ID} by $V_{overlap}$ and that is I_D / I and on the y axis and of course as I discussed with you I_d even maximum value of I_D will be equals to I and therefore I_D by I will always be equals to 1 and that's the reason a maximum I am going is plus 1, right.

And as I discussed with you that that my V_{IDmax} can go up to my maximum root (2) $V_{overlap}$ and minimum minus root(2) $V_{overlap}$ so I am restricting myself to this this 1.4 here and 1.4 here just a numerical value, do not worry about it, that is a numerical value but this ensures to me that my V_{idmax} which is the difference voltage difference right, the voltage between the two difference is exactly this root (2) $V_{overlap}$ and therefore, you get the negative side due to $V_{overlap}$ out so at the negative side.

Now, so the whole idea is therefore to make this current independent of V_{ID}^2 term because square term introduces large amount of non-linearity right and you do not want to do that and that is the reason you somehow ever have to remove this V_{ID} we will see how to do that later on. But with this knowledge you have gained, with this knowledge which you have just seen here.

(Refer Slide Time: 21:52)





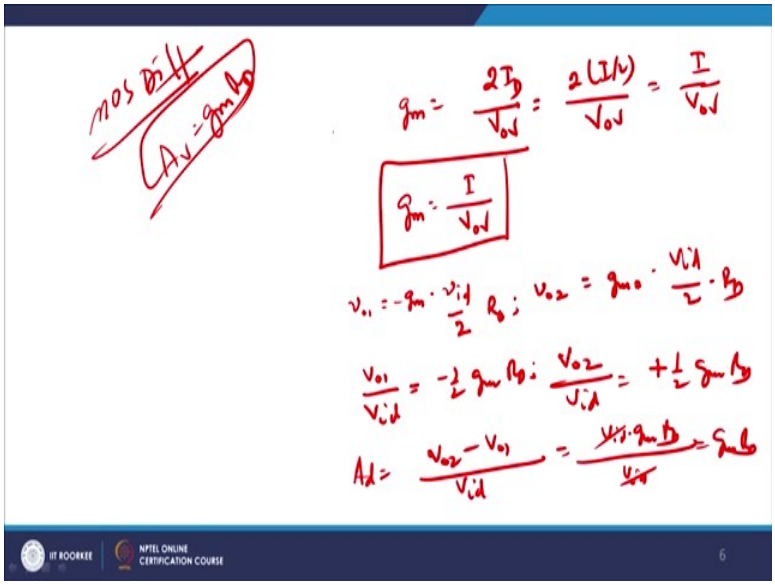
Let me write down for you certain statements and certainly issues that that I could write down that $I_{D\,1}$ therefore can be written as I / 2 +/- I / $V_{overlap}$ into V_{ID} / 2, V_{ID} / 2. Now, how it is V_{ID} by two, provided what I do is, I provided I make, if I make my V_{ID} much smaller as compared to other values then this square term will be very small as compared to $V_{overlap}$, so if I make my V_{ID} much smaller as compared to $V_{overlap}$ then this quantity will be very small and therefore 1 upon this will be typically very large and therefore this will be approximately goes to 0 and what I get will be $I_{D\,2}$ will be I / 2 - 1- I / Voverlap into V_{ID}/2 right, this is what we get, if I do $I_{D\,1}$ $I_{D\,1}$ will be therefore this was minus this will be plus, fine so I get $I_{D\,1}$ and $I_{D\,2}$ values with us here.

Now let me see what happens if we increase the linearity of this region right that is my job because as a designer I want that my linearity should be of larger range so that for a larger input voltage range my gain is almost independent of the input voltage right that is the major functionality of this this equation. So what we intend to do therefore is we take two or three important steps here to understand the basic features here and the first thing is that we if you want to increase linearity right you end up having little reduced transconductance.

And second thing is that you require a small W / L right so increase in linearity comes from a reduction in gain right, so we need to find out methodologies by which we can actually enhance the gain even with this this stage differential stage amplifier okay. So we required therefore, as I discussed with you since this this has come because $V_{I\,D}$ square is very small and therefore that can be neglected with respect to 1 and therefore I will be left with $I_{D\,1}$ equals to I / 2 +/- I / $V_{overlap}$ * V_i / 2 as the value of your V_{o1} right.

Now if you see $V_{o1} + V_{o2}$ because V_{o2} will be just minus of that, so when you want to add those 2 so I get I / 2 right plus minus $(I / V_{overlap}) * (V_{ID} / 2)$ right, this is the I_D value which you get, this if you multiply with R_L load resistance you get the overall voltage in the output side, so this will be V_o right. If I want to as I discussed with you if I want to improve the linearity of the system make your W / L small cost you pay is reduced in reduced gain right and not only it is give me will have other problems as well but W / L small prime facie will require a reduced gain right so even for a differential amplifier.

(Refer Slide Time: 25:13)



Let me therefore explain to you how a GM looks like, GM is defined as the transconductance is defined as to I_D by $V_{overlap}$. So, it will be to 2(I/2) / $V_{overlap}$ right, so this is nothing but to 2 2 will cancels $I / V_{overlap}$ right, so I get GM transconductance to be equals to $I / V_{overlap}$. Now, therefore I can write down V_{01} to be equal to g_m times minus g_m times $V_{I D}$ by 2 into R_d and V_{01} equals to GM2 * $(V_{ID} / 2)$ * R_d but since g_m 1 equals to GM equals to GM 2 can just simply replace by this formulation, so therefore I get V_{01} / V_{ID2} equals to half GM times Rd and V_{o2} / V_{ID} is equals to plus 1/2 g_m I_D.

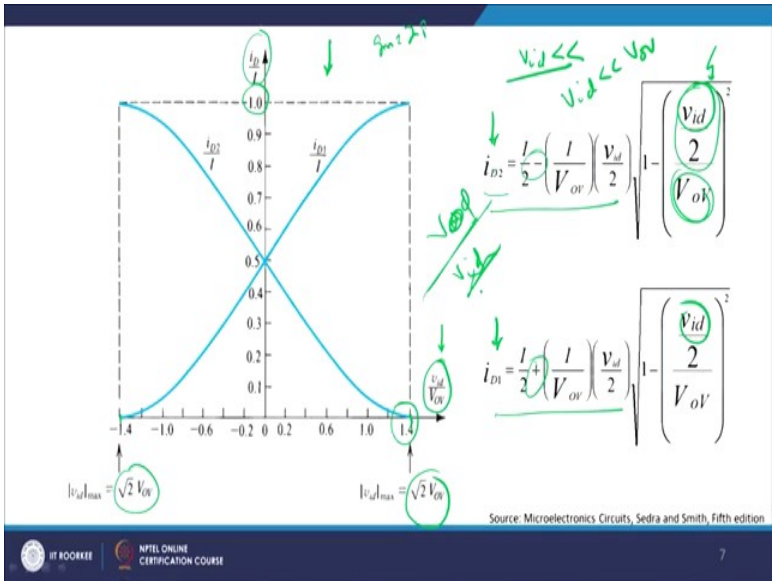
Therefore, if I want to find the differential gain will be $V_{O2} - V_{O1} / V_{ID}$. Now V_{O2} , $V_{out\ 1}$ will be nothing but you will have V_{ID} multiplied by g_m R_d this if you divide by V_{ID}, this cancels off and I get g_m times R_d which we have already derived earlier also that means for a MOS transistor, for a MOS based, for a MOS based differential pair where g_m is the acting load I can safely write down my A_V gain to be equal to g_m times r_d fine and this is what you get g_m times R_d is the best value of a voltage which you get.

Now if you if you therefore have this g_m R_d available with you or has got a g_m R_d which is digitally smaller therefore if you want to improve the gain you need to make your gm's larger right. But if you want to make a g_m larger as I discussed with you the previous term, even this term also you end up having a larger non-linearity also coming into picture right. So you have to be very careful while designing operational amplifiers or for the differential amplifiers to a larger extent.

With this knowledge let me come to the next section of our talk and that is basically finding out the CMRR value and to skate the CMRR value maybe let me switch it over and let me explain to you here that as discussed yesterday as well this left hand side is basically I_D / I, the current normalized with respect to the overall current and this is difference current divided by $V_{overlap}$.

As you can see when my V_{ID} is very-very high almost near to root (2) $V_{overlap}$ the maximum value I get all the current, all the charge carriers are flowing through I_{D1} through Q 1 and Q 2 is giving you 0 current whereas when your input voltage is minus times root (2) $V_{overlap}$ then you all the current is flowing through Q 2 and you are not getting any current to Q 1 right. So this is the extreme value anything larger than that no problem, but then you will explain extend larger non-linearity.

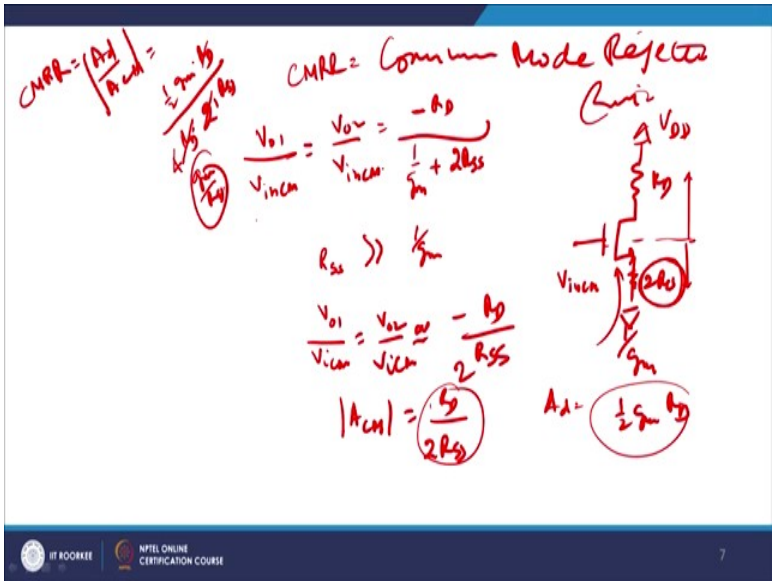
(Refer Slide Time: 28:35)



Similarly if you look at the trans conductance profile which is basically g_m which is $\partial (I_D)/ \partial (V_G)$ then somewhere here if you see around mid-point you will see the maximum value of g_m

is available here which means that if you bias your device somewhere in the middle and try to give your V_{ID} just this difference between these two right, I would expect to see a very large gain anything larger than that no problem, but it will to go into this nonlinear region and in your nonlinear gain with you and therefore, that is not a very good idea to stop with.

(Refer Slide Time: 29:11)



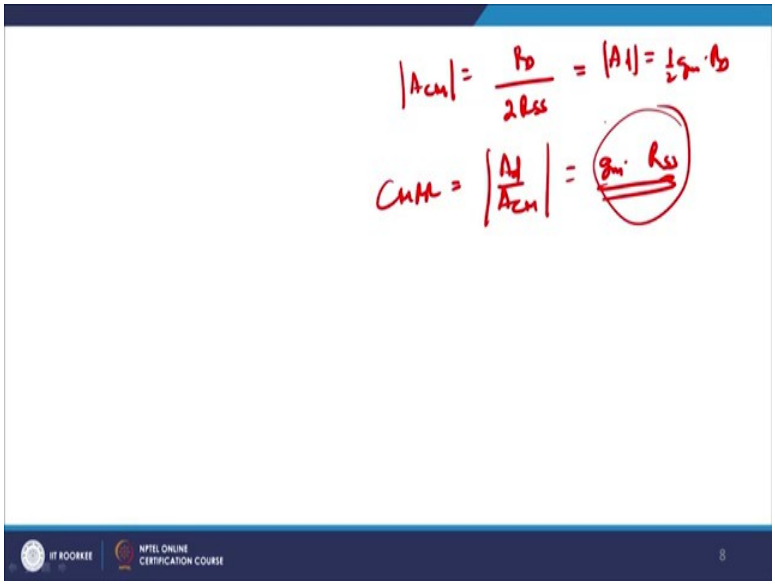
With this knowledge of it this idea let me just also explain to you an important term which is basically your CMRR also known as Common Mode Rejection Ration right. If you find out Common Mode Rejection Ratio, if you look at that graph it is basically R_d and then you have got right so this is your this and this is a V_{incm}, this is your R_d and let us suppose 2 R_{SS} and this is my V_d fine then V_{01} output 1 / V_{incm} is equals to V_{02} by V_{input_cm} right equals to minus R_d / (1/ g_m + 2 R_{SS}).

See this is one of the techniques which people used in later days that but just by inspection only you can tell me the sort of a volume sort of a gain of a circuitry. So how do you do take the active device right go from numerated from this active device to up and from activity device to down then you will see they divide the total impedance seen from active device to V_{DD} you divide that by total impedance seen from the device to the ground, and that will be your overall gain with a negative sign because you will have a 180 degree phase shift so with the minus R_D as you move to the top, if you go below you have $2R_{ss}$ as your load plus 1 by g_m remember 1 / g_m, 1 / g_m is very important term.

Which means that looking from the source end of my active device, MOS device, the resistance offered is 1 / GM right, and since RS, twice R_{SS} is a series to that we automatically get this much amount of this was amount of this your V_{01} / V_{incm}. Now R_{SS} is generally greater than 1 / K small g_m and therefore V_{01} / V_{icm} equals to V_{02} / V_I cm right is approximately equal to R_d / R_{SS} or 2 R_{SS} right so which tells me that mod (A_{cm}) is nothing but R_d / 2 * R_{SS}.

Why, because you still have not inserted any differential signal you are only inserting V_{incm} and therefore the overall gain is R_d / 2* R_{SS} right R_d / 2 R_{SS} with a negative sign and mod of that will a positive value. Now your differential gain A_D will be equals to 1 / 2 g_m * R_d this we have already seen earlier and therefore your CMRR can be written as A_D / A_C, A_{cm} and A_{cm} is how much, A_{cm} is R_d / 2 R_{SS}, A_D is this much so I just need to solve the value is A_D is 1 / 2 g_m * R_d this divided by R_d times 2 R_{SS}. So this took so I have got 4 here, this R_D gets cancelled out and I get g_m by R_{SS} fine, and that is the differential gain which you see here.

(Refer Slide Time: 32:24)



So if you want to find out CMRR at which you let me again give you an idea that A_{CM} will be equal to R_d / 2 R_{SS} which is equal to and your mod (A_D) will be equals to 1/2 g_m*Rd so therefore CMRR is given as A_D / A_{CM} with the mod sign right and this will come out to be approximately equal to g_m * R_{SS}. So you see unlike in the previous case it was g_m * R_d when you want to find out CMRR it is g_m* R_{SS}. So gain is g_m * Rd and CMRR is g_m * R_S.

So, therefore if you want to improve your CMRR the best option available to you increase the value of R_{SS}. So make it to the order of Giga ohms or something very large value as a result it

will never be able to get the output swings but the price then you have to pay is that there will be large power dissipation across these resistors, right and voltage swings and the leg room will also be restricted (33:21) directly because there will be some voltage drop across R_{SS} as such.

If you therefore so if you look very carefully I get g_m * R_{SS} so if you want to improve it a CMRR make it higher make your R_{SS} large and g_m large and this takes care of approximately our understanding of CMRR in the basic principle. In our next discussion, our next slide we will be actually looking into the various other aspects of the MOS device based differential amplifier and its applications right. Thank you very much.