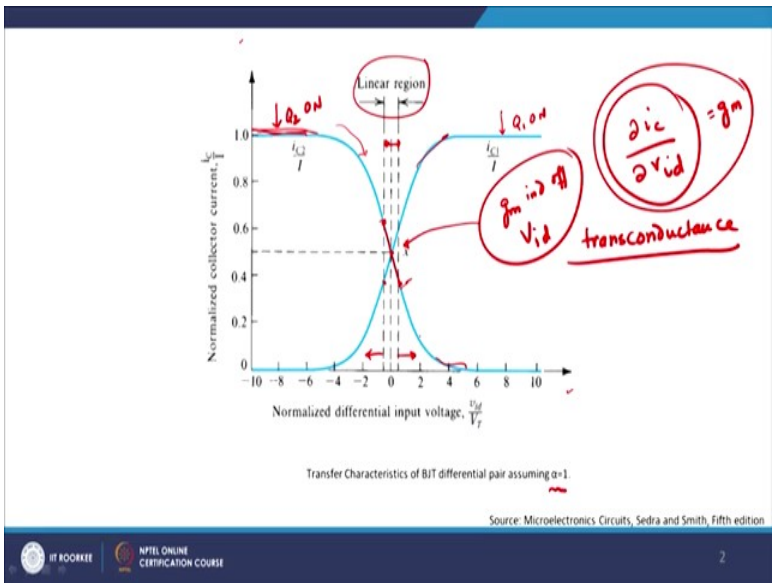
Microelectronics: Devices to Circuits
Professor Sudeb Dasgupta
Department of Electronics and Communication Engineering
Indian Institute of Technology Roorkee
Lecture 34
Multistage and Differential Amplifiers-II

Hello everybody and welcome to the NPTEL online certification course on Microelectronics: Devices to Circuits. In our previous model we had looked into differential amplifiers and we will start of from where we left and let us look at the therefore the transfer characteristics.

(Refer Slide Time: 00:45)



As we discussed in the previous term that, if you go to extreme this is basically the plot between collector current, normalize collector current with respect to difference voltage, normalize with respect to the thermal equivalent voltage which is V_T, 25 millivolts. If you go to extreme right as you can see, you will see that the Q 2 will be basically off and therefore the current will be 0 whereas Q 1 will be on and therefore you will get a large current, so this is Q 1 is on, right.

On the extreme left, Q 2 will be on and therefore you will get Q 2 a high current whereas Q 2 will be off and you will get a Q 1 current. Somewhere in the middle where linear region has been maintained, is the region where the differential of current with respect to input differential voltage, so this is basically if you want to find out the slope of this curve from this point to this point, this point to this point it is basically $\partial (i_c) / \partial (V_{id})$, right.

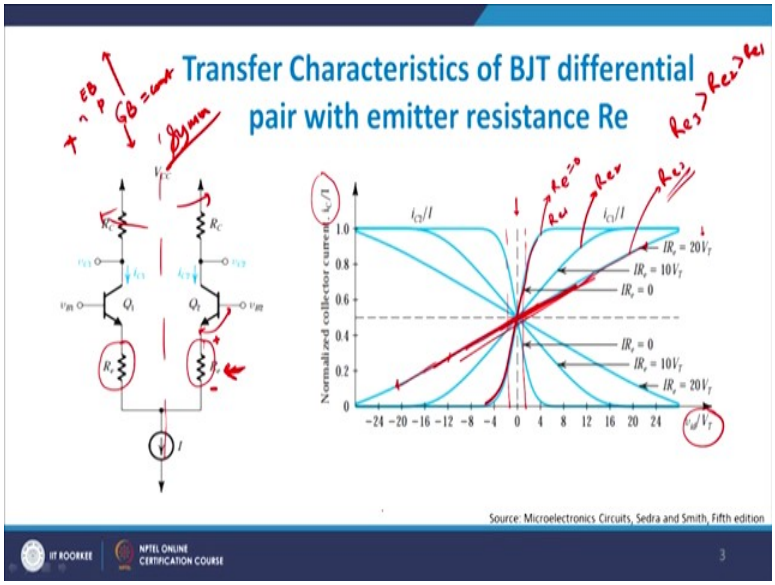
So, if that is the slope you are referring to $\partial (i_c) / \partial (V_{id})$ is maximum somewhere in the middle of this region, right somewhere in the middle of this linear region and if you look very carefully this is nothing but the transconductance of the transistor, so this is transconductance, why it is a transconductance? Because you are giving on to the base the voltage, the difference of the base and i_c is the difference of the collector current.

So, it is basically g_m for the whole differential pair, for the whole differential pair this is g_m which you see transconductance. And as you can see, this is the region where gm is almost linear and therefore g_m is almost independent of V_{id}, right g_m is almost independent of V_{id} at this particular point. Which means that, take any value of g_m any point, at any point you bias your device and give you peak to peak swing between this point and this point and you would expect to see your g_m to be almost constant and therefore gain to be almost constant and the highest gain also you will get here.

As you move towards this region, this effect sample if you look at this point, the gain will be almost equals to 0, right because the current is not changing with respect to variation in the differential voltage. Similarly, the here the gain will be slightly less but as you shift towards the middle where you have a linear region of operation you get the highest gain, right and therefore, I am also assuming that approximately α is approximately equals to 1 which I am which basic assumption I am taking here.

To improve these linear regions the problem is, if you look very carefully the problem is at linear region is only restricted by this much amount of V_{id}, hardly of the other of few millivolts, right few millivolts. So, typically if you want to make it more realistic differential amplifiers you have to increase the linear region of operation which means that you want to increase this 1 unit to increase it, right and make it shift go to both right hand side.

(Refer Slide Time: 03:41)



How do you do it? Well the methodology which people adopted was that they inserted a resistance R_e in series to the (emitted region) emitter region and if you plot there for the graph between i_c by I which is basically collector current normalize with respect to total current versus V_{id} by V_T, the same graph as the above, you see as the R_i value becomes larger, right.

So, this is for various values of R_i, this is the value with R_i is equals to R_e equals to 0, right this is with certain value of R_e such that I_e into R_e 10 times V_T and this is with the value i into R_e equals to 20 times V_T. So, obviously this is suppose R_1, R_{e1}, R_{e2} and R_{e3} then R_{e3} is greater than R_{e2} is greater than R_{e1}, in fact, R_{e1} is approximately equals to 0 we have sorted it, the previous one which means that, if you look very carefully you are actually increase the linearity, look at the point that when you increase, when your R_{e3} is largest, your linear region is extending from maybe from this point to this point to larger extend, right.

So, your linear region is extending, so you can play with this for a large linear region whereas when you make a R_e equals to 0 your linear region is very, very small maybe this just small around as I discussed with previous slide. And therefore putting R_e we will discuss why is it like that but increasing R_e mixed the it is more linear but cost to pay for it is that the transconductance in the gain therefore reduces when your R_e is large, we will also explain this point one by one.

But as you can see the slope here around this particular point around mid when V_{id} equals to 0 is small slope as compare to a slope of this line. So, you see that it putting R_e makes my linear region of operation broaden but the cost I pay for it is that I reduce my overall gain, so g m

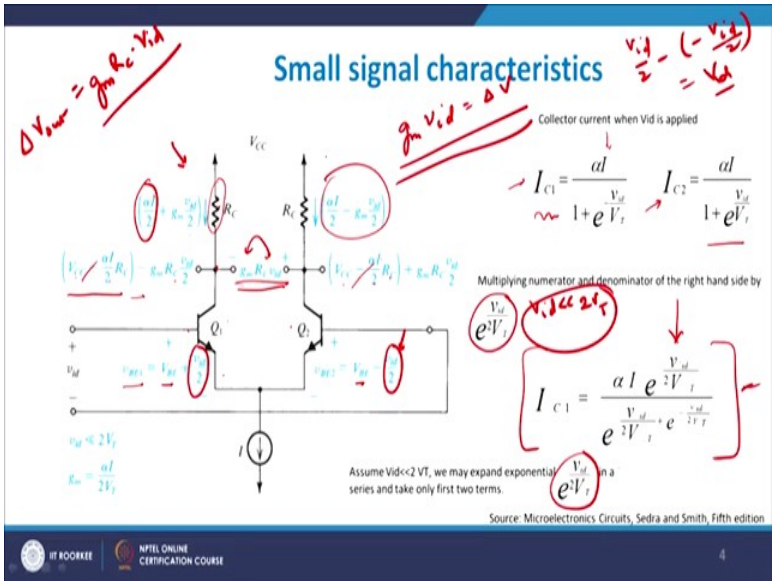
reduces transconductance reduces, why does it happen? We will just discuss that point. Say, you have inserted Re here, right you have inserted Re, first let us see why transconductance and therefore your gm or gm reduces in this case.

See, once you reduce when as you put R_e, your R_e actually has a bias which is something like this, right and therefore in a sense it is reverse biasing your npn (transfer) emitter base junction. So, I have an emitted base junction, if you given it is npn, so if you give a positive potential on the n side your reverse biasing emitter base junction and it is reverse biasing it, what is happen? The gains fall down because you are not letting down large amount of emitted current to come across and therefore your collector current will be also small.

That is the reason your gain starts to fall down when you insert R_e, right and that is the reason your gain and therefore you see gm values are reducing, gain starts to fall down, why does it increase the linear region? Because if you remember gain bandwidth product is always constant, so therefore when the gains fall down you can work with the larger bandwidth, your bandwidth increase and therefore your linear region of operation becomes larger and larger in this case, right.

So, that is the reason why we use, so we can use these two generally make it this thing. Please understand all these discussions are with the classist assumption that my both the arms here, left arm and right arm are exactly symmetrical in nature. If they are not, then this is not a whole good, there will be some changes which you need to do.

(Refer Slide Time: 07:14)



Ok, let me come to the small signal characteristics of the of a BJT bipolar transistor as differential amplifier. So, I have Q 1, Q 2 here, I also have V_{id}, V_{id} is basically the difference in the potential of base to emitter of Q 1 and Q 2, so if see V_{B1} is nothing but V_B, V_B is the basically the DC bias which we applying + V_{id} / 2, so the difference is V_{id} then if I write this to be as plus V_{id} by 2 then they should be - V_{id} / 2 why? Because V_{id} / 2 minus of minus V_{id} / 2 will give you plus V_{id}, right and that is a difference which you see here, that is the reason we write plus V_{id} / 2 or - V_{id} / 2.

Similarly, we can write I_{C1} to be equals to α times I_{e1}, now I_{e1} is nothing but I upon 1 plus e ^ - V_{id} / V_T and I_{C2} will similarly will be α I upon 1 + e^(V_{id} / V_T), right. Now, if you multiply the numerator and denominator for this transistor and this one by e to the power V_{id} by e ^ $2V_T$, we get I_{c1} to be equals to this much, right and I_{c1} we get is and therefore I mean if assume that V_{id}, right is much smaller as compare to $2V_T$ which is typically is.

Let us assume, we may expand the series in exponential this one, this one is in the numerator and in the series and take only two first two terms. So, what the first two terms will be? I will just discuss that in the next slide but assume this to be as the I_c which is available to us again α I_e to the power so multiply V_{id} by 2 times V_T and then I multiply this to the power e^(V_{id} / $2V_T$) plus if I by $2V_T$, I will get minus V_d / $2V_T$, right and that will therefore that is what I am doing here.

If you look, therefore on this side from the on the base side, I get V_{cc} - α I / 2 * jab Rc, remember why? Why is it minus α Ic / 2? The reason been the total current flowing through

Rc on the left hand side will be nothing but α I / 2 which is the dc bias which you see, we have already discussed this point earlier plus g m multiplied by Vid / 2 because Vid/2 is the approximate voltage which is visible between base emitter that you multiply with gm you get the currents, so this is what you get I_c.

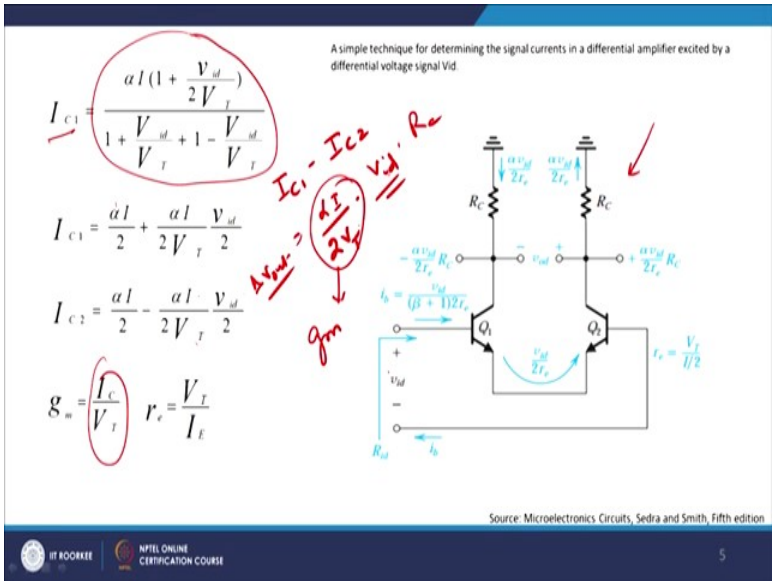
But on the right hand side, you will get a minus V id because you see this is minus V_{id} / 2, so I get minus g_m * V_{id} / 2, right we get minus g_m * V_{id} / 2. Now, quite interestingly if you simply add subtract these two α I by 2 at α a by 2 cancels off and you what you get is? Basically g_m times V_{id}. So, even without knowing anything if you just simply find the difference between this and this, the current difference this is ∂ voltage difference, sorry ∂ voltage difference which you see, right and you get ∂V * I_c which you see.

Now, you see, so what I get if we closely therefore come into the point then I can simply this, so if you look from the right hand side I can simply multiplied V_{cc}, right minus (alp) so if the potential drop across R_c I need to find out will be nothing but V_{cc} minus α I by 2 into R_c, right that is the potential which is appearing across R_c - g_m * Rc into V id by 2, right because you have to subtract these voltage to achieve the voltage at this particular point.

Similarly, if get this I have to multiply this with R_c and therefore I get V_{cc} - α I by 2 into R_c α I / 2 * R_c plus, why plus? Because there will be a negative sign here, so minus into minus is plus gm * R_c / V_{id} / 2. But if you subtract this from this, this whole thing get cancelled with this whole thing, this remains so this minus of minus this will give me g_m * R_c * V_{id}, fine.

So, the output voltage difference between the two is nothing but gm R_c * V_{id}. So, this is ∂ V_{out} is equals to gm R_c * V_{id}. So, if your V_{id} is large you get a very large value of ∂ta V_{out}, if your g_m is large you also get a very large value of V_{out} and this is true also, we have understood from our basic understanding previously.

(Refer Slide Time: 11:42)

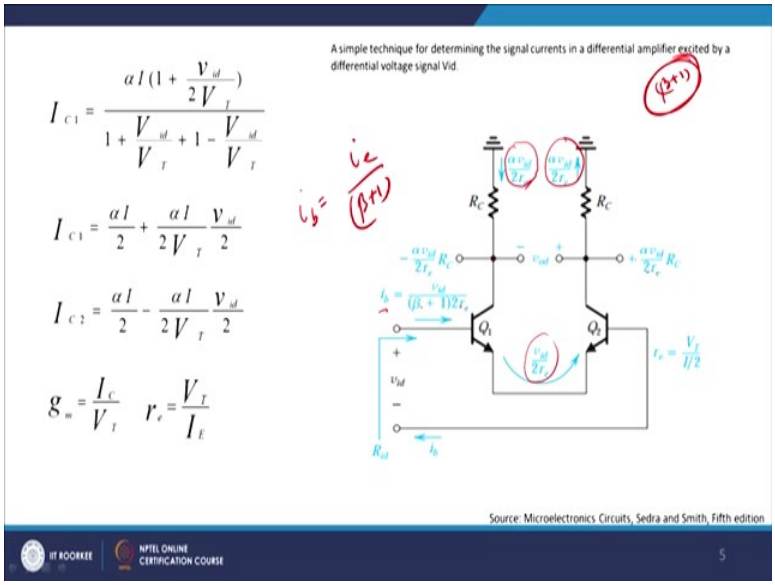


Now, let me find out the, this what I was discussing with you an earlier sense, that IC1 therefore can be written as this by expanding it by expanding the previous discussion and similarly I_c and therefore if I break it down I get α I by 2 plus α I V is by 2 times $2V_T$ and I_{c2} is equals to α I by 2 minus α I $2V_T$ / V_{id} / 2. So, if you add these tw o, two, so if get the I_{c1} - I_{c2} as I discussed with you, you will get the this will gets cancelled out and there will get you, this will get added up and you get α I by $2V_T$ into V_{id}, we will get, fine.

That is basically difference in current, this multiplied by R_c will give you with the difference in voltage. Now, you see very well that this is nothing but the Charles conductors of the device gm and therefore we can safely, so that is what I am saying I_c / V_T is transconductance of the device and therefore I can safely write down this to be as g_m * V_{id} * R_c which we have already derived in a our previous our case, right, ok.

So, this gives me an idea about the basic understanding and therefore as we have already discussed the transconductance of a device higher the transconductance of the device more will be the output voltage, higher the value of R_c more will be the value of it. So, this is basically your ∂ (V_{out}) which you see, right, If you look at this graph here and what I am trying to tell you here is, if you look at the figure here, you see the Q 1 and Q 2 are both in active region of operation.

(Refer Slide Time: 13:12)



And if we now try to find out a how much amount of input resistance is there? See, when you are looking at MOS as devices, MOS based devices, right in MOS base devices you were actually looking into the gate side, with then signal was inserted to the gate side of a MOS device which is obviously giving you infinitely large input impedance because gate was having a dielectric constant of oxide and therefore this was problem whereas in this case which is in this case you are actually looking into the base side.

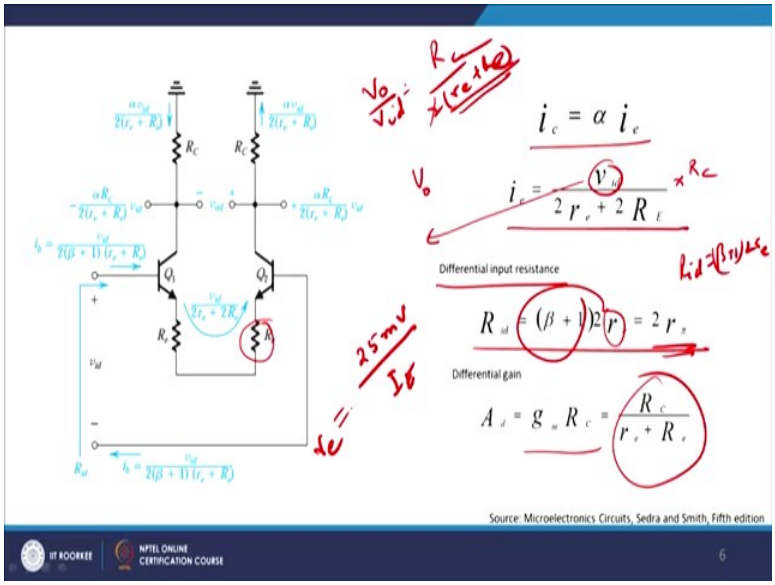
So, base side will have a finite resistance and that is what you are trying to find out, how do you find out? You find out the base current, right. So, base current if you want to find out if it was basically a basic idea that if the resistance looking from the source side, is let a suppose twice R e, right then on the base side it will be B plus 1 times R_e, so that is what I am trying to, so we it will you have to multiply by β plus 1 when you looking from the base side.

So, the base current will be Vid by $2R_e$ * β + 1. Similarly, on this side, so where Vid by 2Re is the difference voltage which you see in front of you therefore if the same current flows through, so α times Vid, so current is basically V_{id} / 2 R_e that is emitter current if you multiply by α that is a collector current, so this is the collector current here and this the collector current here.

If you multiply this with Rc I get the voltage at this particular point with a negative sign and since there 180 degree phase shifted I will get a positive voltage here which is a α V_{id} by 2 R_e * R_c, right and the base current will be V_{id} / 2 R_e; V_{id} / 2 R_e is nothing but emitter current

divided by β plus 1. So, i_b equals to emitter ie upon β + 1, remember and from there I get this as the emitter current which you see, right.

(Refer Slide Time: 15:05)

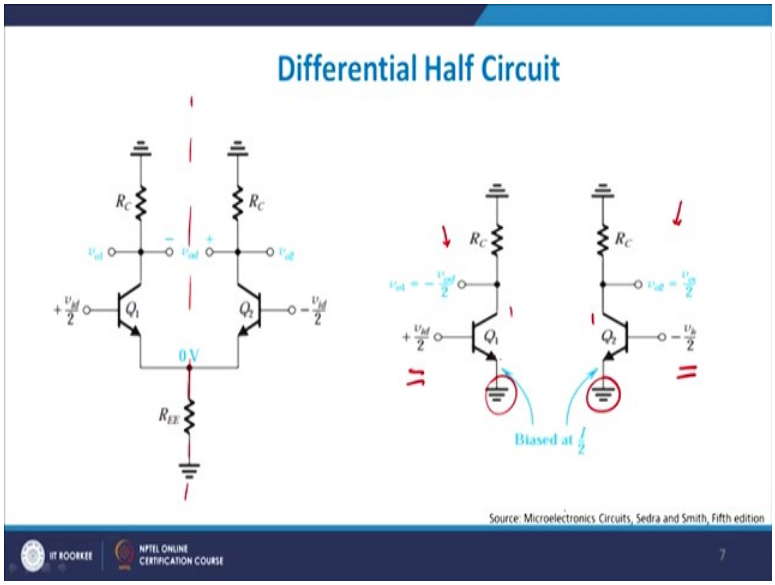


Now, with this region I said i_c equals to α i and i therefore is equals to V_{id} / 2 r_e + 2 r_e we get. So, the input differential resistance R_{id} is equals to β plus 1 * 2 r_e, right and this β plus 1 into 2 r_e is also referred this is r_{pi} and therefore we referred to this as R_{id} is equals to β + 1 * 2 re, re is the resistance looking from the emitter side, right.

And the differential gain is g_m times R_c, g_m we have already find out to be some value which is R_c by r_e + R_e, right R_c, how did you find out differential gain if you want to this will be this you need to multiply with R_c, right you multiply with Rc you get the Vout. Now, this Vid if it goes down I get V_o / V_{id}, right I will get R_c / 2 r_e + R_c, so this 2 will be very small as compare to the anything else I get R_c / r_e + R_e, sorry re, right R_e is the resistance offered from the emitter side and r_e is the dc resistance which you have actual resistance which you have put.

So, if you see a differential gain depends upon the ration of your collector resistance to that of the emitter resistance plus the r_e value, r_e value is the small signal r_e which you see to it is basically 25 mv millivolt by I_E, this is equals to r_e, right and this is what we get as a differential gain.

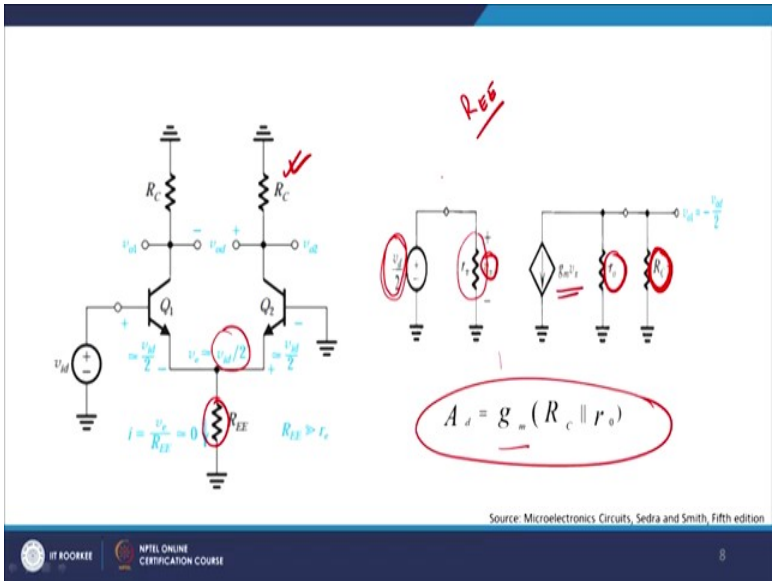
(Refer Slide Time: 16:36)



Now, the concept here is that if everything is symmetrical both the left arm and right arm are symmetrical, we can divide the whole differential circuit in a two half circuits. So, what we do typically is that we break it down this middle and then we say that on the left hand side V_{id} / 2 is the input voltage, on the right hand side - V_{id} / 2 voltage and they are biased such that I / 2 current flows through this arm and this arm and therefore V_{od} / 2 at this point and V_{od} / 2 at, so minus plus is there, right and therefore the output difference, did you find the difference between the two? It will be still V equals to V_{od}.

So, this is the concept of differential half circuits that overall transconductance will be divided by 2, you will also have the bias current divided by 2 and you what you do? Is that you emitted part of the BJT is actually grounded here, right they grounded here and once they grounded they act as a differential half circuit, right.

(Refer Slide Time: 17:34)

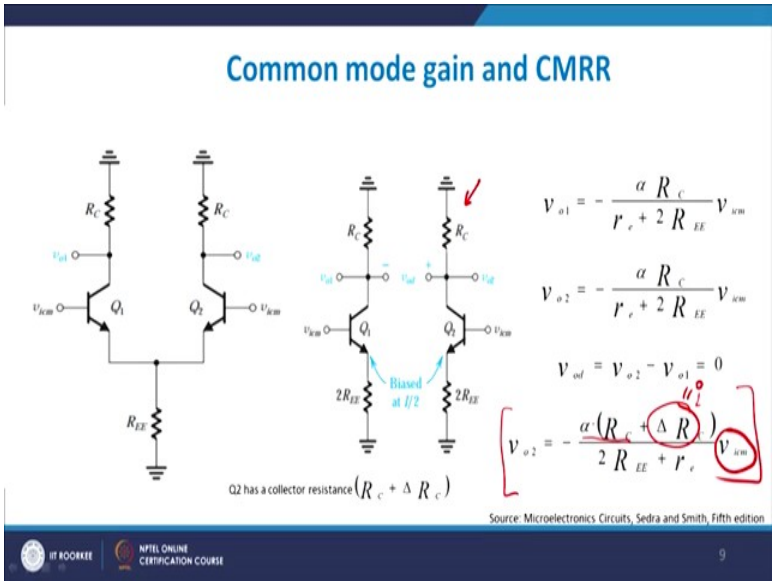


The advantages it is much easier to calculate various formulas from differential half circuits. With this knowledge, let me therefore come to a small signal characteristic of the differential amplifiers. As you can see my input voltage, I have already told you is differential V_d / 2, right so I have giving V_d / 2, this r_{pi} is nothing but the input side resistance offered by the differential pair. So, it is basically the pairs r_{pi}, right.

If you look at the right hand side since it is V_{cc} voltage control current source, any V_{pi} which you give in the input side you will have g_m * V_{pi} as the current flowing in the output side, right. So, this is your this, this is your collector resistance which you have already found out and R_0 is the resistance offered by the device itself, right, so, these two are in parallel. So, if you even close your eyes do any problem, I simply can get the differential gain to be equals to g_m * R_c || R_o, right.

So, transconductance multiplied by output impedance will be actually equals to the voltage gain and that is what we have shown here, right. This is with the assumption that my R_{EE} which is the, so what I have done here? Is that I replace the current source by your resistance and this resistance value is very, very large, it is typically very large, right and it does not let any current to flow through a typically and therefore I can safely write down V to be equals to V_{id} / 2 which you see here, V_{id} / 2. So, the emitter resistance, so emitter voltage is exactly equals to V_{id} been V_{id} / 2 in both the cases.

(Refer Slide Time: 19:04)

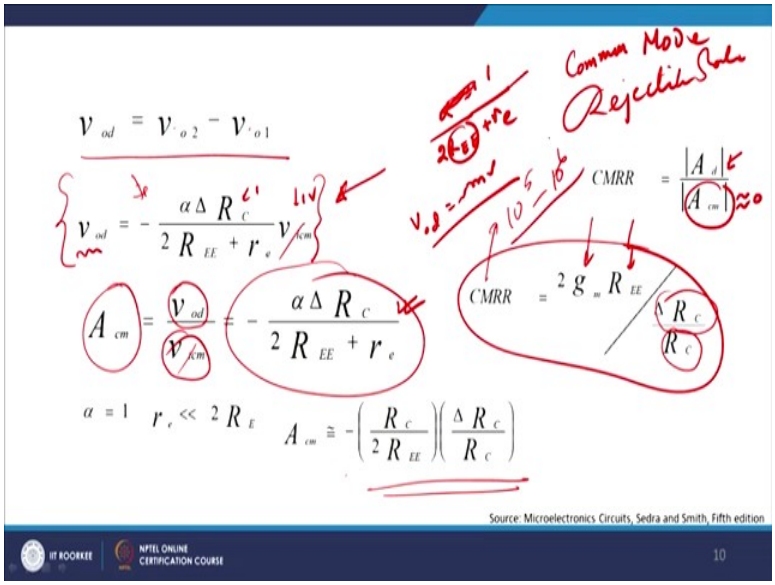


Let us look at the common mode gain and CMRR. To what we will be doing and what we will be understanding is basically that, let us suppose that in reality, of course, your left hand, right hand side will never be symmetrical with respect to each other, that we already know because there will be some mismatch in the resistances, some mismatch in the emitter resistances, some mismatch in the character resistances, the transistor itself will be mismatch in terms of thermal equivalent voltage is through and so on and so forth.

Now, under a criteria that you do have a change, let us suppose that my one of the arms R_c changes by ∂R_c then I can safely write down V_{o2}, you can do it yourself is given by minus α times R_c plus ∂R_c / 2 R_{EE} + r_e * V_{icm}, V_{icm} is nothing but the input common mode voltage, right, I am not giving any differential voltage now. So, under the presence of a input common mode voltage my output voltage V_{oc} comes out to be this.

So let us suppose there would not have been any ∂ R, so this would have been 0, this would have been 0, right this would have been 0, and I would have got a α R_c / 2 R_{EE} + r_e. Now, because of this ∂R_c I have an extra voltage term which comes into picture.

(Refer Slide Time: 20:12)



Now, therefore V_{od}, which is a output difference voltage is V_{o2} - V_{o1} will be given by this quantity. So, which means that even in presence of a equal voltage at the base of the two transistors because of a ∂ R change in one of the resistances I always will get a V_{od} equals to this value which is given by this value. So, ∂ R_c say 1 ohm then I will always get off, so V in equals to 1 ohm, this is 1 volt and this is also equals to 1 ohm, then there will be an α upon 2 R_{EE} + r_e, right α is very close to 1, so I will get almost equals to 1 upon this whole quantity, R_{EE} is very large quantity.

So, typically what I will get is, V_{od} few millivolt there will be an always offset available to me, the order of few millivolts. We define therefore A_{cm} which is basically my common mode we defined this to be as common mode gain, common mode gain is basically my output voltage under the condition that I am given a common mode voltage in the input side, I get this to be true, you see this V_{od}.

So, if you divide by V_{icm}, this V_{icm} cancels with this V_{icm} and you are left with A_{cm} to be equals to this much. Now, you can write down A_{cm} to be also breaking up into this value, you just simply can do a small manipulation and CMRR which is basically known as common mode rejection ratio is defined as the difference of the or ratio of the differential gain to common mode gain. Which means that, if I give a common mode signal to both the arms of my bipolar differential amplifier I record a gain, right and that gain will be by virtue of ∂ R whatever change is there and I also record the gain by giving a differential signal to both the arms, I divide 1 upon another and should get the CMRR. Ideally CMRR should be infinitely high,

the reason you can understand, why? Because your A_{cm} should be (approxi) will should be ideally equals to 0, ideally your A_{cm} should be 0.

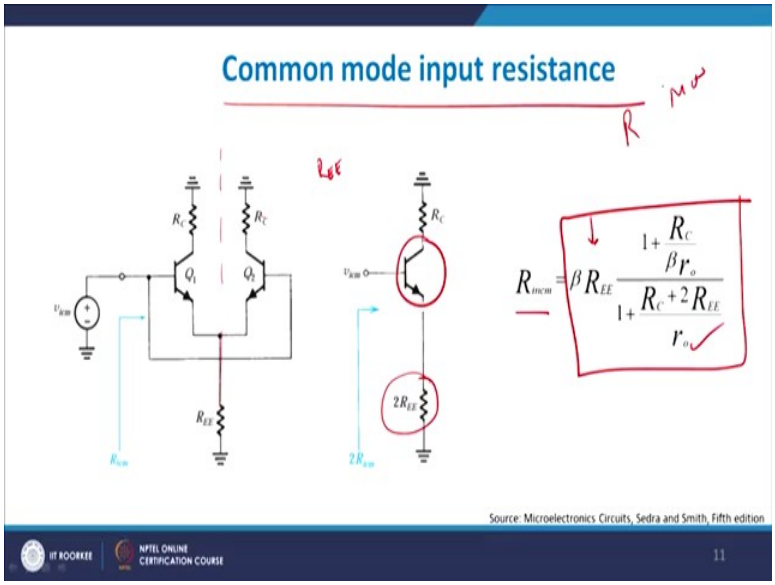
We, have seen in the first few slides of my previous picture that A_{cm} should be approximately equals to 0, the reason been for a exactly the same bias apply to do transistors, the output was actually equals to 0, so my A_{cm} should ideally equals to 0, it is not by virtue the fact that both the arms are not symmetrical in natures, there is some difference, so there is some finite value of A_{cm}.

Similarly, Ad will be some particular value. So, if you divide A_d / A_c, I get this as my CMRR, so it is 2 g_m * R_{EE} upon ∂R_c / R_c, right and this gives you a value of your CMRR, Re obviously is very large value, g_m is also very large, ∂R_c is very small, R_c is also relatively large of the order of kilo ohms. So, you get CMRR very large of the order of 10 to the power 5 to 10 to the power 6, ideally you should get infinity but this is a order which you get for CMRR.

Higher the value of therefore the CMRR, a common mode rejection ratio better the differential amplifier in rejecting common mode signals and accepting differential mode signals or amplifying differential mode signals, right. Typically you will see as you may be we can stick up in the next slide or maybe in the next lecture, that noise is generally common to both the arms, noise is not differential.

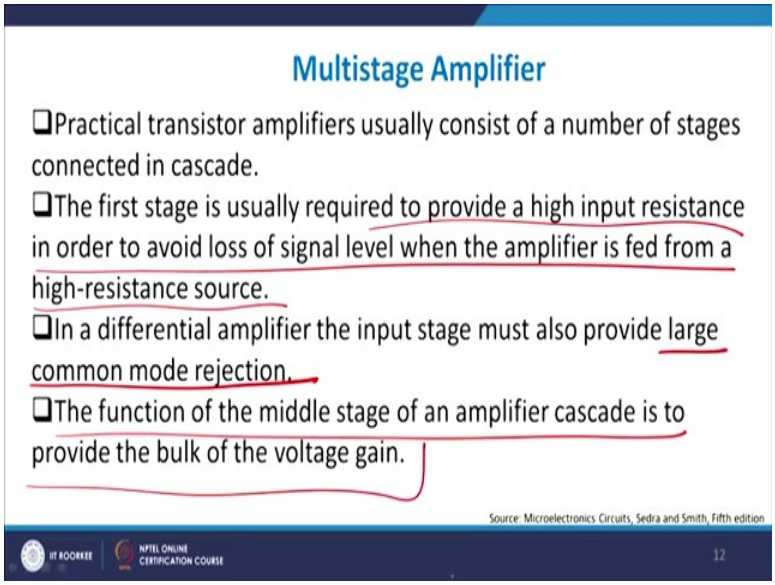
So, therefore a differential amplifier will be a very good rejecter of noise and very good amplifier of signal and therefore higher the CMRR value of differential amplifier better the design is as far as it is input resistance is concerned, ok.

(Refer Slide Time: 23:56)



Let me therefore explain to you, what is known as common mode input resistance? We have seen it already and it is resistance looking from the input side to the base side of (my) of a design, right. So, remember half mode signal I / 2, so if I take (so I will get R $_E$) so I get R_{EE}, so I get $2R_{EE}$ available to me because this time just overlapping with respect to each other Rc, R_c and therefore I get V_{icm}, so R_c in comes out to be just definition I am not deriving it in the class but it is β times R_{EE} upon 1 + R_c / (β) r_o and this is the value of your R_{incm}. So, this is the input resistance, it is actually infinite in case of MOS differential pairs but infinite value when you have this into consideration, right. Let me come to the multi stage amplifiers, well in practical stages you will have maybe each differential amplifier driving another differential amplifier so on and so forth.

(Refer Slide Time: 24:56)

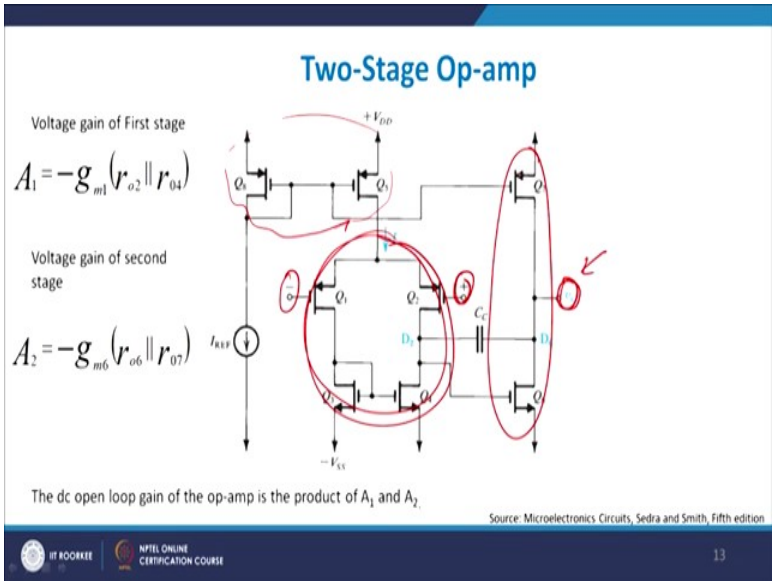


The first it is usually, so if you have a multistage amplifier typically, the first stage is require to provide a high input resistance and order to avoid loss of signal level. So, if I, so if you have put two stage amplifier, the first stage is generally used to match the impedance, so the first stage is got a high input impedance because typically my source has got a high output impedance to match the two, I generally the first stage is basically having high input impedance.

In the, in differential amplifier the input stage must have very large CMRR, right and therefore that is what I written here, right. So, the function of the middle stage of an amplifier cascade is to provide the bulk of the voltage gain. So, if I gave got two stages, three stages let us suppose, the first stage is just to match the impedance level, so that the maximum power is transferred.

The differential part will be responsible for high gain by virtue of by noise reduction, by virtue of high value of CMRR and maybe the third stage or middle stage will be responsible for high value of voltage gain, right. So, we will come to that in a much more detail manner.

(Refer Slide Time: 26:04)

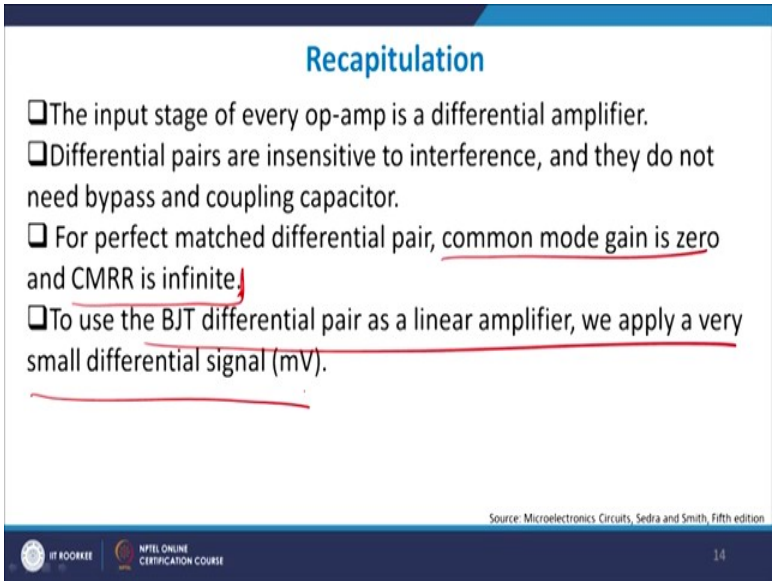


At this stage, this is just a diagram of a two stage op-amp. We have just give you an idea about in reality because when we because after this lecture we will do the MOS differential pair then it will become clear, maybe we will revisit once more when we come to op-amp later on but if you look carefully this is nothing but an replication of a BJT differential pair. If you look carefully, this is the differential pair which you get here, right and this is the differential pair which you get here where I am giving this is the input differential R which I am giving here and this is the single ended output which I am taking from the sub, right.

So, this pair is responsible for doing all impedance matching, this one is responsible for giving you a large gain and this one is responsible for again impedance matching and giving a proper output, right. So, there are three stages, one, two, three stages available here. Let us now look into this basic fact here, these are simple facts which you should be aware of. At this stage, we will discuss op-amp maybe in details, we will come to revisit this formula once again.

So, just to recapitulate or what we have done till now. So, the first stage of any amplifier design is basically a differential amplifier, right gives you a very high gain. As I discussed with you differential amplifiers are insensitive to noise, they are very good rejecters of noise but they are very good enhancers of input signal.

(Refer Slide Time: 27:35)



For perfect CMRR common mode gain is zero and CMRR is infinite as I discussed with you. So, if you want to use BJT as a linear amplifier, we apply a very small differential signal, if you apply a large differential signal you might end up having a highly nonlinear profile available with you, right because then you move over from the linear region. So, you generally apply a small input signal, right.

So, this may we have actually taking care of the very basic understanding of a differential signal. We, in the next lecture series, we will take a MOS differential amplifiers, right and then explain to you how is a difference from BJT difference amplifier then we will see that MOS is relatively slower in switching as compare to BJT because in BJT if you remember one basic idea was we are moving from active to cut-off and vice versa, we are not atoll moving the saturation.

So, once you do not like let the device move into saturation, the time take into come out from active to cut-off is much faster as compare from saturation to the to active, right because you are in saturation you are storing large amount of charge in the base side which you are have to first remove, right and therefore it is much faster. So, BJT based amplifiers are much, much faster as compare to MOS based, right.

So, but we will look into others factor as well for example power dissipation is higher much higher in case of the MOS devices as compare to in case of BJT as compare to MOS device, fine. With this I think, we have finished with single stage amplifier, basic understanding

using BJT. In the next we will look into the single stage amplifier, differential amplifier using MOS devices, thank you.