Microelectronics: Devices to Circuits
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Lecture 33
Multistage and Differential Amplifiers-I

Hello everybody and welcome once again to the next module of NPTEL online certification course from Microelectronics: Devices to Circuits. Today's lecture will be on multi stage and differential amplifiers. We have studied in our previous few modules, about a single stage amplifier which primarily means that, if I have a simple common source amplifier bit a MOS or a BJT and I give a input signal which is basically a small signal ensuring that my devices are in the linear region of operation.

Then my output voltage will be undistorted without any nonlinear distortion available to it and therefore the gain will be almost independent of the input voltage. But a single stage amplifier, as you can always understand will give you a gain just quite small right, it is the order of few tens a few hundred or maybe something like that, when you want a very large gain out of some particular for a particular operation you either require a differential amplifier or even a multi stage amplifier.

So, what we try to do is? That in the first half of the lecture, we will be looking into the concept of differential amplifier and we will also look into the fact that using a single stage amplifier and by cascading it properly or adding stages to it properly how can I make my gain high. One more important property of differential amplifier which is not there in a single stage amplifier is.

It is capability of rejection of noise which means that unlike single stage amplifier which amplifies both signal as well as noise differential amplifier has got a capability of blocking the noise and enhancing the signal, right. So, signal to noise ratio, sort of if you want to take that as a parameter will be quite high in front of a differential amplifier, so with this basic knowledge or with this basic background.

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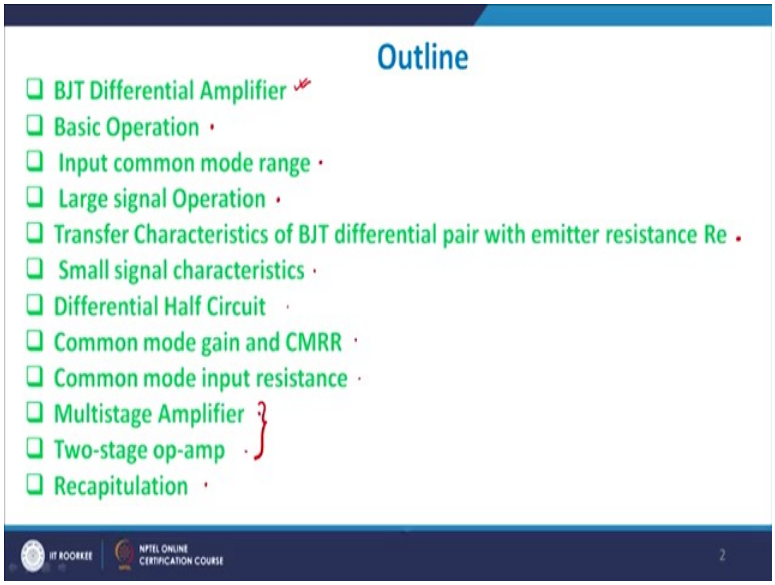

So, the outline of the present course module is, we will first of all look into a BJT differential amplifier in under which, we will look into its basic operation of the device, we will also understand what is the input common mode range with us then last signal operation of the device and then we will see that if we have an emitter resistance how does the output transfer characteristics change.

And then, we will look into small signal characteristics, we will also look into differential half circuits, CMRR we will which is basically common mode rejection ratio and then we will look at common mode input resistance and then we will finally have a look into multistage amplifiers and two stage op-amp as an example and then we will recapitulate, right.

So, these two the last two we will be dealing in a much more detailed manner in subsequent slides or subsequent lectures but today's topic will be more concentrated on differential amplifiers, right. So, let us first look at a differential amplifier and to go ahead let me give you an brief insight if you remember from your very basic device physics courses.

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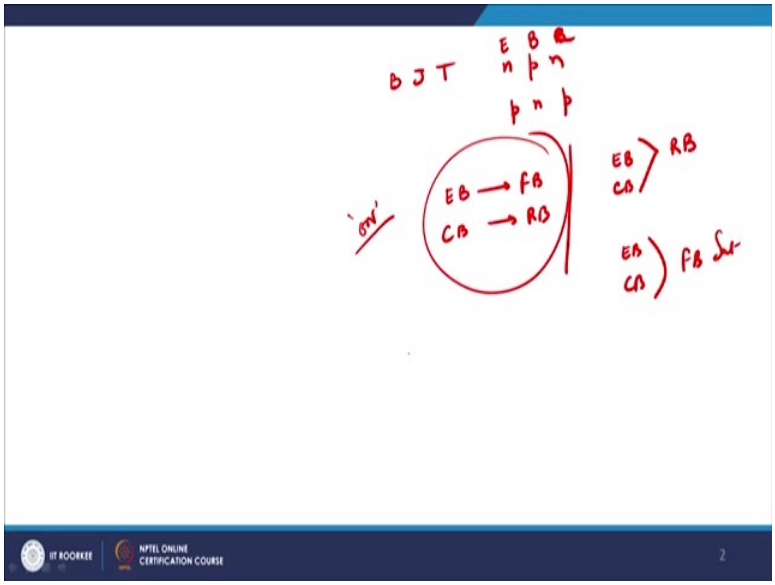

That if you have a BJT which is basically an npn or you will have pnp, right this is emitter base and Junction for the base and collector and therefore, if you want the device to be operating in the saturation region or in the triode region you require the emitter base Junction to be forward biased, right and collector base Junction should be reversed biased. If you wanted to be in cut-off then emitter base as well as collector base both should be reversed biased, right I hope you understood these points.

If you want to work it in the in the active region of operation then maybe emitter base and both collector base should be forward bias, this is your saturation region of operation, right. So, typically we want to keep this is where we define the been on state and we get better idea, right. So, please understand when you want to move the device BJT from a saturated stage to non-saturated stage, you spend large amount of time in switching because the charges in the base has to be removed or flushed out before the next cycle starts.

So, the time taken is very important, we will see in a differential amplifier that we do not like the devices to go into saturation region and that is the beauty of the whole thing that it gives you a much better gain and not only again it gives you a much faster switching speeds. We will discuss one by one as you move along but we will just look at the first of all at a basic differential BJT differential amplifier.

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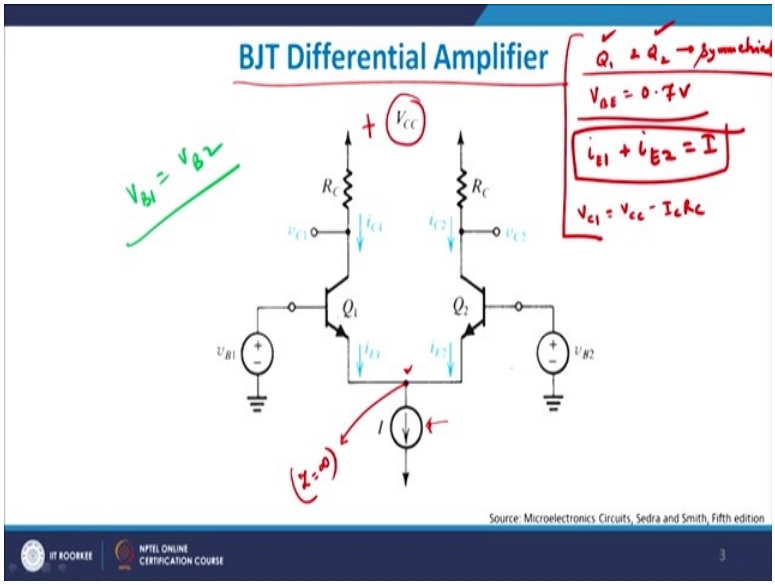

Which is something in front of you, which you can see here, right. This is a basic BJT differential amplifier in which we have got two transistors Q 1 and Q 2, we are assuming that Q 1 and Q 2 are perfectly symmetrical, symmetrical in the sense that they have exactly the same profile, they will give you the same amount of collector current for the same amount of base emitter bias and so on and so forth, that is the meaning of Q1 and Q2 being symmetrical, right and their V_{BE} is since the silicon we assume it to be 0.7 volts because it is the silicon junction which we are assuming.

We also obviously a load resistance R_C of the order of few ohms or kilo ohms, we have a plus V_{CC} here which is basically the power supply and these two Q 1 and Q 2 are fed by a current source which is I which as you can see here and this current source I is basically a current source which is basically and is considered to be an ideal current source and therefore, if you look at the impedance at this point Z will be obviously infinity in infinity, right for ideal current source.

Which means that, at this point it is the impedance looking at this point is particularly infinitely large and whatever current flows through Q 1 and Q 2, if you add the currents you will always get the total current to be equals to I. So, what I get is? The i_{E1} plus i_{E2} will always be equals to I, capital I. so, this constraint always holds good, that the total current flowing through the left arm, which is this one and the right arm, which is this one will always be charge.

If you want to find out the value of V_{C2} and V_{C2}, then it is very simple V_{C1} will be equal to $V_{CC} - I_C * R_C$, right because this is the voltage drop which you see, right this is the $-I_C*R_C$ plus there will be also $V_{ce\ sat}$ which will be coming because of this one for the device to be saturation if provided I allow Q1 and Q2 to go into saturation, will see that we will not allow it to do that but these are the few constraints which one has to work upon, right.

That the total current will be always fixed to I and we are having V_B equals to 0.7 which is the cutting voltage for an npn. We also assume that Q 1 and Q 2 are perfectly symmetrical in nature, with this knowledge we also say that now we apply a voltage V_{B1} on the base side of Q 1 and V_{B2} on the base side of Q 2, right.

If we assume that these two are correct then what we can safely say is something like this that that we can say that which that the collector current I_{C1} and I_{C2} which is the current flowing through the two collector arms of these networks are also equal provided V_{B1} is equals to V_{B2}, right. So, if I assume that V_{B1} equals to V_{B2}, V_{B1} equals to V_{B2} we will see that mathematically later on then if the same bias is there everything else is same I_{C1} will because I_{C2}, right.

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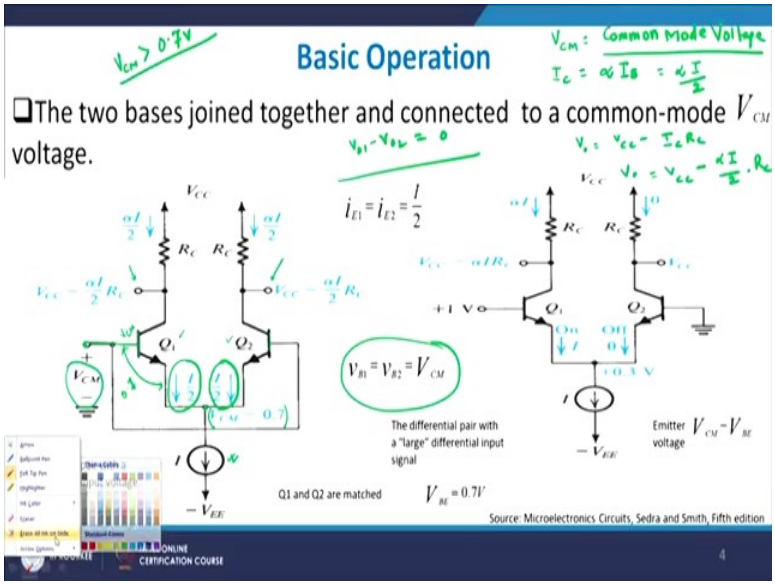

So, this is the basic differential amplifier this thing diagram. Let me see, what happens if we apply the same potential to the base of Q 1 and Q 2, so what I have done? I have simply applied a positive bias here and the same potential is applied to the base terminal of Q 2 and this is basically known as a common mode V_{CM}, V_{CM} is referred to as a common mode voltage, right.

Let me or explain all these things later on but at this stage just assume it to be common mode voltage as the name suggests, this is the voltage which is common to both the arms, right. So, you will ask me why do you require it? Well see, you initially as I discussed with you earlier also that you want this Q 1 and Q 2 to be in the region where you can actually achieve an amplification right.

So, you require a DC bias from an external world, right a DC bias which will fix this device into certain regions of operation where it can do an amplification then superimposed on that you will have an AC signal being available to you. So, these basically or a DC signal which are giving, assuming at this stage what I am saying is correct and under such a criteria let us see what happens.

If I assume, that I am giving V_{B1} equals to V_{B2} equals to V_{CM}, the common mode signal, right so I gave V_{CM} here. Obviously, this will give you a potential drop of 0.7, fine and therefore the potential at this particular point will be V_{CM} minus 0.7. so, you have applied a potential DC bias here which is V_{CM} a 0.7 voltage drops takes place here, so at this point the value of the voltage will be V_{CM} minus 0.7, right.

So, which means that both the devices Q 1 and Q 2 will be in all state provided V_{CM} is greater than 0.7, fine. So, if my V_{CM} is greater than 0.7 volts I would expect to see that both the devices will be non-state, right. So, they will be on, when they are (equ) they are on they will be carrying since both of them are on equally they will be carrying equal currents. So, therefore if total current is basically equals to I, Q 1 will carry I by 2, right and Q 2 will also carry I by 2.

So, half the current will be flowing through the left arm and half the current will be flowing through right arm and therefore if you want to find out the current through this collector remember, if you are from a basic semiconductor the code says is that IC will be equals to alpha times i_E, so if your i_E is equal to I by 2, I get I_C equals to alpha times I by 2. So, I_C is equal to alpha I by 2.

So, therefore as I discussed with you that V_{CC} or output V_{out} will be equals to V_{CC} minus I_C times R_C right, so I get V_{CC} minus I_C is nothing but alpha I by 2 into R_C this is equals to V_0, right. Now you see, since it is perfectly symmetrical this output voltage and this output voltage are exactly goes to each other. So, if you if you want to find out the differential of that means if you subtract V_{out1} - V_{out2}, V_{out1} - V_{out2} automatically I will get a 0 volt.

Which means that, it is very, very important stage that any bias equal bias given or DC bias equal bias given to the two base of a symmetric differential amplifier the output will always be equal to 0, right. So, DC bias and equal biases to both the arms does not give you a differential output voltage. Now, with this knowledge or with this idea let me move forward and maybe show it to something else.

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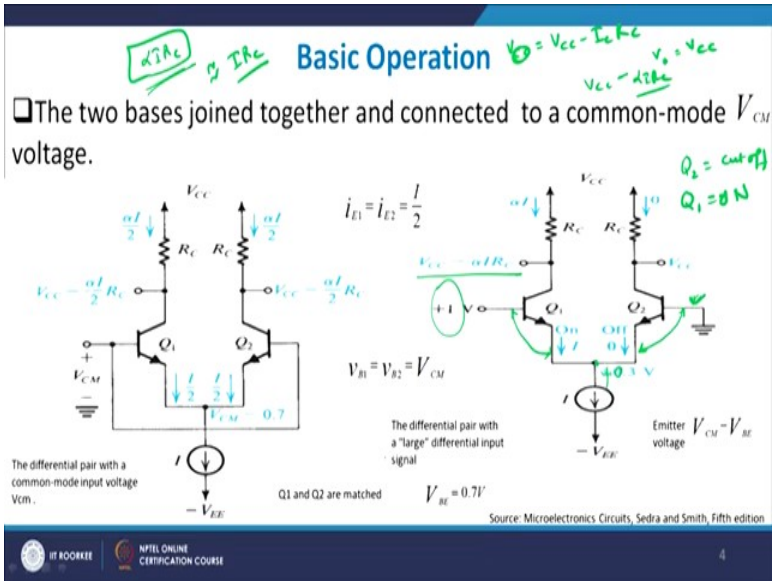

That now, what I do is? I make a small change that at Q 2, I ground it base of Q 2 is grounded and my base of Q 1 is given 0.7 volts, so what will happen is? So, this Q 1 will have this again 0.7 volt here, so 1 minus 0.7 you will achieve a point 3 volt here, right. Now, if you give a base which is grounded, so base to emitter junction will be just 0.3 now because this is 0 and this is plus point 3 please understand this an npn transistor, so you reverse biasing a your emitter base Junction, right.

And therefore Q 2 will be basically cut-off and Q 1 will be on, I hope you agree with this point that Q 1 will be on and Q 2 will be off. Which means that, Q 1 will be responsible for biasing all the currents through it on to IC, fine and therefore as you can see here if you if by again by the previous statement which I gave you, we sorry V_{out} will be equals to V_{CC} - I_C*R_C.

Now, if you if you see I_C a for the right arm Q 2 I_C equals to 0, so V_{out} will be equals to V_{CC} and for the left arm it is V_{CC} minus alpha by 2, it only alpha by 2 divided alpha I R_C, see VCC minus alpha I R_C, fine. Now, if you find the difference between this and this, what the answer you will get is alpha IR_C, right. Which means that if I give a difference voltage of + 1 volt

between the left arm and right arm I get output which is basically a DC output and is given by alpha I times R_C, alpha is very close to 1.

So I Can approximately this to be as it equals to I times RC where I is the current flowing through the device. This is with the assumption that Q 2 is perfectly off and Q 1 is perfectly on and all the current is routed through Q 1 all the current of this current source is routed through Q 1, so, this is with the basic assumption is there. Now, so Q 1 and Q 2 are matched I am assuming this to be true right.

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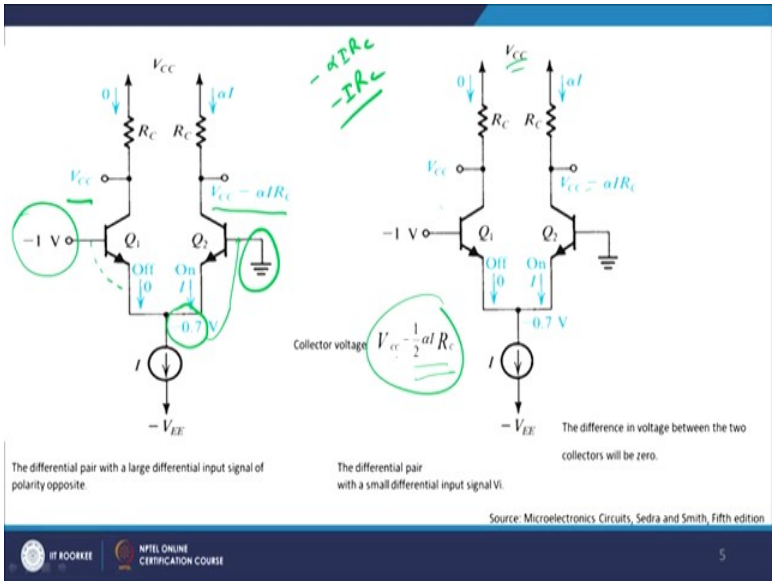

Now, let me do one small thing and let me make a small change once again. With this let me say, that now let me say my Q 2 was grounded, right but my Q 1 I have given a minus 1 volt here which means that if this is minus 1 volt here and if this is grounded, right assuming this there is a potential drop here, I will get 0.7 minus 0.7 volts here, minus 0.7 primarily means that this will be 0 bias between this and this it will be 0 bias.

So, what it will happen is? That Q 2 will be now on and Q 1 will be off, right. So, understand the relationship I am going for both the positive swing and the negative swing in my input when I did a positive swing my Q 1 was on and Q 2 was off with Q 2 grounded with my negative swing of course Q 1 will go off and Q 2 will on, why? Because my Q 1 is going to have because you are reverse biasing the emitter base Junction and therefore Q 1 goes to off state but then this ensures that Q 2 goes to a non-state because minimum point 7 volt is already there between the emitter base Junction.

And therefore it will be an on state and therefore the reverse will happen that my V_{out} 1 will be equal to V_{CC} and V_{out2} will be equal to V_{CC} minus alpha times I_C and therefore the output will be actually equals to minus alpha IRC assuming alpha to be approximately equals to 1, I get output 2 because 2 IR_C. let us see, so with this basic knowledge what things we have been able to found out? We have been able to recapitulate or found out or find out that if same voltage is given to the two base of the inverter BJT the output will be always equals to 0, right.

What therefore, what does the differential amplifier do? It tries to sense the difference between the two signals and then tries to amplify it, right so that is the reason it is known as a differential amplifier. So, if you look at the collector voltage, it is V_{CC} right minus I_C so it is alpha I by 2 into R_C provided both the devices are on, I get minus alpha by 2 alpha I by 2 into R_C which is V_{CC} minus alpha R_C.

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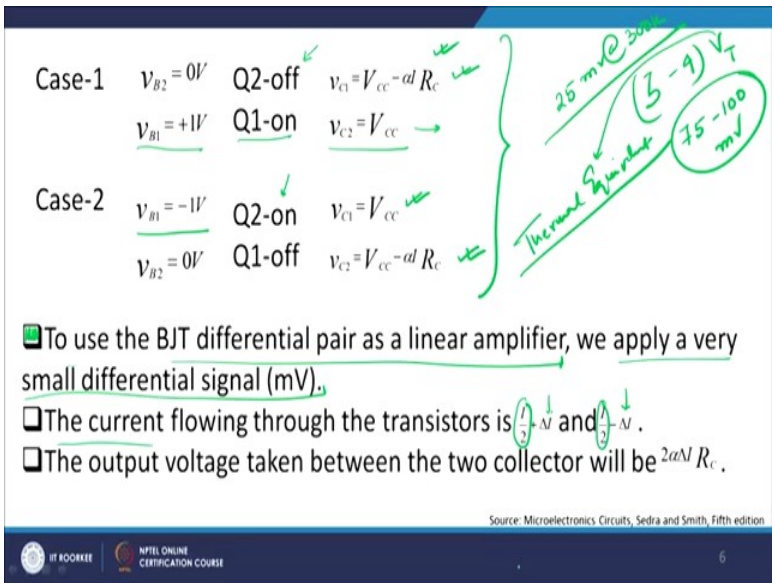

With this knowledge or with this basic idea, let me therefore move on. So, as I discussed with you in the first case Q 2 will be off and therefore V C1 will be equals to V_{CC} minus alpha I times R_C and V_{B1} when it is plus 1 volt Q 1 will be on and then V_{C2} will be equals to V_{CC}. So, whichever the transistor is off the output will be latched to V_{CC} and whichever transistor is on the output will be latched to V_{CC} minus alpha R_C.

In case two when you get V_{B1} is equals to minus 1 volt in that case Q 2 will be on as I discussed with you and therefore Q 1 will be off, Q 1 off implies that VC1 will be equal to V_{CC} and Q 2 on implies that V_{C2} will be equals to V_{CC} minus alpha IR_C. so, all the current is

routed through Q 2 now. So, there are two cases across which the differential amplifier to work.

Therefore just see this point which I am shading here, that to use the differential amplifier BJT differential amplifier, as a linear amplifier linear amplifier means? That the gain is independent of the input voltage, a fixed gain is available to me, we have to apply a very small differential signal of the order of few millivolts, right. Typically generally it is approximately 3 to 4 V_T we say, if the difference is this much we will expect to see a change 3 to 4 V_T is approximately 200 millivolt difference would be there, V_T is thermally equivalent voltage is approximately equals to at 300 Kelvin.

This is, we have already discussed this point is known as thermal equivalent voltage which means that minimum difference of 3 to 4 V_T should be there for the switching or cut-off or switching to be proper. Now, therefore the current through the transistors, the second point will be I by 2 plus delta I and then I by 2 minus delta I, you understand reason why it is, in one case it is minus 1, once case it is plus?

And the reason is something like this, that assuming that as I discuss with you in the previous slides, let us suppose let me just explain to you here, right and I explained here, ok. Let me explain to you, therefore if I give up in one case if I give a base voltage which is higher in another case I reduce the base voltage then the current here will be larger and on the right hand side it will be smaller. So, I will just explain to you what I am trying to say.

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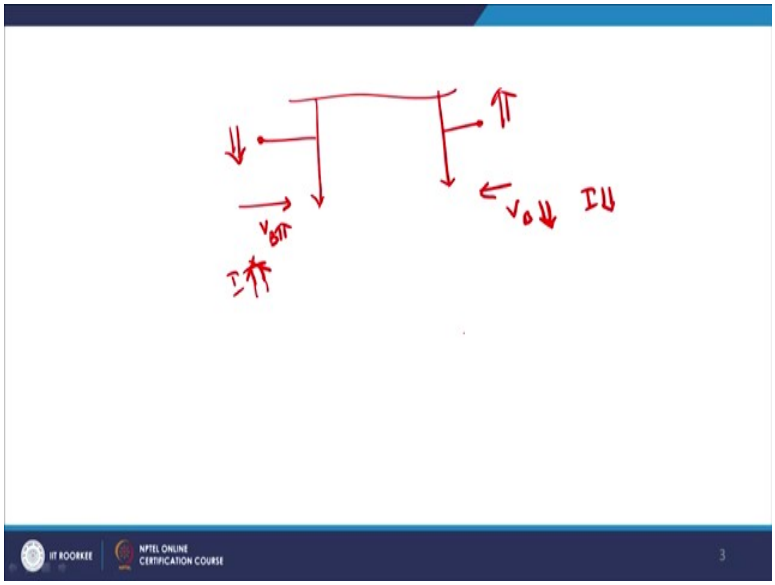

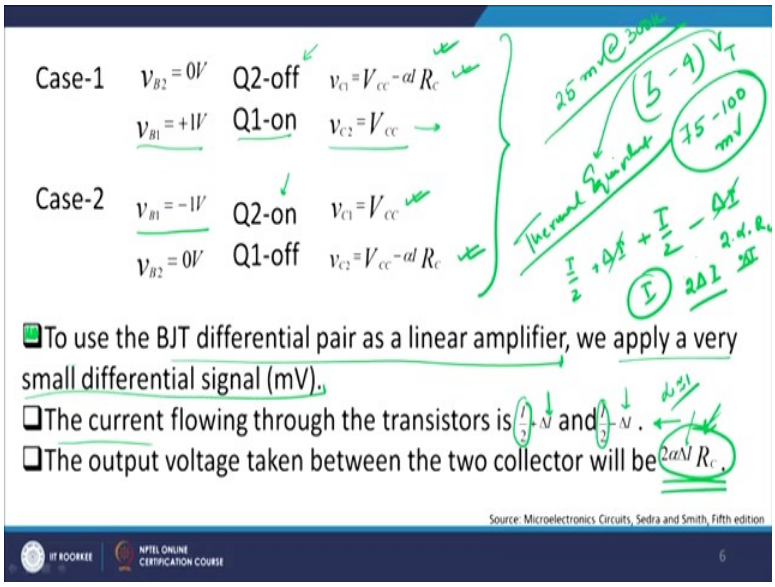

Let us suppose, that I have got two arms here right and these two arms are going on here, in this arm I increase the base voltage V_B and in this arm I reduce the base voltage V_B, so if I increase it the current becomes larger, right the current increases, as the current increases this voltage will drop down here. Similarly, when the base voltage reduces the current reduces and therefore the voltage at this point actually increases.

So, if I therefore make my base voltage make it a differential base voltage, the current will be also differential in both arms and therefore the voltage will also be differentiating in both the arms, that is what I am try to say in the second statement here. Secondly that delta I and plus delta I minus delta I. So one, in one case with the base voltage is increased there will be

increase in the current plus delta I and in another case where there is a decrease there will be a change in the value of current.

But please understand this delta I will always be same for both arms because if you add these two together I should get I, so I by 2 right plus delta I plus I by 2 minus delta I if you see this cancels off and if you add these two I get I, which is the basic emitter current from the current source, submit violating the basic principle, right and that is the reason this is this thing. And therefore, if you want to take the output you will get 2 times alpha delta I by R_C, right.

It will be 2 times alpha times delta into R_C, how why he will get two times alpha ? the reason being you get you when you, so when you subtract the two together I get, so if I if you subtract say for example the current is I by 2 plus delta I, so if you add those to subtract the 2 I get I my 2 cancels out and I get 2 delta IComing into picture, so I get 2 delta I by primal means that 2 times alpha times R_C times, right I get delta I which is basically I here, so, I get this much delta I to be this much, so I get this much as the current.

So what, which means that output voltage difference will be higher provided the current difference is also higher, right alpha is typically very close to 1, so that does not play a major role, so delta I higher the delta I value larger will be the differential voltage output difference between the two.

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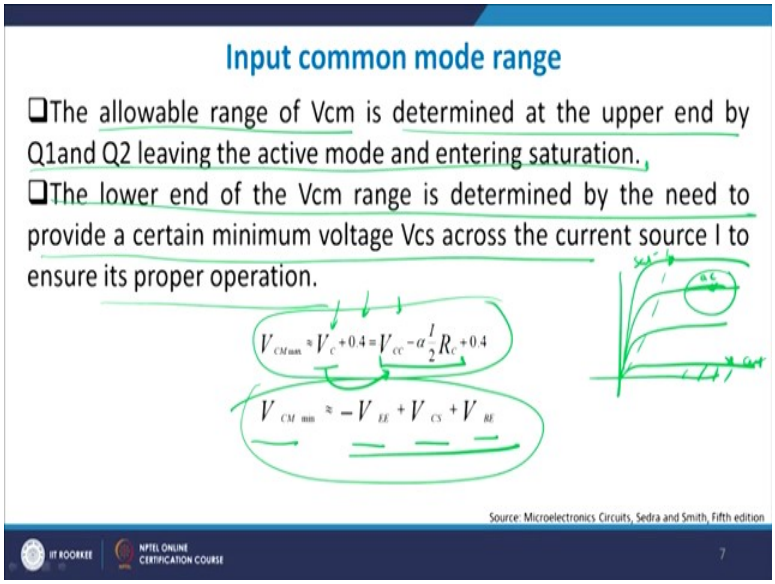

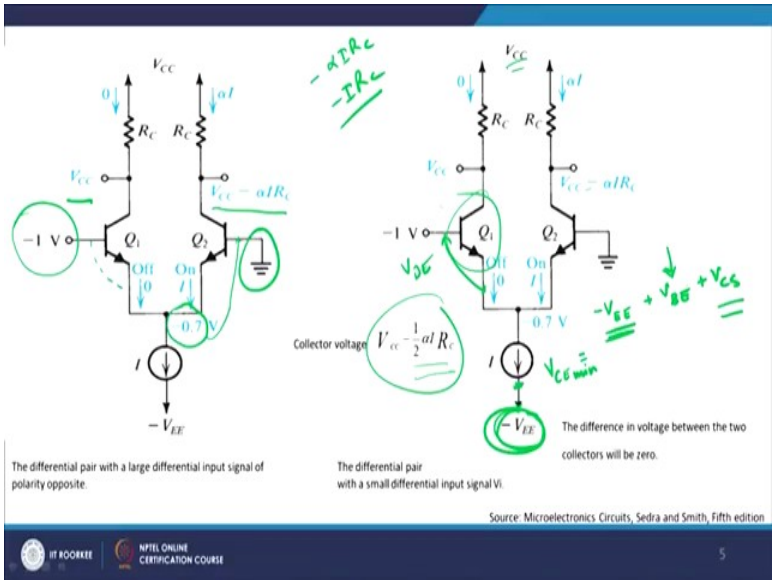

Now, let us see, what is the allowable common mode voltage? So, the initial voltage is the DC voltage which I am giving to a Q 1 and Q 2 before actually inserting AC bias over superimposing over it. Let us see till what point V_{CM} is allowed, right. Now, the allowable as you can see the allowable range of V_{CM} common mode voltage is determined at the upper end by Q 1 and Q 2 leaving the active mode and entering into saturation mode.

So, what I ensure is that both Q 1 and Q 2 should be in the active mode and from active, it should go back to cut-off and my higher limit of V_{CM} should be such that, that it does not allow you to go into saturation, so I am sitting somewhere in the edge of my active region, please understand this very carefully that if you remember from your basic when we are discussing the BJT and npn transistors, we saw this to be as the saturation region, so this was my active, right this is a saturation region and this was my cut-off, this is cut off below this is cut-off.

So, if you are biasing somewhere here, then you do not bias it very close to saturation region, keep it very much in the active region because even amplification to be there but the highest value of common mode voltage which you can put is basically somewhere here, right and the lowest value is somewhere here. So, the highest value is very near to saturation and the very lowest value is near cut-off, but you do not keep it there because then small change in V_{CM} will result in the device going into saturation and thereby reducing your speed or going to cut off and thereby giving you as erroneous output result.

So, keep it in the middle to find out. The, that is what I will say, the lower end of the V_{CM} range is determined by the need to provide a certain minimum voltage across the current

source to ensure the operation. So, let us see what is V_{cmax}? V_{cmax} typically is the collector voltage which you give plus 0.4 which is nothing but V_{CC} minus alpha into I by 2 into R_C plus R_C.

So, this V_c is nothing but this whole thing, right and a V_{CC} minus alpha into I by 2 R_C plus 0.4 approximately and V_{cmin} is equals to minus V_{EE} plus V_{CS} plus V_{BE}, why? Please understand, why is it like that. If you go back to a previous slide, you see you have bias this with minus V_{EE}, right and this is your base to emitter voltage V_{BE}, so what was written here? It was written as minus V_{EE}, right.

So, minus, so I will write down sorry, minus so it is minus V_{EE} plus sorry, plus V_{BE}, right plus V_{BE} plus V_{CS}, right. So, this minus V_{EE} is and I am saying this to be as approximately the value of your $V_{CE\ min}$, minimum value why? Because any volt, see so for the device to be on state I require minimal V_{BE} to be potential given to the base side otherwise it will go into off state.

So, assuming that your V_{BE}, Q 1 is in the on state, I have to give a minimum voltage of 0.7 V_{BE} onto the Q point, so that takes care of this one, right is it ok, what is V_{EE}? V_{EE} is this potential, so minimum this potential has to be there in order, so because this potential is appearing so this is basically a V_{EE} and this potential is appearing somewhere at the edge of your current source here, right.

So, the minimum amount of DC bias, so because if you do not give this much amount this will actually reverse bias your sorry, it will forward bias it will give one every time and therefore you require minus V_{EE} as one of the point and we V_{CS} is basically the collector to source potential, which you need to add to V_{BE} in order to ensure that the device is non-state.

So, the requirement therefore is that for the V_{cmax} common mode max is given by this and common mode min is given by this, right. So, if your V_{CC} is typically around 3 volts or 4 volts or 5 volts then you can see what is the value of $V_{CM\ max}$. so, higher the value of V_{CC} more you can go for V_{cmax} without entering into the saturation region of operation and the critical part is that we do not allow it to enter in the saturation region because then it compromises in the speed of the device, right.

Let us look at the therefore the, we have understood therefore the small signal amount not the small signal amount it, the basic operation. So, what I will do? Is I will give a differential voltage here, if therefore I will get a 180 degree phase shift at signal between Q 1 and Q 2, I

will get an output which is 180 degree phase shifted if you therefore take the difference of the two collector voltages, the output voltage will be twice and therefore I will get a differential of twice approximately.

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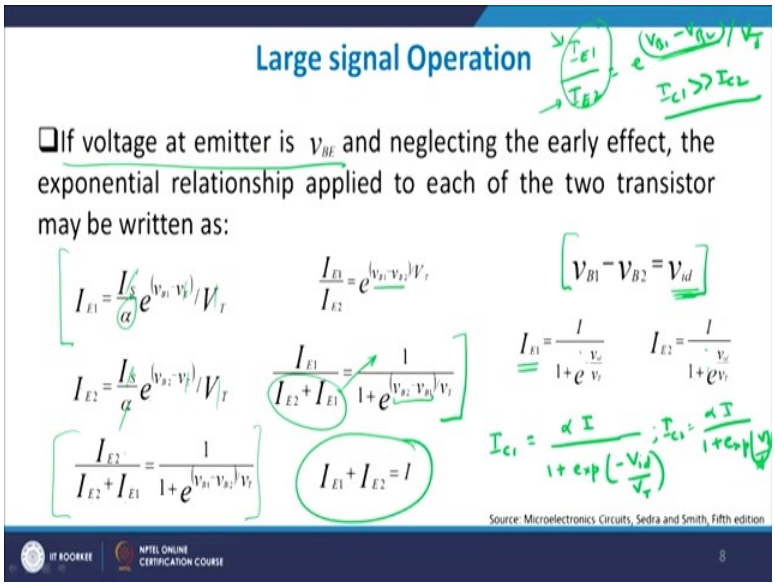

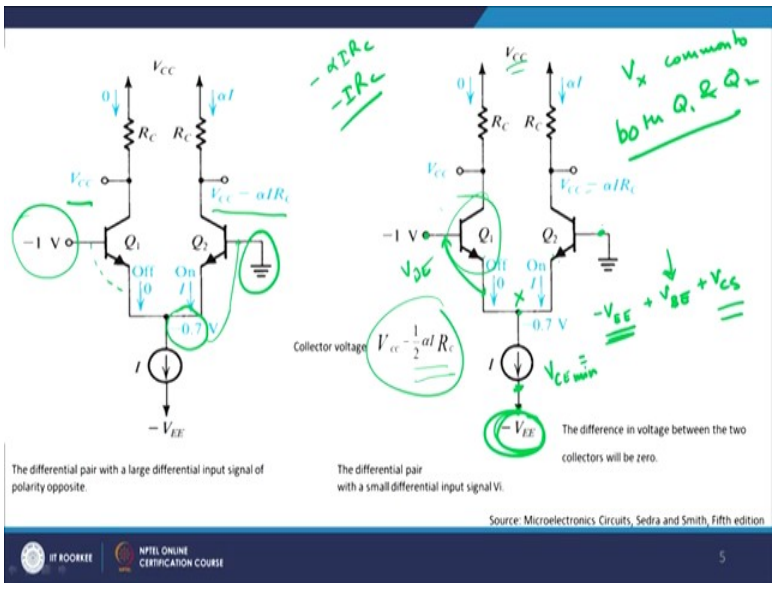

Now, if obviously if the voltage at the emitter is given by V_{BE} and therefore assuming that there is no early effect then I Can safely write down the emitter voltage I_E to be equals to I_S by alpha, IS by alpha into e to the power V_{B1}, V_{B1} minus V_E by V_T, my basic semiconductor equation and V_{E2} equals to I_S by alpha into e to the power V_{B2} - V_E. Now, if you add and therefore this equation if you do like this manipulation, I get this into consideration and if I do some I_E, so the I_{E2} by I_{E1} plus I_{E2}, I get this, I will also get I_{E1} by I_{E1} plus I_{E2} equals to this, right.

Now, you see so I_{E1} by I_{E2}, I_{E1} by I_{E2} this will cancel off, right this will cancel off, this will cancel off sorry, this will remain there and therefore we I_{E1} by I_{E2} is equals to e to the power V_{B1} minus V_{B2} by V_T and there even without knowing the physics of the device you can appreciate that higher this difference between the base (voltage) voltages, right more will be the ratio this one.

So, which means that if V_{B1} is much, much larger as compared to V_{B2}, right everything else remaining the same I_{E1} will obviously be much larger as compared to I_{E2} and therefore I_{C1} will also be much, much larger as compared to I_{C2}. So, that is the bottom like a or that is the sort of a the whole crux of the whole issue, that I need to make one side base voltage much larger as compared to another side.

Now, I we also know that I_{E1} plus I_{E2} will be always equals to I, you see this one and we refer to V_{BI} minus V_{B2} as $V i_d$, i_d means input difference, input difference between the two, why we are saying input difference between the two? Because you see, this potential is always constant, right I will just come back to the previous slide and you will explain, this potential is always common to the both the emitters of Q 1 and Q 2.

So, let me name it as X then V_X is common to both Q 1 and Q 2 therefore since this is common to both I just need to find out the difference between this voltage and this voltage that is all, so that is the reason I am referring to this as V_{B1} minus V_{B2}, right I am forgetting the common node because unnecessarily complicate the matters and therefore I refer VB1 minus V_{B2} equals to v_{id}.

Therefore I Can write down, I_E, right I_{E1} to b equals to I_{E1} to be, so this is basically your I, so this is I this I, I am take it in the numerator and I get I_{E1} plus e to the power V_{B1} minus V_{B2} is V_{id}. So, V_{id} minus V_{id} by V_2 and I_{E2} equals to I upon 1 plus V_{id} by e to exponential plus V_{id} $_2$, right. So, 1 is a got a negative sign and other is good as a positive sign.

So, these are the emitter currents which are available to us right and if you want to just find out the collector current you multiply this with alpha, so I_{C1} will be equals to alpha times I upon 1 plus exponential minus V_{id} by V_T right and I_{C2} will be equals to alpha I upon 1 plus exponential V_{id} by V_T, fine, ok.

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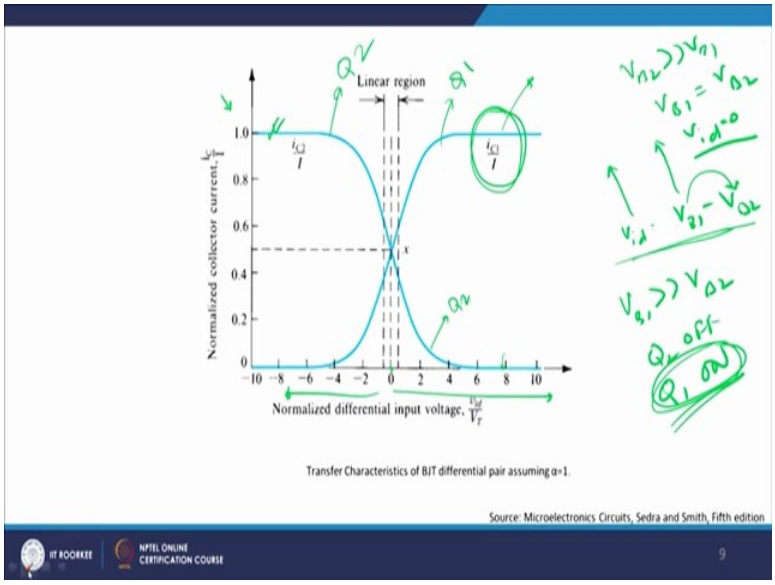

Now, with this knowledge which you have gained till now, right let me just therefore give you a small idea about the transfer characteristics. Now, on the y axis you will see it is basically the normalized collector current which means that collector current normalized with respect to the total current which is available to us and therefore the maximum I Can go is 1 and on the x axis we have V_{id} by V_T, V_{id} is basically the difference voltage of the base

So, V_{id} is as I discussed with you is basically V_{B1} minus V_{B2}, right so if we divide that by V_T thermal equivalent voltage this is what I get, this is the point 0 where V_{BI1} equals to V V_{I2}, right and as you move to the left or right let us see how it works out. As you move to the let us suppose left, right as we move to the left or let us say we are moving to the right that is more easy to understand.

It primarily means that my moving to the right means this is becoming more and more positive which means that VB1 is becoming more and more higher as compared to, so V_{B1} is getting higher and higher as compared to V_{B2} which therefore means that the Q 2 is in the off state and Q 1 is in the on state, when Q 2 is in the off state obviously so sorry, when Q 1 in the on state I will get on current available here at this particular point, right.

And therefore, if you look very carefully that as I and therefore as you can see the collector current which is flowing, now when you make it V_{id} very, very large right this is very, very large as compared to V_{B2}, right so Q 1 is in the on state, right Q 1 is my on state, Q 1 is in the on state primarily meaning that you have a large collector current available to it and therefore you see you have large collector current I_{C1} by I is the large collector current whereas since

already Q 2 is a switched off mode the current goes to 0 and you can see the current goes to 0.

So, this is the Q 2 current and this is Q 1 current sorry, this one is Q 1 current and this is Q 2 current. Similarly, if we go to extreme left somewhere here then V_{B2} will be much, much larger as compared to V_{B1} and therefore your second Q 2 will be on having a large current and Q 1 will be off. So, this is C is a perfectly symmetrical sort of a butterfly available with, it is a perfectly symmetrical, somewhere in the middle where you will have V_{B1} equals to V_{B2} which means that V_{id} equals to 0 you automatically get a place where the current changes drastically with respect to V_{id}.

So, we will start from here in the next slide in the in our next discussion, we will see how it works out and we will discuss from the linear region of operation, how we can move ahead and give you the value of CMRR and give you the value of the differential mode common signal, right thank you, thanks a lot.