**Microelectronics: Devices to Circuits**
**Professor Sudeb Dasgupta**
**Department of Electronics and Communication Engineering**
**Indian Institute of Technology Roorkee**
**Lecture 32**
**JFET, Structure and Operation**

Hello everybody and welcome again to the NPTEL online certification course on Microelectronics: Devices to Circuits. In our previous lecture schedule, we had seen how a common source amplifier works and what do you mean by mid band frequency? What do you mean by lower cutoff frequency? And what do you mean by higher cutoff frequency or upper cutoff frequency? How do you define bandwidth? What is the meaning of gain bandwidth product? And this is one of the figures of merits which we have discussed.

We also saw, why does the gain false of at relatively high frequencies and low frequencies and remain stable, independent of the applied frequency somewhere in the mid band. Then we saw the mathematics of it and we saw that, if we do have common source design at low frequencies at the device the capacitance are open circuited and high frequency is there shorted.

We are left with two important parts which we did not carry forwarded in the previous lecture series and that is what we have actually seen is the Miller capacitance is, we have already discussed with them together but I will just refurbish you memories here.

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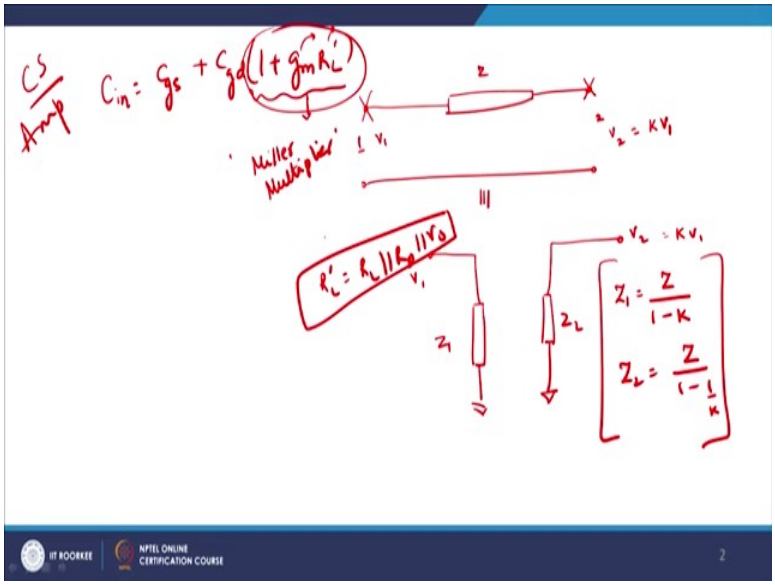

So, let us suppose I have I want to just refurbish the whole thing. So, I will let us have a two port network, this is port one and this is port two and I have V1 is the voltage source at port 1 and I say at port 2 the voltage V2 is equals to k * V1, which means that the voltage at V2 is a function of V1, right. So, there is sort of feedback loop between nodes 2 and 1, right.

Now, this can be replicated as that is sort of string is, it can be replicated as like this, right where this is basically is z1, this is v1 once again and this is z2 and this is again replicated where this is v2 and where we supposed to be is k * V1 where we can write down Z1 = z / 1-k and Z2 = Z1 /( 1 – 1/k ).

Now, formal proof at this stage is beyond the scope of this course but this I how it works out which means that, if I ground those two capacitances I get it. Now, in my previous discussion we saw that when we doing high frequency response we that saw that C in will be equal to $C_{gs}$ for a common source amplifier, for a common source amplifier $C_{gs} + C_{gd}(1+ g_m * R_L')$ right this is high frequency response which you got, where $R_L'$ is nothing but the resistance $R_L \| R_D \| r_o$, right.

So, this is basically your $R_L'$, right and this quantity is referred to as a Miller multiplier, Miller multiplier which means that? The gate to drain capacitors which was initially a low value in reality gets multiplied with $1 + g_m * R_L'$ and gives effectively gives you a larger value which means the reason been gm is typically large, right $R_L$ is also large, so this quantity is a relatively large quantity.

So, that means even if the gate to drain capacitance is small it is effect on the output is relatively large, right that is what I wanted to give you an idea about place an idea about. And the reason being that which means that therefore when two ports are connected by an impedance just as gate and drain current at through a gate impedance then we can refurbish or re-clarify it and we get this structure into consideration, right and this is what we get as the output capacitances.

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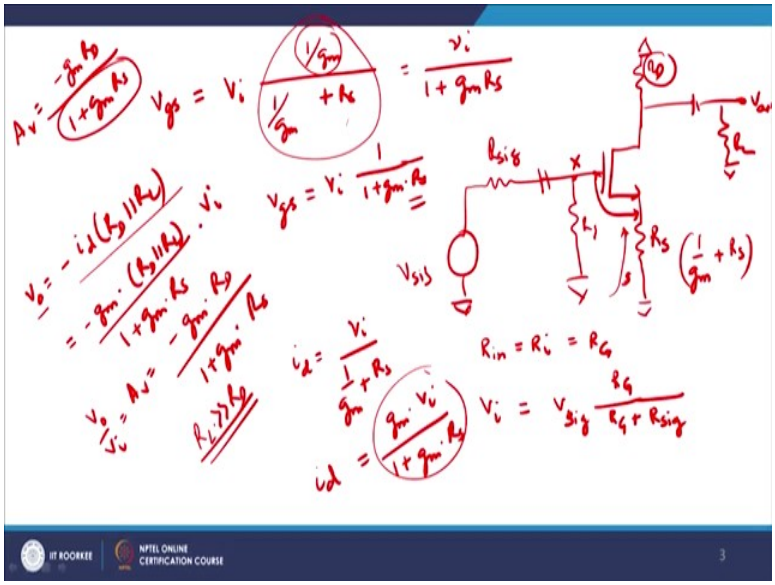


Now, let me come to, we have also seen that, sorry we have also seen that there was a source degeneration resistance concept which we have seen, right. And we saw that if that is true which means that if I have got a common gate that means I have got a this, this and now capacitance here and I am driving by $V_{sig}$, right and I also have a resistance here, right this is your $R_g$ and you have $R_D$ here, right and then this is a cap here and then you have $R_L$ here, right and this is your $V_{out}$ and this is your $V_{dd}$ , let me save ground and gate.

Now, under these criteria this is also referred to as source resistance Rs, right and what happens is that? The effective resistance seen from the source side is basically $1 / g_m + R_s$, fine. So, if you look from the source side which is a source end of this MOS device, the effective resistance seen by the devices $1 / g_m + R_s$, with this knowledge let me write down for you Rin to be equals to $R_i$ that is equals to almost equals to $R_G$, right because the gate resistance is the largest one and you get this.

Therefore I get Vi input voltage which mean input voltage is the voltage at this particular point at point x will be equal to $V_{sig}$ signal, right signal * $R_G + R_{sig}$, so this is Rsig, right. So, $V_i$ equals to $V_{sig}$ * $R_{sig}$, so this is basically potential divider network which you see. Therefore I can safely write down $V_{gs}$, right equals to $V_i$ * $((1 / g_m) / (1 / g_m) + R_s)$, why? Very simple, if you look $V_{gs}$ is gate to source voltage which is applied here, right $V_{gs}$ is the gate to source voltage, gate to source voltage, this one.

Will be nothing but, so not all of $V_i$ will appear as gate to source voltage apart of it will appear across gate to source voltage depending on this value of $((1 / g_m) / (1 / g_m)$, why?

Because this is the resistance of the device itself and this is the resistance of the device shrink from the source side and therefore if we divide it I get this into consideration, this will be approximately equals to $V_i$ / ( 1 + $g_m$ * $R_s$).

So, if you if therefore, if you find out $V_{GS}$ therefore, I am sure to be Vi *( 1 / 1 + $g_m$ * $R_s$ ), right and this is the source resistance which you see, right. Therefore, if I want to find out the drain current $i_d$, will be given as Vi / ( 1 / $g_m$ + $R_s$ ) and this will be approximately equals to ( $g_m$ * $V_i$ ) / ( 1 + $g_m$ * $R_s$ ) is equals to $i_d$, right. Now, we very well know that Vo output voltage will be - $i_d$ , right $R_D$ || $R_L$, where $R_D$ and $R_L$ what?

Suppose this is $R_L$, this is $R_D$ then we define V0 equals to -id phase is change is there therefore there is negative sign. So, I can safely write down this to be as - $g_m$ * $R_D$ || $R_L$, right divided by (1 + $g_m$*$R_s$) * $V_i$, this is what we are doing, we are placing it here and plugging it here and therefore $V_0$ / $V_i$ which is nothing but Av gain is equals to – ($g_m$ * $R_D$)/ 1 + $g_m$*$R_s$ where $R_D$ is the drain resist.

If you actually see the overall resistance assuming that your $R_L$ is much, much larger as compare to $R_D$ and this is true also, right. So, I get overall gain $A_v$ to be equals to - $g_m$*$R_D$/ (1 + $g_m$*$R_s$). So, if you look very carefully or if you want to have look into the careful consideration we will see that your presence of Rs actually lowers the gain, right and it makes the gain low because as you increase the value of Rs at the denominator increases and as a result it becomes slow and as a result what happens is ?

That your gain starts to fall down but the interesting part is that, as I discussed today earlier also that this presence of Rs actually helps you to do a negative feedback and stabilizes it. So, though your gain falls down your bandwidth increases because the gain bandwidth product is always fixed for a system, right. So, that is the advantage of having this resistance as available to you.

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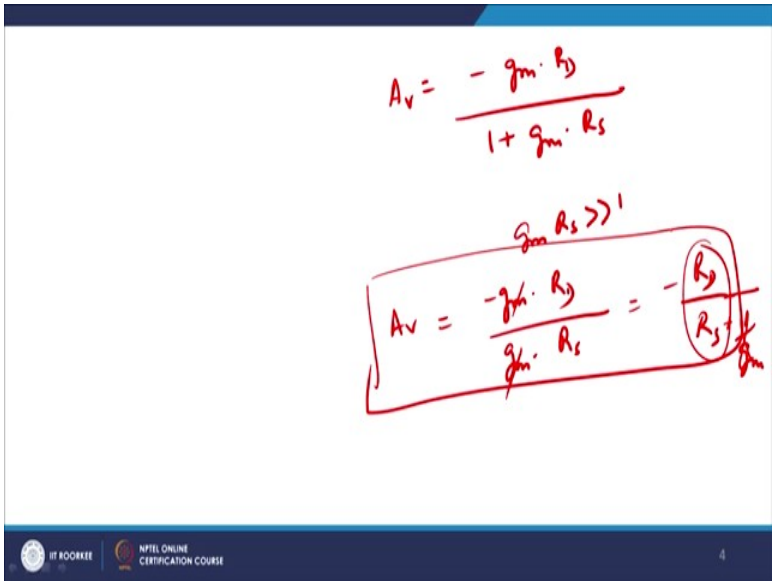


Now, if you look at this equation here, so let me just write down in a clearer fashion that Av equals to - $g_m$ * $R_D$ / ( 1 + $g_m$*$R_s$ ). Now, obviously $g_m$ * $R_s$ is much larger as compare to 1 therefore I can safely write down Av to be equals to - $g_m$ * $R_D$ / $g_m$ * $R_s$, right. So, this gm cancels out and you are left with minus $R_D$ / Rs equals to gain, right which means that if you want to find out the gain just by inspection, look at the drain resistance, look at the source resistance.

But there is an issue here that you will see the source resistance extra term 1 / $g_m$ will also come into picture, right because when you sweep in the source side that is the extra gm which you which as come already if you remember correctly it is already come. So, you need not put this one but typically $R_D$ by R $_s$ will be the value of $A_v$ which you need get in such a scenario, right. So, this is what we get from a previous discussion and our knowledge as far as this design is concerned. We have also understood the basic concept, let me come to the next one, which is basically a common gate design, right.

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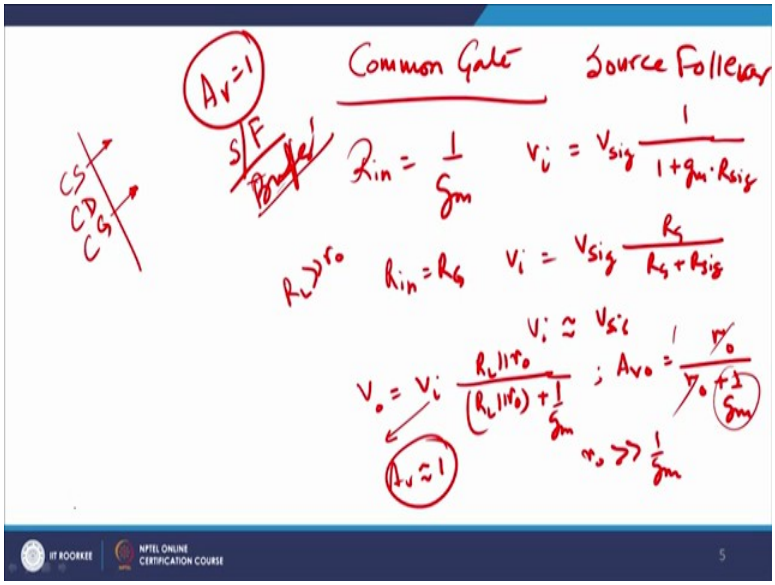


Common gate, gate is grounded and therefore, I so I can do common gate design not very seldom used to it, it is not basically seldom used it is also known as a source follower design which means that it is gain is almost equals to 1. So, Rin equals to 1 / $g_m$ as I discussed with you, Vi equals to $V_{sig}$ 1 + $g_m$ * $R_{sig}$, right and therefore I get $R_{in}$ equals to $R_G$ approximately and therefore I get $V_i$ equals to $V_{sig}$ into $R_G$ /$R_G$ + $R_{sig}$.

So, therefore Vi will be approximately equals to $V_{sig}$ because $R_G$ or $R_{sig}$ because $R_{sig}$ is very small as compared to RG. So, I get $V_0$ to be equals to $V_i$ into $R_L$ parallel to $r_0$, right into $R_L$ || r0, right + 1 / $g_m$, fine and therefore I will get open loop gain $A_{v0}$, so this $V_i$ will come into denominator since $R_L$ is much, much larger as compare to $r_0$, I can really write down this to be as $r_0$ / $r_0$ + 1 / j, right.

Since, in reality $r_0$ is much, much larger as compare to 1 / $g_m$, we can write down $A_v$ to be approximately equals to 1 because this will be very small, this cancels out and I get 1, right. So, in a common gate configuration, the gain is always equals to 1 and therefore it is also referred to as a source follower and generally there used as buffers, right they used as buffer. So, with this discussion we are finished with the three configurations available to us and these key configurations are common source, right.

We have got, you have got common drain and you also have the third type which is common gate. So, there are three configurations, the most seldom used as this one because of it is high gain, this is source follower which you used for impedance matching purposes, right. With this we have finished the basic concept of single stage amplifier, how to design a single stage

amplifier from MOS devices. We now come to a new device, which is the topic of this module and that is known as JFET or junction field effect transistor. We will look into it is structure and it is operation in this module and in the subsequent modules we will discuss other parts of the structure, ok.

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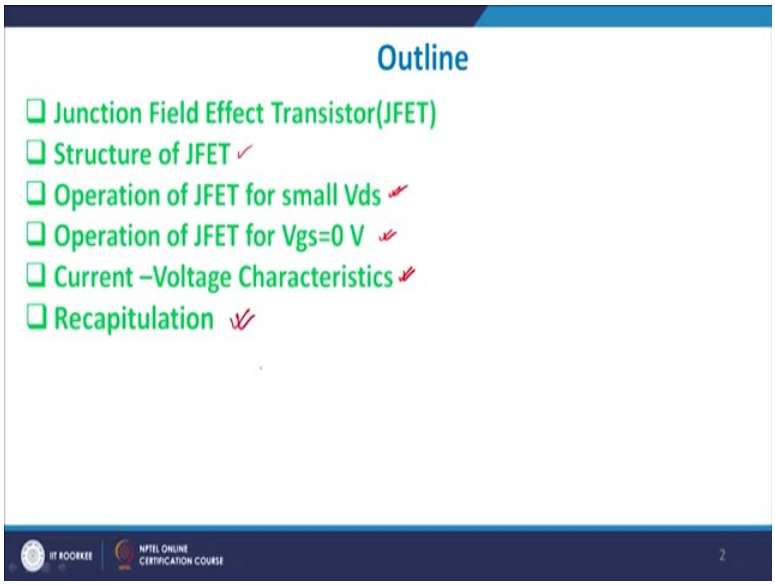


Let me come to the, what will be the outline, the outline will be look into JFET or junction field effect transistor. We will looking it is structure, how it is looks like then how does it operate when you are apply a small drain to source voltage and when you apply $V_{GS}$ is equals to 0, how does it operate? We will look at the I V characteristics and then recapitulate our idea is about JFET, right.

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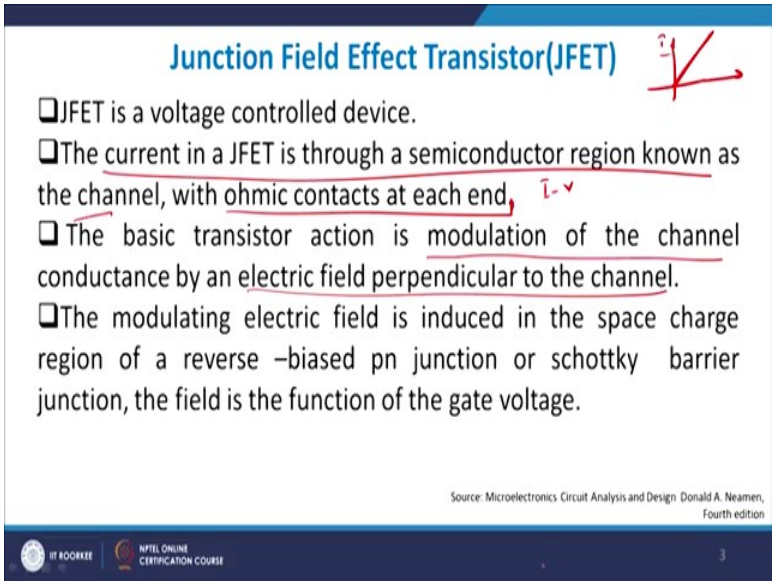


So, it is what we will doing here? So, again as have, as a MOS device, this also voltage control device which means that this basically again a voltage control current source. So, you will be applying a voltage and the current will be changing on the output side. So, the current in the JFET is therefore through a (resi) semi-conductor region known as channel and the with the ohmic contacts at each end, ohmic contacts means? Which follow I V current versus Voltage linear graph.

So, this is basically, this is the ohms law, right because so I versus V, so any contact in which I versus V is a linear graph is basically my ohmic contact, what we will be looking into his how it operates and that operation will be explain to you in subsequent slides. But, the basic transistor action is the modulation of the channel, right by electric field perpendicular to the channel, so which means that it is the something like this.

So, if I have a channel, in suppose a water is flowing through the channel, right then what I do? As I close the channel from outside by pressing it from both the sides, so channel is getting narrower and narrower, then what will happen? The volume of water will reduce, right and as a result, so I increase the volume of water by opening of the channel or decrease it by closing the channel. It is conceptually the same thing exactly happens in a junction field effect transistor and let the see how it is works out, how what it is structure looks like.

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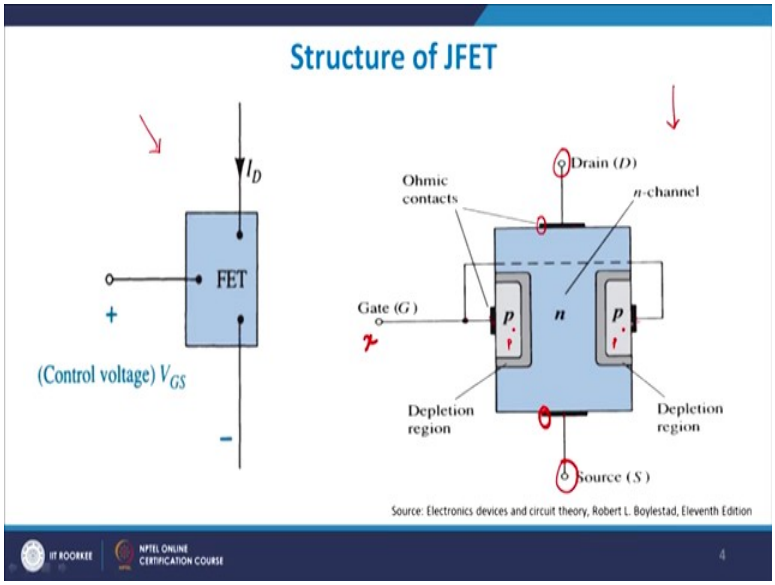


So, if you look at this on the left hand side is the schematic of JFET, on the right hand side would you see here is the actual diagram cross section of a JFET. So, if you look closely I have this ohmic contact here, I have drain region, I have a source region exactly like a MOS device, this is ohmic contact, so it is a basically a metal contact, metal semiconductor contact here, I have a gate region also in ohmic contacts are 1 ohmic, 2 ohmic, 3 ohmic and 4 ohmic contacts then I have a P region, this is basically P type, this is P type and this whole substrate is basically your n type, right this whole substrate is basically n type.

Now, if you look very closely from your previous discussion and these two gates are this gate and this gate are shorted with respect to each other. Which means that, if I give a voltage x here the same voltage appears here as well as here, right so it is known as the (shorted gain) shorted gate or the two gates are shorted with respect to each other. So, the same voltage is applied to both the gates.

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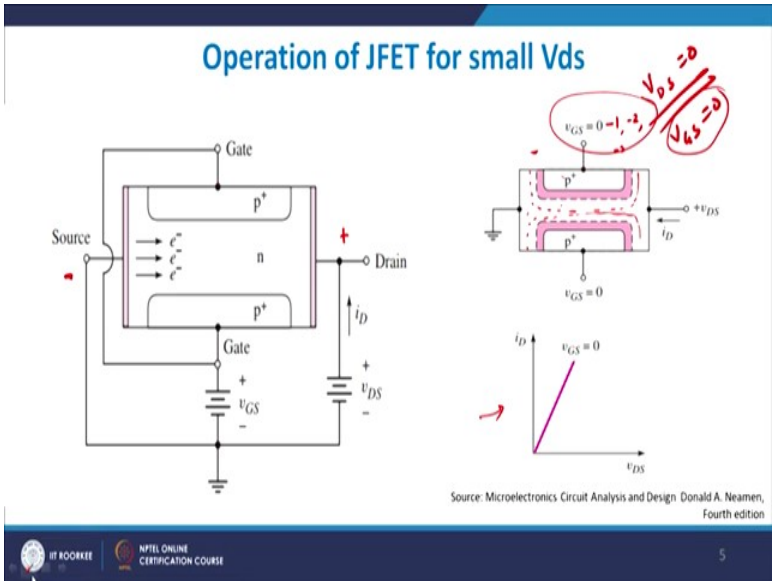


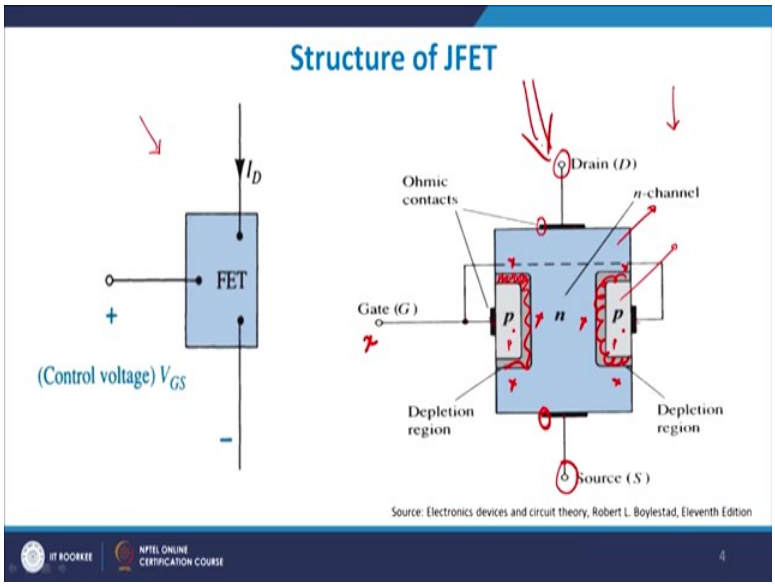


On the such a criteria, we will see (how those) how it works out or how it works in a general sense. So, before we move, so this is a structure which you see, as I discussed with you, the doping concentration here is pretty large, this is also doping concentration is pretty large and drain and source you have metal contact here. Now, as I discussed with you even a without application of any external source or external bias there will be obviously a depletion region is will be here, right.

There will be always a obviously depletion region which will be here, right and this depletion region thickness will depend upon the relative doping concentrations of the P side and n side but the interesting point will be the depletion region will be equally thick here, here as well as here, fine I hope you agree with the statement that the depletion since I am not giving any

bias anywhere all of them look equally reverse biased or forward biased and therefore, the depletion region will be formed equally in all the directions, right because the doping concentration is same across the all the directions.

Now, let us see how it works out. Let me see that you did not you first of all, now let us suppose we explain in this manner that I apply on the gate side, this is the gate voltage I am applying, a positive bias means I have forward biasing the gate with respect to the source and applying a positive bias here and a negative bias here, right, let us see how it works out. Let us suppose I this is like a let me see, will be how we will understand.

Let me see let me put VG, let me have $V_{DS}$ equals to 0, right also my VGS equals to 0 which is exactly the this graph which you see or this profile which you see. Now, what I do is I keep my $V_{DS}$ equals to 0, right and I go on increasing the value of VGS, right and how do I increase it? I make it more and more negative, so -1, -2, -3 and so on and do forth.

So, once I put to the positive sign and negative voltage obviously this will reverse bias with respect to n channel, right and as a result what will happen is? This will grow and this will grow what? Equal in all directions, can we got the point, right. So, will VGS equals to 0 with channel is fully open, you go and increasing the value of VGS keep your $V_{DS}$ constant at this stage, go on increasing the value of VGS in a negative fashion for n channel.

If you have P+ as your source and drain and n as channel will go on, giving more and more negative value to the gate and you will see that the depletion region in the both edges will start drowning together and a time will come when they will approximately touch with each other though that is a debatable issue but they will touch each other and therefore the channel will be lost and therefore even now if you apply a drain voltage nothing will happen because you are the because those areas divide of any free charge carriers, right.

So, this is what I want to do say that by simply application of negative bias on the gates side I was able to control the width of my channel and therefore the net flow of charge carriers from source to drain. Now, with this idea or with this basic concept let me therefore explain to you this graph here which is given at this point. Now, let me do one thing since you understood how a channel will be closed, let me do one thing.

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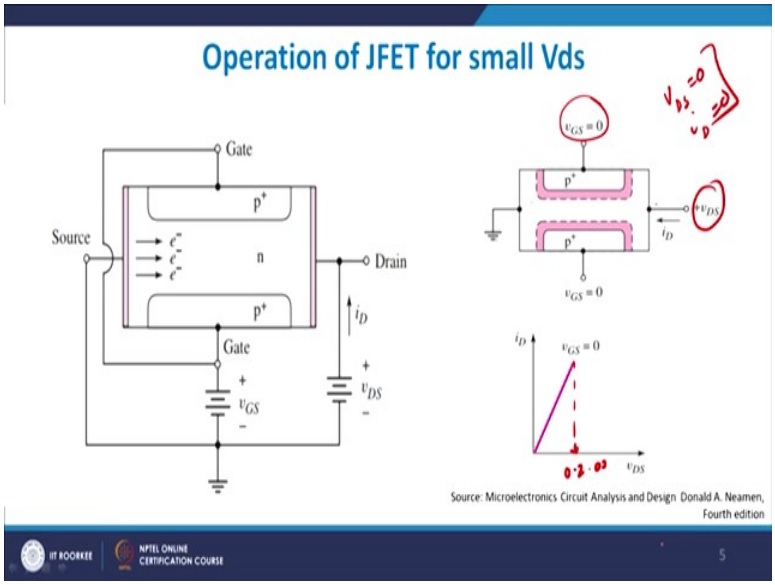


Now, what I do is? I make the VGS equals to 0 and then go on increasing the value of $V_{DS}$ which I am doing it here. So, you will be obviously certain that when $V_{DS}$ equals to 0 when $V_{DS}$ equals to 0, right your $i_D$ will also be equal to 0 because it is no potential, there is no chance of any electric field and therefore when there is no electric field no electrons will be moving from source to drain and as a result, source is grounded and as a result there will be no current but as you go and increasing the value of $V_{DS}$ in a very, very small domain this $V_{DS}$ is relatively very small say 0.2 volt or 0.3 volts, right.

The electrons will be moving and it will move fast from this end to this end and a current will be fall but and quite interestingly and therefore we just compare it with flow of water, I have water is flowing but tap is there I open the tap fully or I open tap and then let I do I start closing it but when I am closing it, I am closing it very slowly at the starting.

So you will not feel the difference in the water flow as such and therefore it will be almost linear increase in the current because you go on increasing the value of $V_{DS}$ more and more electron will be flowing and therefore you will get a larger amount of current. But, understand one important point that and that is quite interesting. Let when you make it $V_{DS}$ larger or larger, right you see say I will give it example to give you an idea about.

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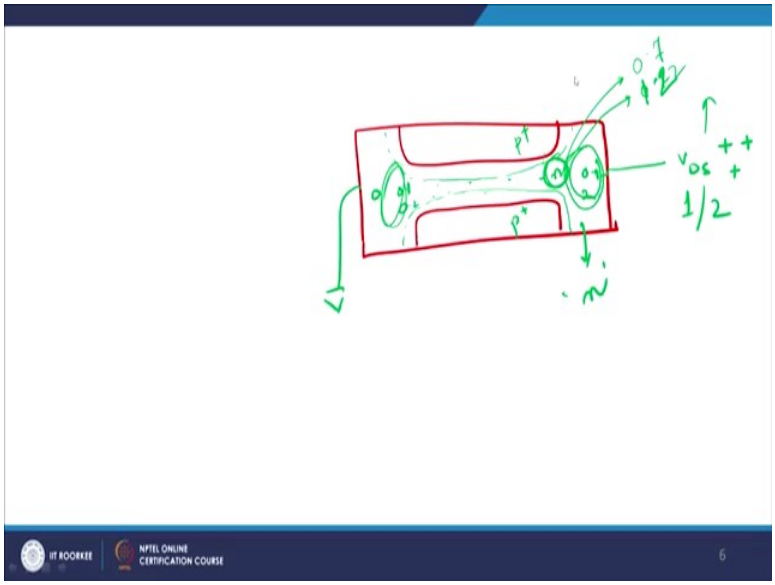


So, let us suppose this is your JFET, right and this is your P+ region, this is your P+ region and then what you do is? You apply a bias and you had a this and this, so assuming it to be equal. Now, you apply a $V_{DS}$ here and we go on and making it more and more positive as you get, so if you apply 1 volt here it means that it is 0, so it is 0.1, 0.2, 0.3, 0.9 and then 1, if it is 2, it is 0.2 here, 3, 4, 5 and then it will come 2 volts here which means that, as you go on and increase the value of $V_{DS}$, this side will become more and more positive as compare to this side means the all the channel will become more positive but this side will be more positive.

So, here it will be 2 volt, here will be, so if you look at very concentrated this point when you apply $V_{DS}$ equals to 1 volt this will be my 0.7, when you apply 2 volts this exactly the same point will be 0.9 maybe or 1.2 maybe, right but understand this is n channel MOSFET, this is n channel JFET. So, within n channel and you would apply a positive bias of the n side your effectively reverse biasing the P plus n region and therefore the depletion region on this side will be larger, right.

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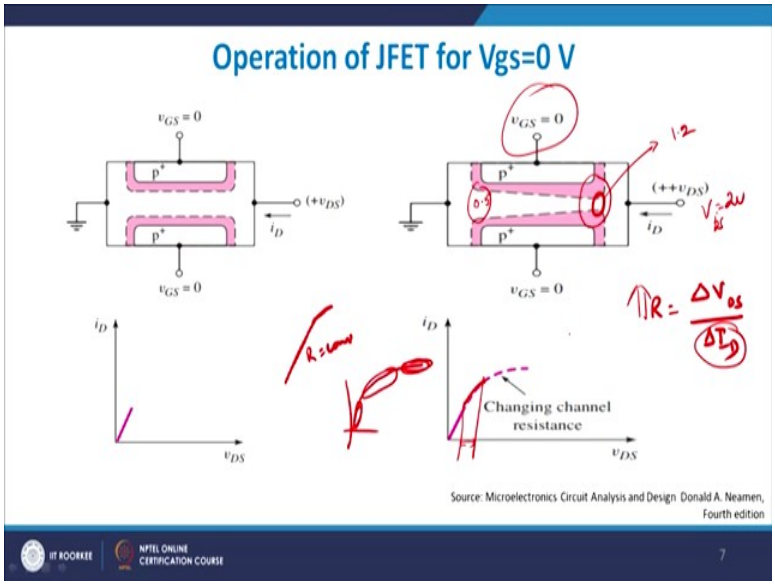


I will just show you what I was trying to say, you see this side depletion region is thicker as compare to this side because what this been see is just it will see 0.5 volts whereas this been see maybe 1.2 volts if you apply $V_{DS}$ equals to 2 volts. So, this side it becomes more and more (thick) more and more thick and therefore your channel starts to shallower and shallower, right it goes and becoming thinner and thinner.

As a result, now what happen is that the channel resistance starts to rise obviously if you are closing something the resistance offered by the channel will become more and more therefore the current which was following linearly straight line starts to show deep here, why? Because if you remember resistance is equals to $\partial (V_{DS}) / \partial (I_D)$. So, when I was in the linear region resistance is constant somewhere here for the same change in the (value), so somewhere here for the same change in the $V_{DS}$ is a smaller change in $I_D$ as therefore this is small and therefore R is large.

So, more the slope is less will be the resistance offered. So, the here is heavy resistance, here is almost very small resistance and here is infinitely large resistance available to you, fine. So, when you take $V_{GS}$ equals to 0, this is can take admission on $V_{GS}$ equals to 0, right and I get this current into profiling. I hope I made myself clear that this is basically with $V_{GS}$ equals to 0, I have increase the value of $V_{DS}$ and I get this into consideration.

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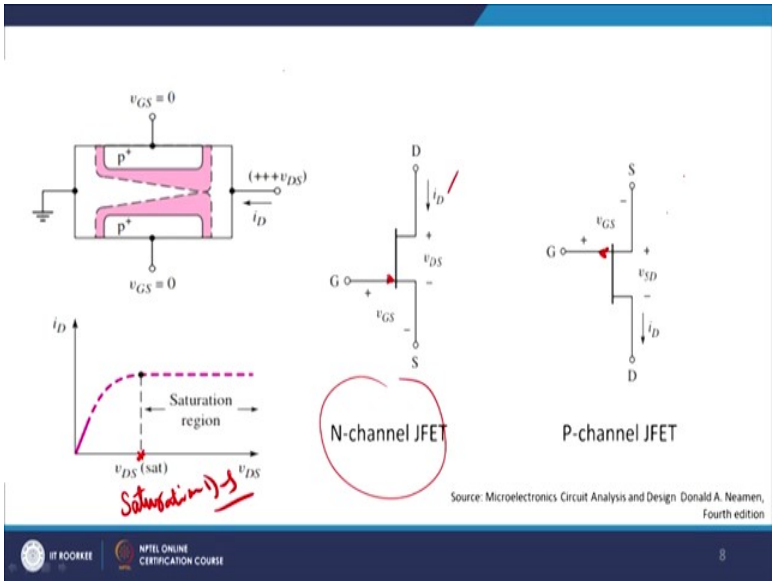


Now, what I do is? Therefore I define a term known as $V_{DS}$ sat or saturation drain to source voltage, saturated saturation drain to source voltage at which? The current gives independent of $V_{DS}$ it is almost too straight line and the resistance offered is infinitely large. This the schematic of n channel JFET and if you look it is pointing gate is pointing inwards and similarly gate is pointing outwards in a P channel JFET and the direction of current is already shown to you, right and this is what JFET look like.

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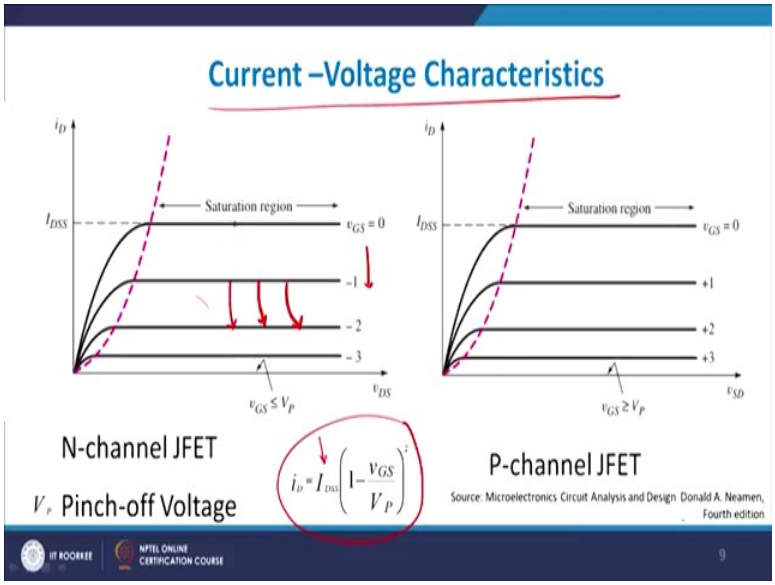

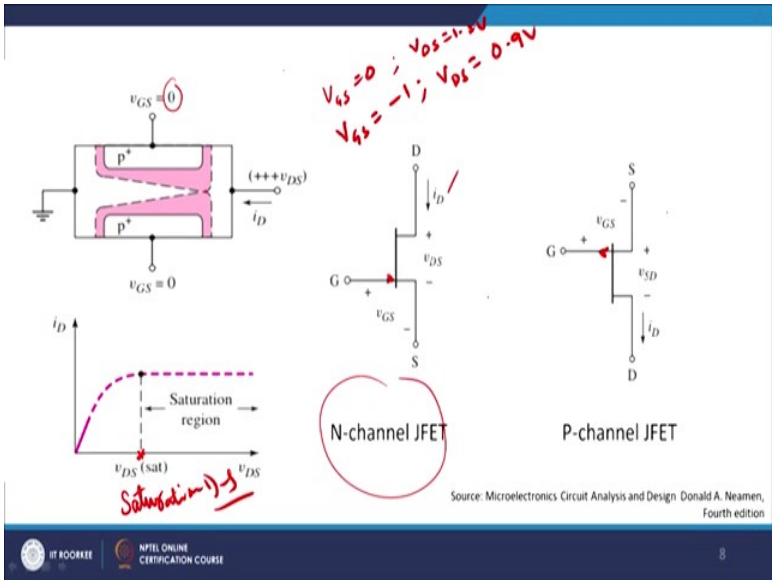


As I discussed with you therefore current versus voltage characteristics of a JFET if you want to look it looks iD versus VGS and it goes like this and as you can see, now you see as you make VGS more and more negative for the same amount of $V_{DS}$, the current starts to fall down, right and the reason being what? Reason being that now when your VGS is more negative, it is helping to formed a depletion layer more and more.

So, when VGS equals to 0, this was forming at say when VGS equals to 0 then it was the depletion region of the depletion region was touching each other as say $V_{DS}$ equals to 1.2 volts, clear. But, now what is happening is that let us suppose my VGS equals to minus 1 volt then my $V_{DS}$ at which the pinch-off will occur will be just 0.9 volts maybe. So, at a lower drain voltage I am able to achieve higher current or almost the same current, so that is what I wanted to tell you here, show you here.

In the saturation region as the gate to source voltage increases becomes more and more negative, the current starts to drop down or current starts to fall, right and we define a voltage pinch-off bad gate voltage at which the current goes to 0 is defined as my pinch-off voltage exactly the same definition which we saw for the MOSFET threshold voltage, right. And this is the equation for the drain current for case of a JFET, $I_{DSS}$ is the value of the current when VGS equals to 0.

So, this is your IDSS, right for VGS equals to 0 and 1 - $V_{GS}$ / $V_P$ where VP is the value which is you see, right. So, I have given you the discussion for n channel JFET, you please try to extend it to a P channel JFET as well, right and the answer remains the same as such occurring to you.

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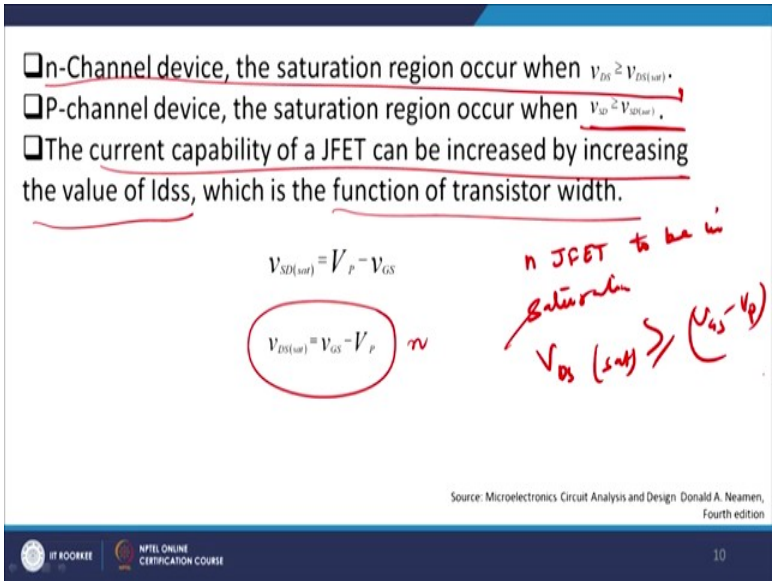


As I discussed with you in n channel JFET, therefore the saturation region occurs when $V_{DS}$ is greater $V_{DS}$ sat, exactly the same principle for a MOSFET, so I am going bit fast in this case because we are already deal with MOSFET in a detailed manner, conceptually, mathematically same as MOS device but cross section wise slightly difference in each operation value.

For, P channel this is what we sat that VSD is greater than VSD sat. Now, therefore the current capability of JFET can be increased by increasing the value of $I_{DSS}$ which is the function of transistor width. I hope you understand more is the width more number of electrons will be there and therefore even with VGS equals to 0 there will be substantially larger amount of current which will be there and as a result you will get a much larger profile in this case.

As i discussed with you for n channel therefore $V_{DS}$ sat should be equals to VGS - $V_P$ which means that for a device n JFET, right to be in saturation, to be in saturation $V_{DS}$ sat should be greater equal to $V_{GS}$ - $V_P$, please keep this in mind when $V_{GS}$ gate to source voltage and $V_P$ is the pinch-off voltage.

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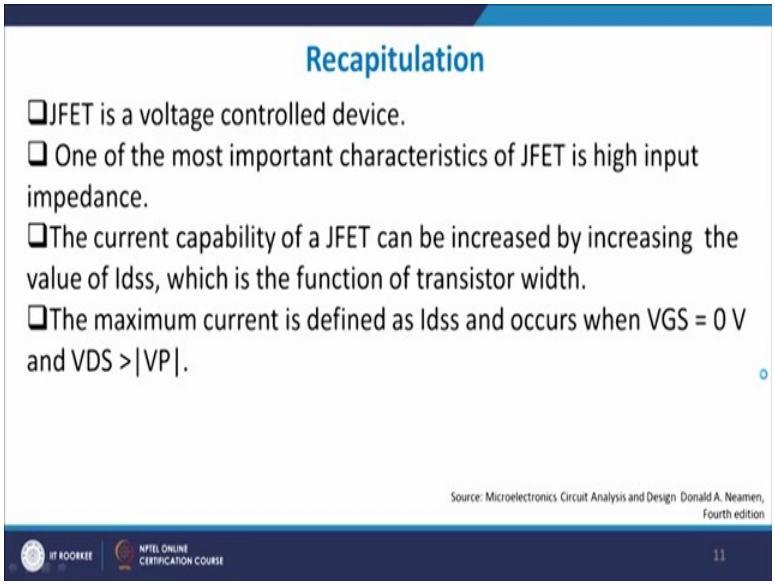


So, let me recapitulate to you, what we did in this small module of JFET because we will not be using too often because now JFETs are not too much used across the board. So, I should give you an idea about how it is working principle and how does it look like, right if time permits we will return back to this later on and explain to you some second applications but primarily it is voltage control device.

It is input impedance is relatively very high because on the gate side as I discussed with you, you have a depletion region working in the depletion region and therefore your forward biased characteristics are typically very low and reverse bias characteristics $i_D$ will be approximately equals to 0 and therefore impedance of a (dristrib) relatively very high. The current capability of JFET can be increased by increasing the value of W, right and typically the current flow is restricted by two important point VGS and $V_{DS}$.

So, for n channel JFET if you increase the value of VGS more negative I will get smaller current for the same amount of $V_{DS}$, right and so on and so forth. The maximum current is defined as I DSS on occurs when VGS equals to 0 and $V_{DS}$ greater than mode of V P which is primarily for n channel JFET, right. So, this gives you brief idea about my working principle for the JFET and basic structural parameter of JFET, right.

Two important parameters, I DSS, the maximum current flow through device in n channel JFET when VGS equals to 0 and VP the pinch-off voltage the value of (that drain to source) that gate to source voltage at which the current is exactly equals to 0, right and for the device

to be in saturation $V_{DS}$ sat should be greater than equals to VGS minus $V_P$, right. With this let me close the module here and thank you for your patient hearing, thank you.