Microelectronics: Devices to Circuits
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Lecture 31
Internal Cap Models and High Frequency Modeling-II

Hello everybody and welcome to the NPTEL online certification course on Microelectronics: Devices to Circuits. What we will be doing today is basically look into the high frequency modelling of the bipolar Junction transistor of the MOS devices. In our previous section, we have seen what are the various capacitive components which are there within the MOS device.

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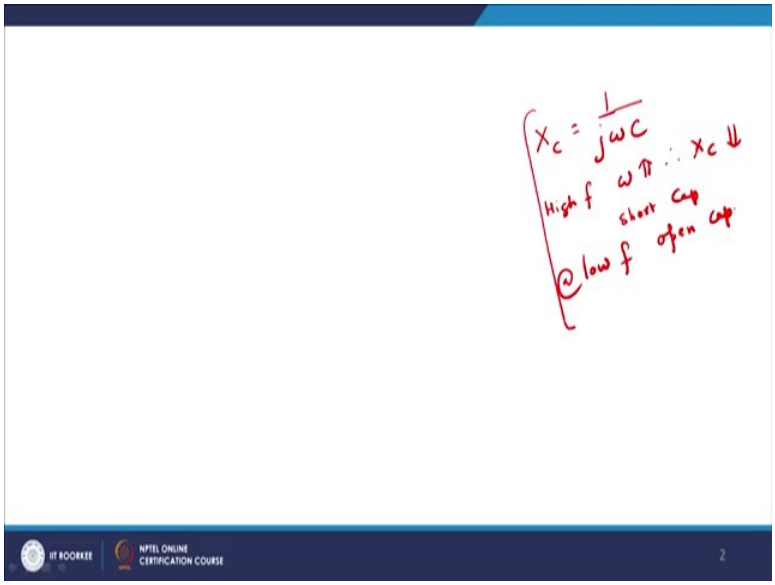

We also saw that, if you have a MOS device and if you have a capacitive model it can be predicted as a capacitance for example the overlap capacitance then it can be written as like this 1/jwc, so at high frequencies your ω, at high frequencies your ω is obviously very large which therefore your Xc are very, very low and therefore at high frequencies I can actually short all my capacitors, right short capacitors.

Where at low frequencies just as the name suggests, we will open circuit the capacitance, right. But this is only true for certain range of capacitances right, which of a certain range of frequencies. So, at very high frequencies you need to short it and certain open frequencies you need to close it. So, what we will be looking today is, that if I take a common source amplifier.

Let us, for example, MOS based common source amplifier and we have all those capacitances which is parasitic capacitances as well as bypass capacitances as well as blocking as capacitances then how does my amplifier behave is the main course of study at this module itself. So, let me come back to the come back to the slide itself and show you how it looks like overall our system looks like.

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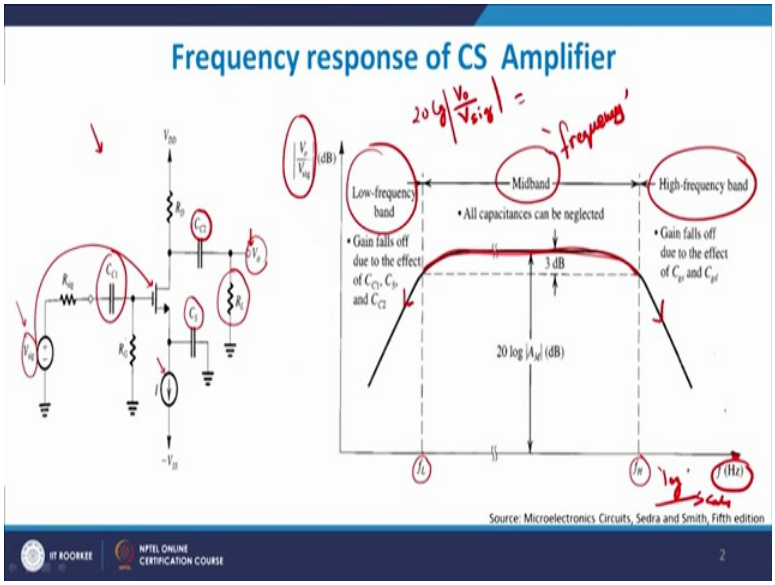

So, to your left if you look at this point is basically your C_s based, common source based design of a common source amplifier and I have attached current source on to the source end and there is a C_s which is the emitter sort of a or a source bypass capacitance, you also have a coupling capacitor in C_{C2} here which couples the drain output to the output of the (pins) drain of the MOS device to the output V_0 and you also have a C_{C1} which is basically the input coupling capacitances which connects your V signal input signal to the gate of my MOS device, right.

R_g is the gate (capacitance) resistance, R_d is the drain resistance and of course there will be also a R_s but since it is in series with the current source R_s will be negligibly small as compared to an output impedance of the current source and therefore that R_s is missing at this stage and R_L is the load resistance which you see here. Now, if you plot on the y axis V0 which is the output voltage divided by V_{sig}, V_{sig} is basically the signal input voltage and if you make it in dB. So, 20 log (V_{out} / V_{sig}) if you try to find out this will give you in dB, right and then you try to plot it with frequency on the x axis right and this is basically in log scale typically, this is in log scale, so you will have 1 Hertz, 10 Hertz, 100 Hertz, 10^3, 10^4, 10^5,

6, 7, 8 so on and so forth. So, this is, so you please understand your y axis will not be a linear scale it will be a basically a log scale right.

And your x axis will be a component, sort of a transfer function, which gives you output voltage by input voltage expressed in dB and mod of that basically. So, mod (V_0 / V_{sig}), in dB of that because at this stage we are not interested whether you have a phase difference or not, so we are just interested in looking to the magnitude a component available to you.

Now, if you look very carefully in this slide or in this overall approach, you will see that typically somewhere between f_L which you see here, we will discuss this later on and f_H your gain is almost constant see, so you are plotting gain v/s frequency and this gain is almost constant, right it is independent of frequency, it is independent of anything else, right this band is known as mid band, so mid band frequency right.

So, what is the mid band frequency? Mid band frequency is that frequency across which the output or the gain is independent of the frequency which you see, right. Now, beyond that particular point, beyond this f_H and beyond f_L as you go on increasing frequency or decreasing frequency your gain starts to fall down, right this is what is happening, right.

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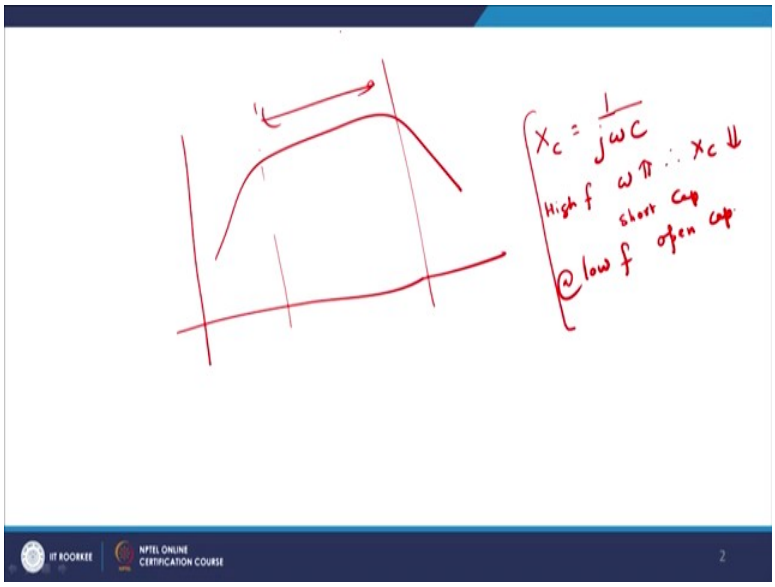

So, what we see therefore is, if you properly plot it is that you get a very steep profile here, you get a very steep profile here but somewhere in the middle you will have automatically a gain which is almost independent of frequency this is known as mid band, as I discussed with you this is mid band.

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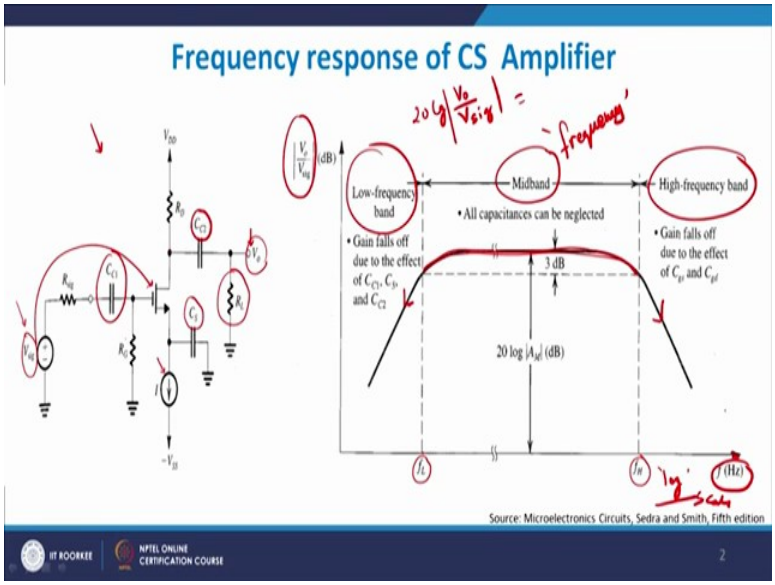

This is low frequency band and this is high frequency band right and a time might come that is it is large frequency or gain will be absolutely equals to 0. So, let us see why this happens or why you actually see a drop in the gain at very low frequencies and at very high frequencies?

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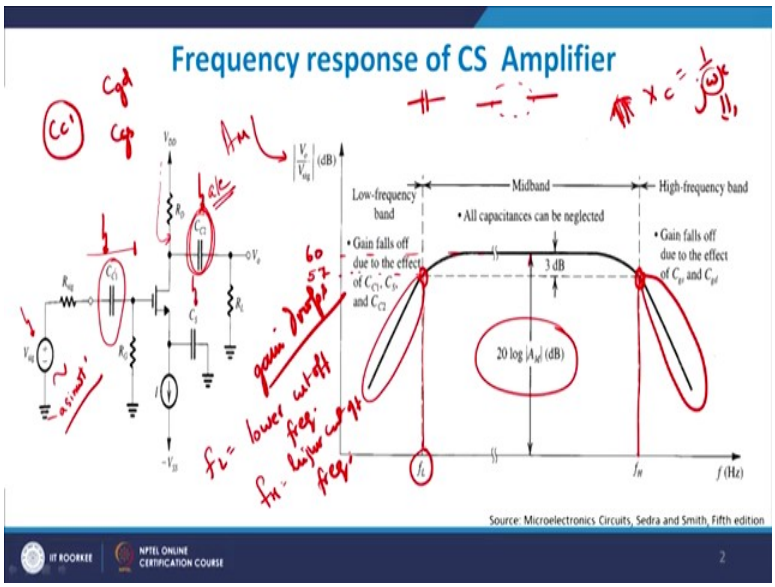

If you remember, if you look very closely and if you remember your previous discussions you will appreciate that you will always have a coupling capacitor here and a coupling capacitor here and you have a C_s which is basically a source capacitance. Now, why these capacitances were used? Initially they were used primarily so that for example, why C_{C1} was

used? C_{C1} was used primarily, so that any DC component of this V_{sig}, so V_{sig} is basically an AC signal.

So, it is basically a sin(wt) but since it is derived from a DCs you do have a source available within itself, there will be a DC component always associated with V sig, right. You do not want that DC component to sit on the gate side of this MOS device otherwise it will change the bias point and that is the reason you put a C_{c1} here, (a coupler) a coupling capacitor, in fact known as a blocking capacitor and as a result you only allow out the AC signals to go through and you block the DC.

Similarly, if you look at C_{C2}, this also allows only the AC signals to go through and block the DC right, say only allow AC signals to flow through and block DC, which DC? DC capping for example from V_{DD}, right coming from V_{DD} this will be blocked by C_{C2}, so that is the reason but then let us see what happens therefore at low frequencies. Now, at low frequencies as I discussed with you X_c was equals to 1/jwc, which primarily means that at low values of w, X_c will be typically large right.

So, as well as this, right, its effective value is typically very large, the resistance offered by this is very large and therefore as you lower you start to lower your frequencies this start would behave more like an open circuit rather than short circuiting and therefore gain starts to fall down, the gain so your gain drops right, your gain drops why does your gain drops? The gain drops because of a simple reason that as you lower your frequency the 1/jwc goes on increasing X_c goes on increasing and then the assumption that you are shorting it now you have to open it to a larger section.

And as you make it open obviously you can understand there will be no signal flowing and therefore your output will be equals to be 0. That is primarily the reason why the gain falls at the low frequency band, right. Let us see, let us look at the fact what happens at the high frequency band which is somewhere here more than f_H, right. If you look at more than f_H part then remember there were two components parasitic component known as C_{gd} and C_{gs}, C_{gd} and C_{gs} gate to source and gate to drain capacitances, right.

Now, at such high frequencies at this, what we were assuming? Was that these capacitances will not playing a role because overlap is small or they are minuscule, they are very small in dimensions but at such high frequencies of operation right the resistance offered by C_{gd} and

C_{gs} though is relatively small but the gate to drain capacitors which is available to me has a extra effect on to the circuitry and gain starts to fall down.

Which means that at such a high frequency though Xc is low for Cgd and Cgs right, which means that your gate and drain are not coupling properly in a sense and therefore gain starts to drop. So, gate starts to lose control over the channel, you know in a sense and as a result the gain starts to fall. So, the high frequency the gain reduction in is primarily by virtue of reduction in C_{gd} and C_{gs}, right and your gain losing control over the channel and the source and drain side.

And on the low frequency part if you look very carefully it is primarily because of the CC1, C_{C2} getting effectively shorted, so sorry effectively open and then when they open the gain starts to fall down, right. So, this is the two reasons why primarily you will see this so most of the characteristics of the amplifier circuits will look like this, this is 20 log A_m, A_m is nothing but this is A_m, this is A_m, right 20 log (V_0 / V_{sig}) in dB is defined as this point, right. Now, let me come to two important cross points in this characteristics and these cross points are this one and this one, right.

So, what you try to do is you just look at the top, suppose this is equals to say your 60 dB then what you do is? You try to go from here to 57 dB, so draw a wire which is 57 dB. So, 3 dB drop is there and then check out two points where you get the 3 dB drop then we drop the point across the frequency axis and we define fL as the lower cut-off frequency and f_H to be equals to higher cut-off frequency, right. So, I have a lower cut-off frequency and I also have a higher cut-off frequency, the lower cut-off frequency is the point where the gain has dropped by 3 dB and higher cut-off is also again point where it is of 3 dB.

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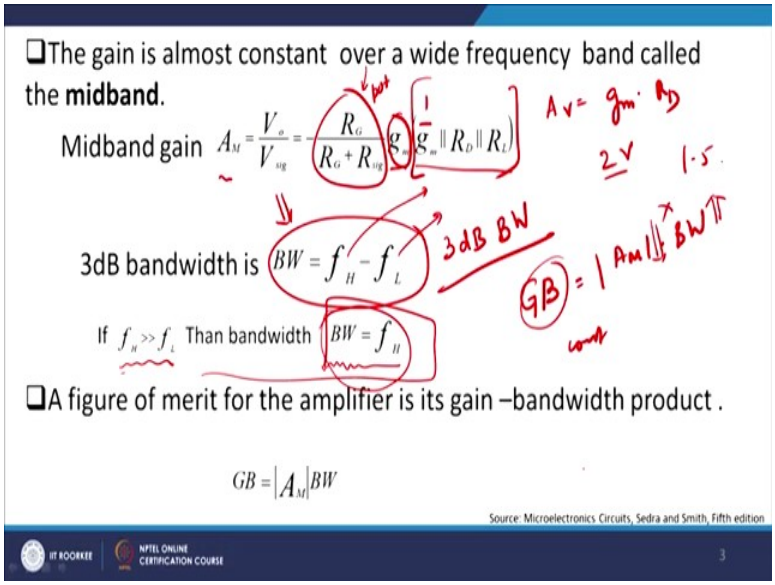

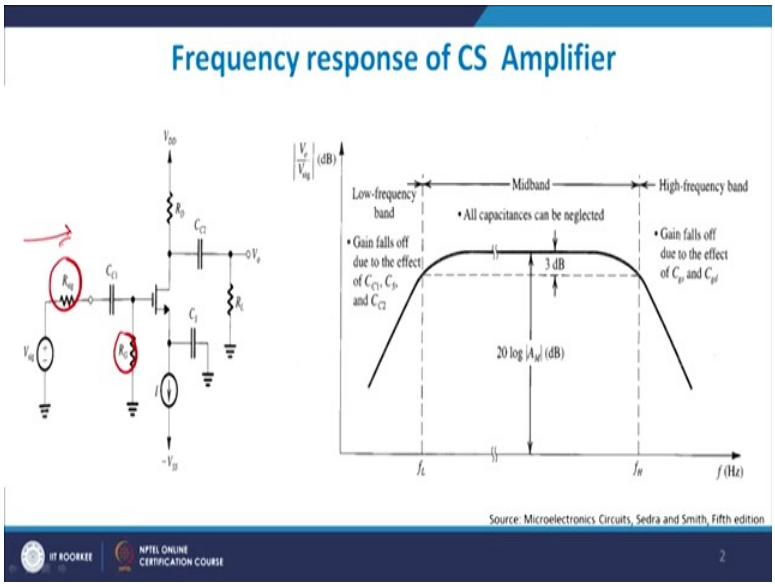

Now, the therefore the distance between the two in frequency domain is defined as my bandwidth, right also referred to as a 3 dB bandwidth. So, bandwidth is defined as difference between higher cut-off to lower cut-off, right and this is known as bandwidth. If f_H is obviously much larger than f_L, so f_H is 10 to the power 7, 10 to the power 8 and I feel may be how the hardly on order of 10.

So, if we subtract the 2 it is approximately goes to f_H. so, whatever we do the value of f_H that will be the bandwidth of the input signal, right. Now, if you look at the mid frequency gain right, mid frequency gain which is basically your Am then it is V_0 / V_{sig} and V_0 / V_{sig} how did I find out or how did I come to know was that if you look at, so if you go back to your previous slide, sorry.

Let me just drop this point for clarity sake, right and let us look from this point of view, right. if we look this point V_{sig} actually is the V_{sig} is the voltage given by the signal but some portion of that goes R_{sig}, C_{C1} and so on and so forth. The remaining falls across R_G and that is the gate voltage given to this MOS device, right. So, if you look at, sorry so if you look at the next slide here you see R_G / R_G + R_{sig} is the division which you do because it is a basically a voltage divider network.

So it is RG, so this is R_G / R_G + R_{sig} is the is the voltage divider network which you see, this one, right multiplied by because this is the voltage divider network multiplied by G_M x G_M parallel R_{Dx} R_L, right to why? So, it is it should be actually 1 / G_M R_D R_L, right. So, it is basically G_M transconductance, so if you remember gain from G_M times R_D remember, so this is GM and this is your effective R_D which you see but this factor comes from the fact that not all the signal voltage appears across the gate side.

A part of it appears because of the potential divider technique because of potential divider technique, so if you are giving V 6 a is equals to 2 volts not all the two volt will appear at the gate side may be 1.5 peak to peak will appear though, what is the reason for that? The reason for that is that you do not want large signal distortion to play into picture.

So, if your input is very, very large peak to peak then you might end up having a nonlinear distortion in your system, right and as a result what will happen is that it output will be heavily distorted that is compared to your (())(13:59) and as a result you will never get a linear profile which is there with you. So, I discussed with you just now that a bandwidth is defined as f_H minus f_L, since f_H is many orders larger than f_L we define that bandwidth can also be written as f_H just the value of f_H itself.

A very important figure of merit which we typically use an amplifier design is defined as the gain bandwidth product, we also refer to as gain bandwidth GB and it is referred to as $A_{m\,x}$ bandwidth and this is generally constant. So, what you do is? That if you want to therefore make your bandwidth high, you have to reduce your gain, so that the product of these two remains constant, right.

And that is the problem for any amplifier that if I want my gain to be high my bandwidth will be restricted and if I want my bandwidth to be high my gain will be restricted, you cannot take both of them together and make both of them high, right, and that is the sort of a price you pay for designing this basic cons, this problem area, right.

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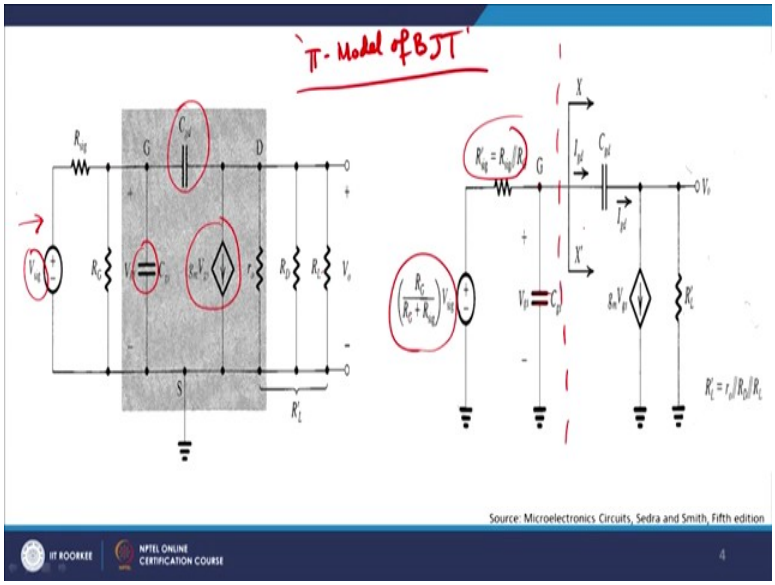

With this knowledge let me do a mathematical treatment for high signal frequency and low frequency response. So, if you look here (click) clearly for the high frequency component if you remember in the previous, I have just replaced the MOS device with it is equivalent circuit model pi. So, this is basically a pi model of BJT is used right, of BJT is used and if you look carefully it is C gd here and here what C_{gs} here, we have got current source $g_m * V_{gs}$ and r_0, R_D, R_L, right.

So, if you look from this side from the left hand side which is the input side then a part of basic appears on the gate side given by this formula, so V_{sig} x (R_G / R_G + Rsig) is that effective value then what we do Rsig' equals to Rsig because these two will be in parallel, so R_{sig}' will be equal to R_{sig} || R_G and then the same voltage is fell into the gate side which is internally having a C_{gs} gate to source voltage which is available with us and this is the input side so, fine.

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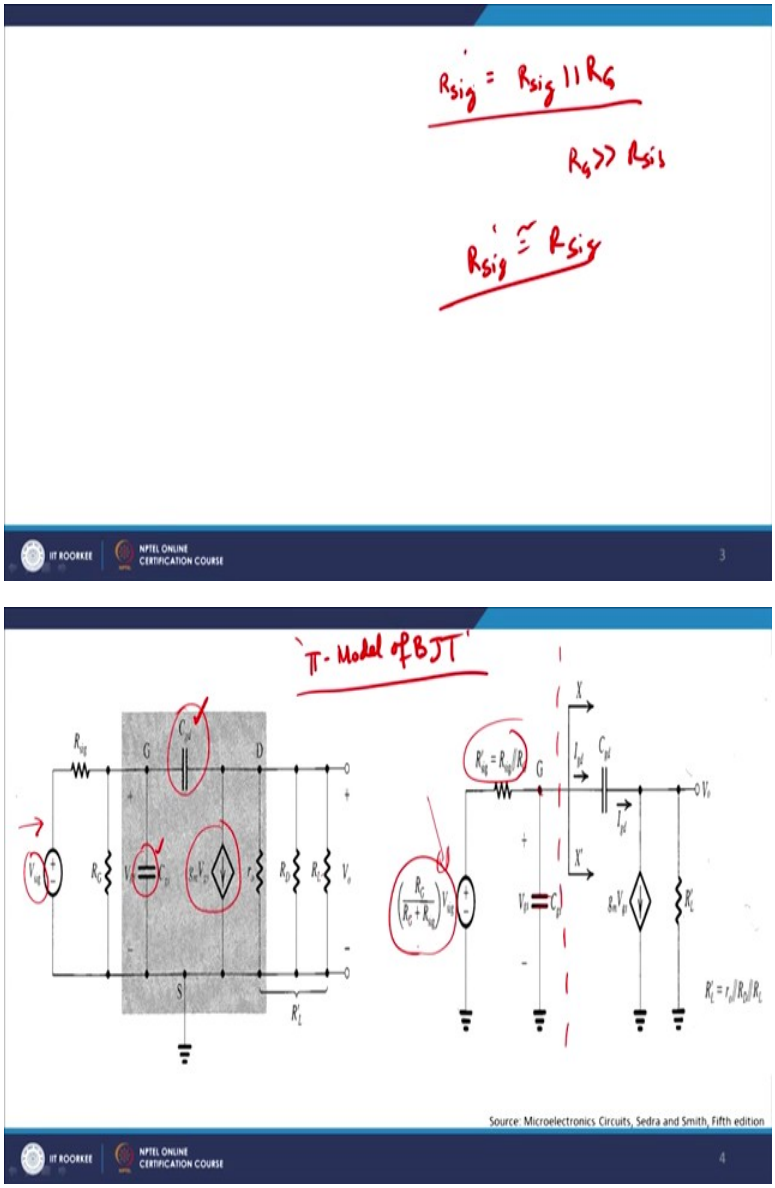

And therefore, what people have found out over the years is that R_{sig}', right R_{sig}' will be approximately equal to Rsig || R_G but since R_G is much larger as compared to R_{sig}, what we safely can write down is R_{sig}' is approximately equal to R_{sig} which means that if you go back to a previous, this slide then R_{sig}' which is the potential or the resistance offer to the gate side is exactly almost of the offered by this structure right and that is what we get from here in this case, right, ok so, this is what we get.

So, if you look at the pi model therefore from therefore looking from this side you what you can do it is quite an interesting summation that, so when you are doing a high frequency modelling or we needing a sorry, a low frequency modelling C_{gd} will come into picture C_{gs}

will come into picture and therefore they will change the output characteristics of the device, right.

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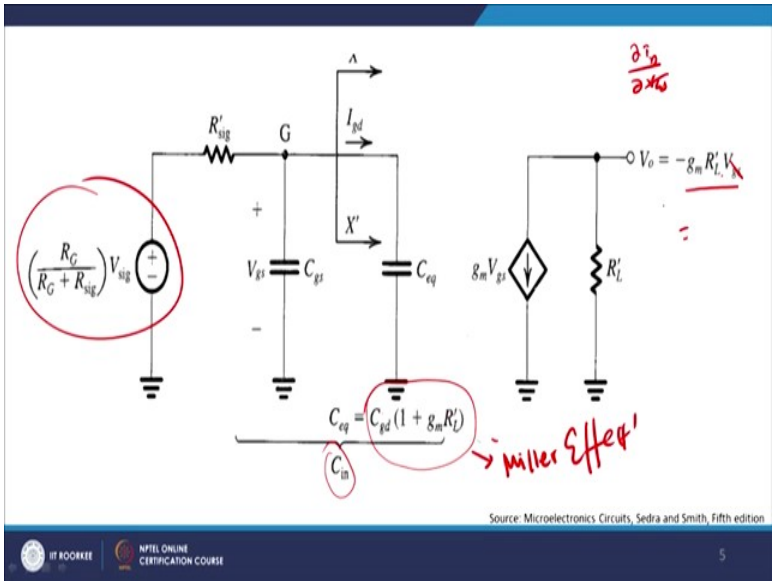

Now, if you look very carefully then what happens is this is, the input voltage which you see in the output side quite interestingly I get C_{gd} * (1 + g_m*R_L'), right. I am a deriving it in the class but C_{gd} or C equivalent or input capacitance will be C_{gd} * (1 + gm*R_L), which means that initially the device would be looking only at C_{gd} but because of a coupling between gate and drain, right, you have a multiplication term 1 + g $_m$ * R_L', this phenomena is known as Miller effect, this is known as Miller effect, right.

And therefore, I get the overall voltage will be g_m*R_D, so g_m* R_D is nothing but gm times R_L*V_{gs}, why? Because g_m is del (I_D) / del (V_{gs}), so this V_{gs} cancels with this V_{gs}, I_D * R_L will give you the output voltage V0, right and from here you can get the value output voltage in a much easier manner, right. If we are now therefore come to the low frequency domain, low frequency domain of this device maybe we can explain to you, so, right.

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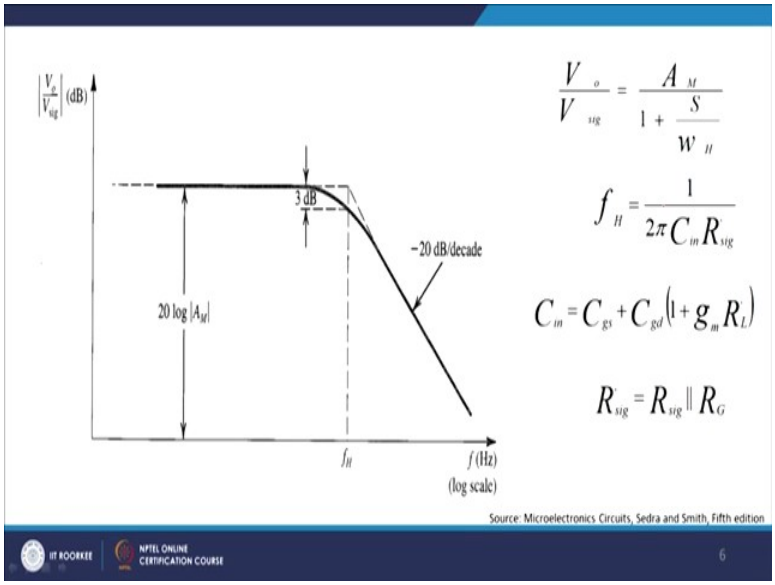

So, let me come to the, sorry, so if you see very closely or if you have a look at the and we also do a low signal, low slow frequency modelling.

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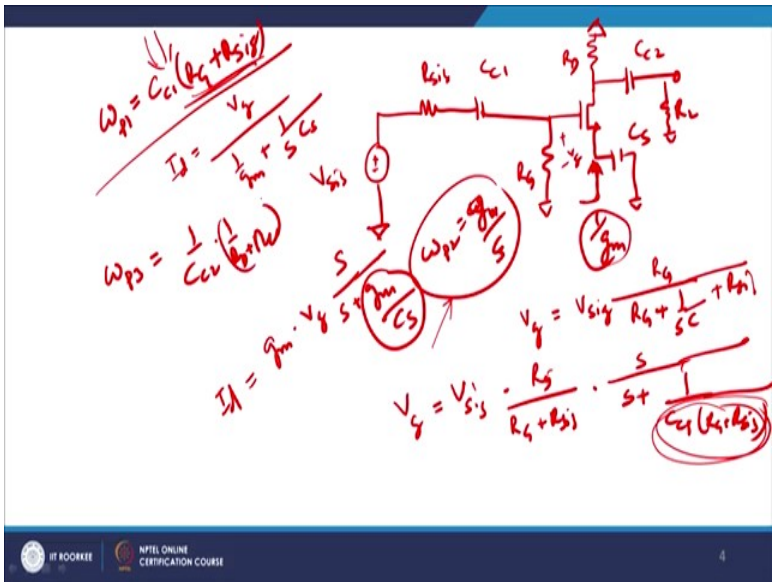

Then in the low frequency, as I discussed with you, right. All the capacitances will remain because they will not be closed as such and therefore I can write down something like this as the overall gate to source variation, right. So, this is R_D, R_G C_{C1}, R_{sig} and this is V_{sig}, this is grounded, and then this is also grounded because DC biases are missing and you have C_{C2}, right and then you have got R_D or R_L as part of it the C_s, right and this is your plus minus V_g which you get.

So, looking from the source side the impedance offered is 1 / gm, right so keep this is in mind a standard methodology. So, I can write down Vg to be equals to V_{sig} * R_G / (R_G + 1/sc + R_{sig}), right and therefore, you can safely we write down Vg to be equals to V_{sig} * (R_G / R_G + R_{sig}) * (S / (S + 1 / C_{C1} (R_G + R_{sig}))) where this value is referred to as w_{P1} or the first point cross point frequency, first cost point frequency is C_{C1}(R_G + R_{sig}). Which means, the first cross point frequency or the frequency beyond which you will see a drop in the gain is governed by the C_{c1}, the coupling capacitor attached here as well as the resistance offered by the RG and Rsig value. Now, therefore I_d, I_d as I discussed with you is V_g* g_m will be V_g / (1 / g_m + 1 / SC_s), fine why? Because looking from this side if you look very carefully 1 / g_m is the source impedance as well as 1 / SC_s is the impedance offered by this capacitance.

So, since they are in sort of a parallel connection therefore what you do is? That you add them up and therefore Vg upon that will give you the value of drain current, right. So, if you solve it and if you want to get the picture I get g_m * V_g (S / S + g_m / C_S), this is your Id, right and therefore I get a second crossover point w_{P2} as gm/s, so have a first crossover point given by this and a second across over point given by this, right.

You also get a I am not deriving in the class but you also get a third crossover point which is given as w_{P3} is (1 / C_{C2} * 1 / R_D + R_L) which means that each of the capacitor C_{C1}, C_{C2} as well as C_S, right starts to give you extra dip in the in the output characteristics. So, as you lower your frequency domain is they start to fall drastically. So, if you plot it is frequency.

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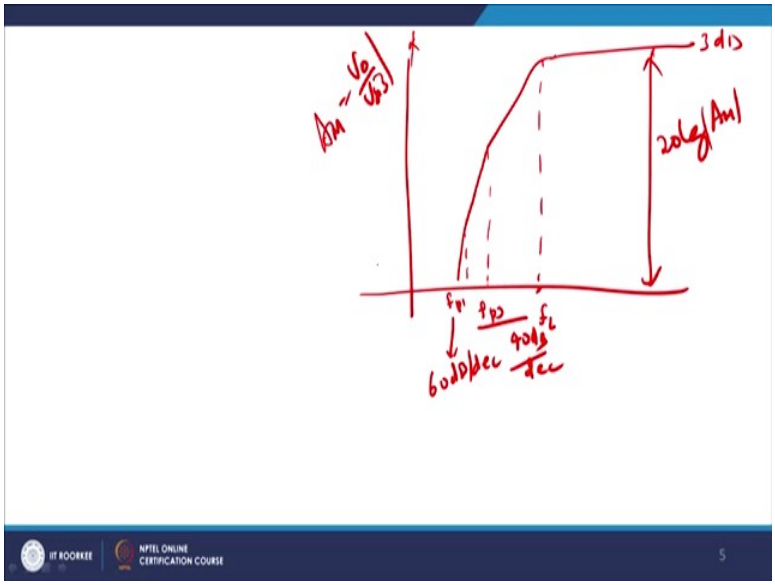

If you plot its frequency versus gain graph then you get something like over 3 dB bandwidth obviously available with you, this shows our drop here and then this shows a drop here and then this shows a drop here. So, if you look very carefully this, is your f_H, right this is your f_L, f_H and this is your f_{P3} and this is your f_{P1}, this gives you approximately 60 dB per decade drop, this gives you 40 dB per decade drop, right and then f_L is there which is the low frequency gain which you see, right. This is nothing but 20 log of A_m, right where A_m is the gain which you see, A_m is therefore equals to V_0 by V_{sig} for a fixed value of this value, right.

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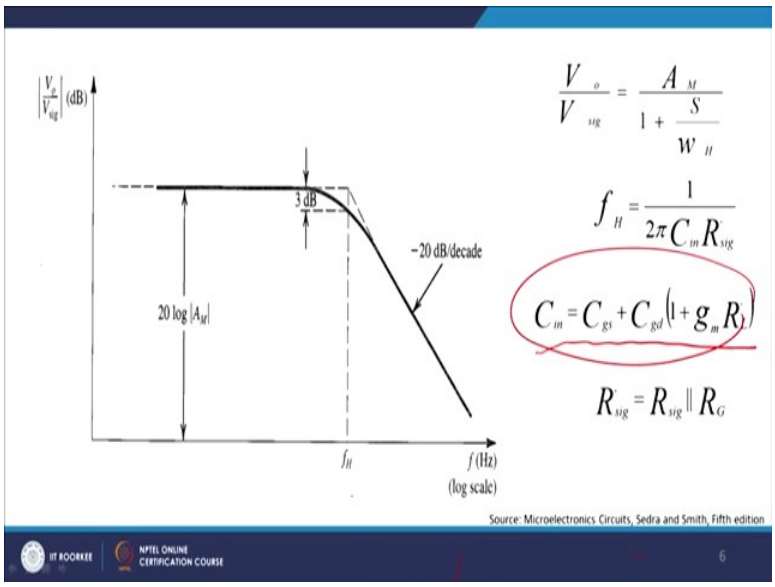

So, this is what you get from the gain and therefore if you look carefully then we get what you get is basically $C_{in} = C_{gs} + C_{gd} *(1 + g_m * R_L)$, right. So, let me do the, this is this for the

low frequency design and therefore let me do for a high frequency design to make that to make it much more better understood in the sense that we can make it high frequency design.

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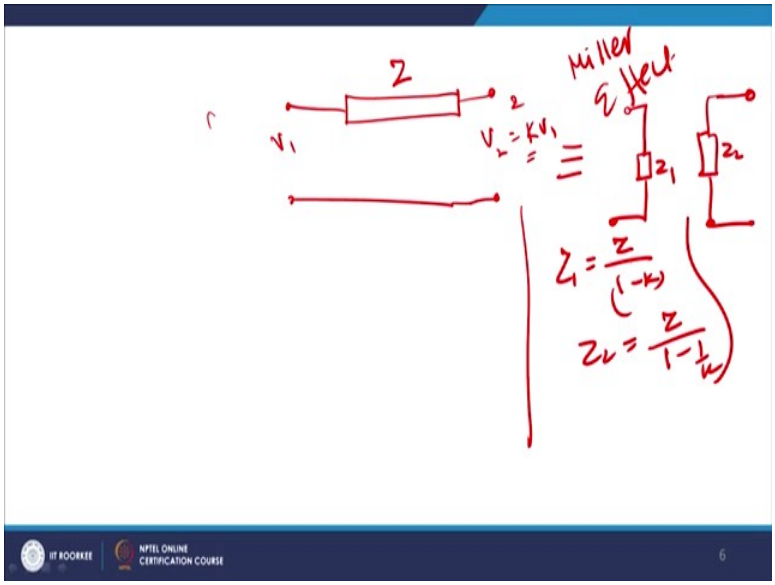

Within the high frequency design, we also try to find out or try to see, what is known as a Miller multiplication, so I have got two ports here 1 and 2, 1 and 2, let us suppose input voltage is V_2, V_1 and output voltage is K * V_1 which means that the input and output are variated through a costing multiplication factor K.

Then this and this is Z is the impedance then this is equivalent to saying as this Z 1, right and then this is Z 2, right and Z 1 is referred to as Z / 1 - K and Z 2 is referred to as Z /(1 - 1 / K), right I am not deriving it in the class, in this lecture but this is how it looks like and it and this is known as Miller effect. So, Miller effect tries to enhance the overall gain by making coupling between gate and drain in a much prettier fashion or easy fashion right and that is what we get from the Miller capacitance as such.

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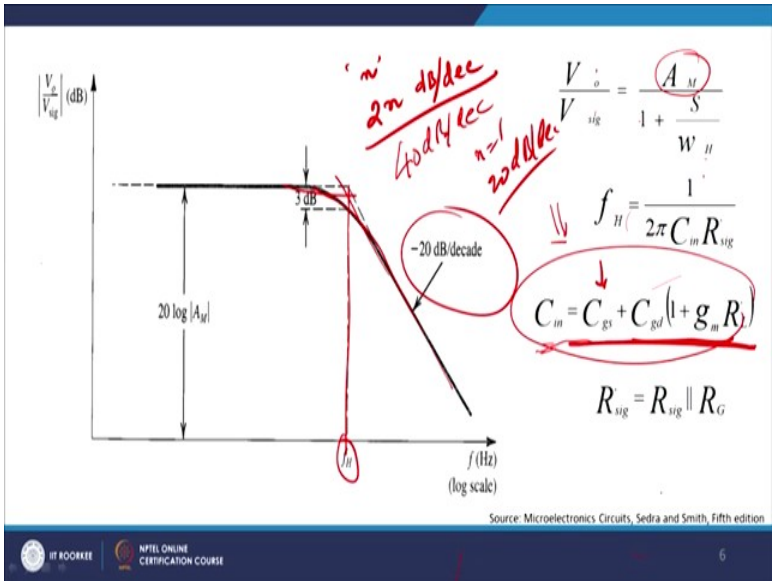

So, with this what we have done therefore is, that we have actually seen therefore that as I discussed with you for every one pole added to the right you get, so for an nth order filter for example this is known as the decade or the role off rate is always given as 2 to the 2n dB per decade. Which means that, if a second order system is there right then it will be 40 dB per decade because n is equal to 2, if n equals to 1 then a single order will be have 20 dB per decade, fine and you can see therefore that this is the this is how it forms.

So, you backtrack this one, the back side in your backtrack this one, the cut is basically your half your f H which is basically your high band design. As I discussed with you earlier therefore V0 / Vsig will be given as A_m / 1 + S / w_H and w_H is given by this formula f_H equals to 1 / 2*pi*C_{in}, C_{in} * R_{sig}, R_{sig} is the approach value of voltage but C_{in} is written C_{gd} + C_{gd} * 1 + g_m * R_L.

So, as you can see that adding an extra potential or a capacitance in the feedback loop in sort of it an inner loop and assuming that C gs will always come into picture irrespective of any other thing we see that my input capacitance can be raised from a value C_{gs} to C_{gd}, C_{gs} plus this whole quantity. And that is quite an interesting and impressive one that by doing so, you will be able to raise the overall gain of the system, right.

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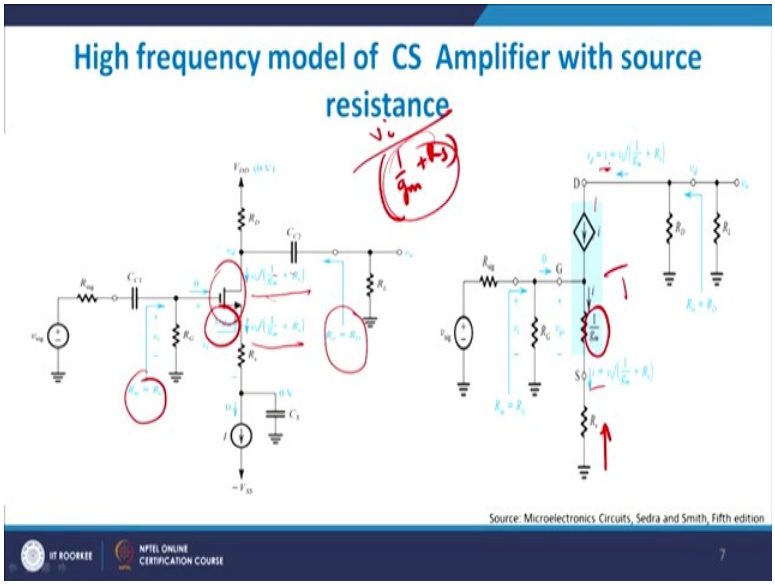

Let me come to the high frequency model of the CS, so that was the low frequency model and let me come to the high frequency model as I discussed with you. If you look very carefully, this is again the same thing $R_n = R_g$ and from looking from this side it is only g_m, right it is only $g_m + R_S$. So, the resistance offered at the source end is $1 / (g_m + R_S)$ right and then if you divide V_i input voltage by this quantity is basically the current which is flowing through this resistor R right and that is what is the current is.

Now, since the current has to be the same, I see that V_I * this quantity and this quantity will also be remaining the same. So, on the right hand side R_0 will be equals to R_d which is basically the input impedance which you see from here. Now, if you replace this MOS device by it is corresponding T model then we say that I will be equals to $V_I / (1 / g_m + R_S)$, $(1 / g_m$ + total current flowing).

Since of the gate side, from the gate side you do not have any exiting an entry of current almost the same current will flow through the resistor and the evidence is that there will be 1/ gm drop there and therefore looking from the source end it is $V_I / 1 +(g_m + R_S)$, right. So, looking for the source side current and both the currents are equal and therefore, there is no problem and as far as I understand in the configuration is concerned. So, we are finished with high frequency model and we have seen how frequency model works. Let me therefore recapitulate the whole discussion on that on this topic.

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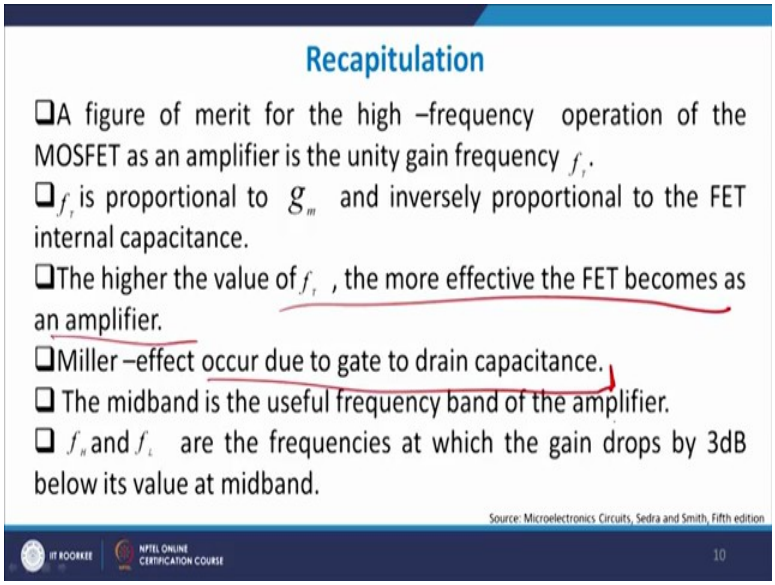

Well with the figure of merit for high frequency operation of MOSFET is an amplifier is the unity gain frequency, how did you define unit gain frequency? Where a gain falls to 1, we define that to be as the unity gain frequency. f_T or the transit frequency is or is the proportional to g_m and inversely proportional to FET internal capacitances, which means that higher the value of g m more will be the bandwidth and more will be the your f_T but if it in general capacitance is also higher than your reduction will be there in your f_T as well as g_m.

The higher value of f_T, the more effective the FET becomes as an amplifier, right. So, one thing which we learn is that your g_m should be high and your f_T should also be high, once you ensure these two to be very high then automatically everything falls into place in a detailed manner. Miller effect occurs due to gate to drain capacitances right and this is quite an interesting problem which people face that the Miller effect which will do may be in the next turn and you show it to how you Miller effect works out.

But Miller effect does what primarily is that it adds to the overall capacitance of a system and that addition is also not linear it is effective addition. So, some there is some constant, you multiply that with C_{gd} to get the new value of C_{gd}, so gate to drain coupling capacitors is there. Now, Miller effect therefore works due to gate to drain capacitances that is what we have just now understood.

The most useful sub band of amplifier is basically your mid gap band, why? Because the gain is almost constant and independent of the frequency and therefore, I can safely say if you are operating your amplifier within that range my output will be almost constant depending only

in the value of V_0, right. Then you have two important frequencies, we have seen f_H which is also referred to as low cut-off frequency, high cut-off frequency and f_L which is basically refer to as a low cut-off frequency.

They are typically 3 dB points below the maximum gain position and beyond these points the gain starts to fall down with increasing or decreasing frequencies, right. So, the most reliable one is basically your the mid band frequency. Last thing is, that there is a figure of merit which is basically known as gain into bandwidth, which is also known as gain bandwidth product that should be always constant for a system.

So, if you are increasing the gain pay the price of a lower bandwidth if you are increasing the bandwidth you pay the price of a lower gain, right. So, we with this we have almost learnt most part of the amplifier design and look into the very critical aspect of amplifier design, next time we will take up another issue as far as this course is concerned, all right thank you very much for your patience hearing.