Microelectronics: Devices to Circuits
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Lecture 30
Internal Cap Models and High Frequency Modeling-I

Hello everybody and welcome to the in NPTEL online course on Microelectronics: Devices to Circuits. We start with the new module today, which is basically on internal capacitance modules and high frequency modelling, right. So, what we have done till now? We have looked into various amplifier configurations using MOS device and we saw that various configurations have their own advantages and disadvantages in terms of working principle and in terms of output parameters being extracted.

However please understand, that these signals, the input signals were restricted to very small signal to maintain linearity and we were also assuming that the MOS devices actually biased in the saturation region of operation, it is neither in the cut-off nor in the triode region or nor at the edge of these regions right, so they are somewhere in the middle of the saturation region.

While this is good for working principles but generally the MOS device for example has to work at relatively high frequencies of operation because finally you will have to assimilate these MOS amplifiers in an analog scenario or in a mixed signal scenario where your frequencies of operation may be of the few MHz to few GHz.

Under such a scenario, your device should work properly at such high frequencies and that is the motivation behind this lecture, that this lecture will give you an idea about what are the device problems at very high frequencies of operation, input frequency and to understand the appreciate that we need to therefore understand the various capacitances associated with the device which become prevalent at very, very high frequencies. We will show you, I will give a reason why frequency is an important concept in a capacitance or inductance.

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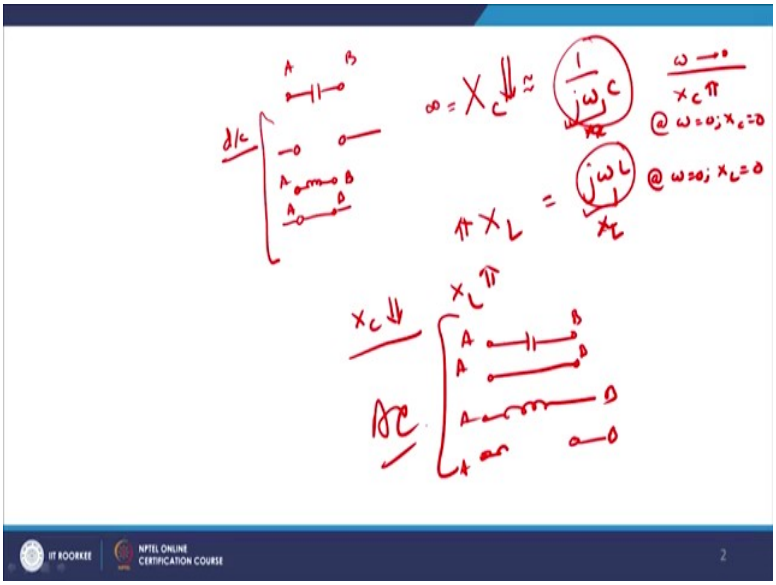

All of you must be aware of the fact that if you want to find out the capacitive reactance it comes out to be equals to 1 by jwC whereas for inductance it is equals to jwL, right this jw is referred to as X_C and this is referred to as X_L right, sorry yes I am sorry this is not jw, this is referred to as X_C and this is referred to as X_L. Now if you look very carefully in case of capacitances if w tends to 0 my X_C becomes very large and therefore I can therefore say that whenever you are doing a DC analysis right whenever you are doing a DC analysis, you can just keep your capacitances you need to.

So, if you are doing DC analysis this is point A and point B and you are doing a DC analysis then the equivalent circuit will have something like this, this will be acting as an open circuit why because at w equals to 0, X_C equals to infinity, right. So, at w equals to 0, X_C equals to infinity. Similarly, at w equals to 0, X_L is equals to 0, so what you do is? When you do a DC manipulation or DC analysis you keep your capacitances open but you if you have an inductor between point A and point B right, if you have an inductor right what you do is that you then short it, right when you do a DC analysis.

But (little) so, but let us look what happens in AC analysis. So, when the frequency increases X_L also increases but X_C starts to drop down, so at relatively large values of frequencies where w is relatively large X_C can be actually reduced to very, very small quantities and X_L can be reduced to very high quantities, so X_L will be relatively very large. So, if I want to find out therefore the cap modelling at high w or a high frequencies this then will be shortened right and what happens to my inductor? Inductor is let us suppose A, B then under AC bias I can I can make assume it to be an open circuitry, so this is under AC.

So, that is the reason that when you go for high frequencies, the points in the circuit which would initially made it made to be opened, now starts to become closed right and therefore access current or movement of current changes and therefore it is totally a different ball game altogether. So, we will be looking into this aspect as we move ahead and to understand therefore the first part of the lecture is that, we will be understanding the internal capacitance model. So, as you can see here the topic is internal capacitance models and it is high frequency modelling, right. So, let us see what the first, what are the outlines of the talk?

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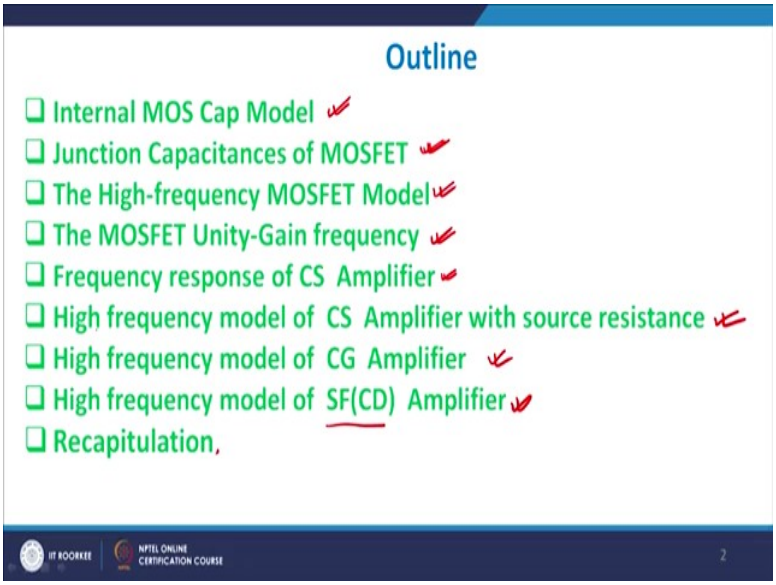

We, will first talk about internal MOS capacitance model, we will look at the junction capacitance of model of the MOSFET, right. We will look at the high frequency modelling of MOSFET, after we understood high frequency we will be coming into MOSFET unity gain amplifier or a unity gain frequency, what is the meaning of unity gain frequency? Then, frequency response of CS, we have already studied CS in our previous interactions, where CS with source resistance, CG and then SD also known as source follower right and then we will recapitulate.

So, we will do high frequency modelling for all the amplifier design which you have already (let) left. And to do that, certain important characteristics of amplifier should be clear to you as we move forward. Let us look at the internal MOS capacitance model, right.

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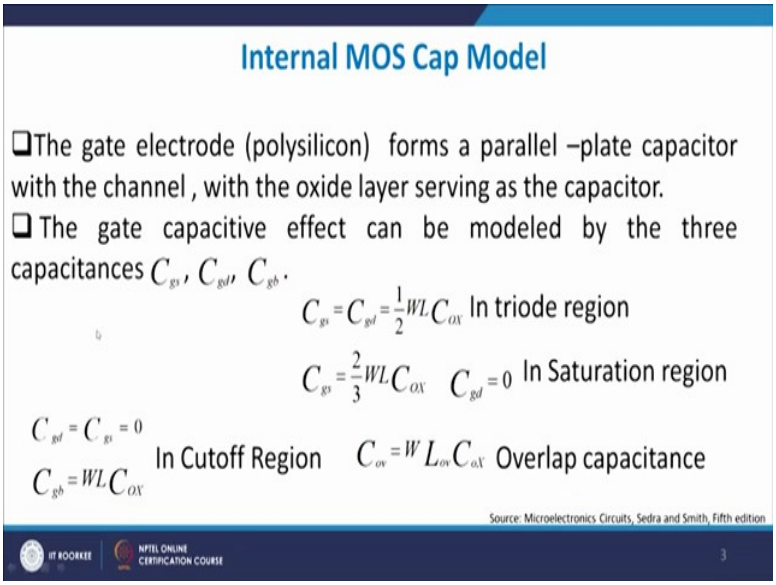

As you can see primarily, if you look at the MOS device, right.

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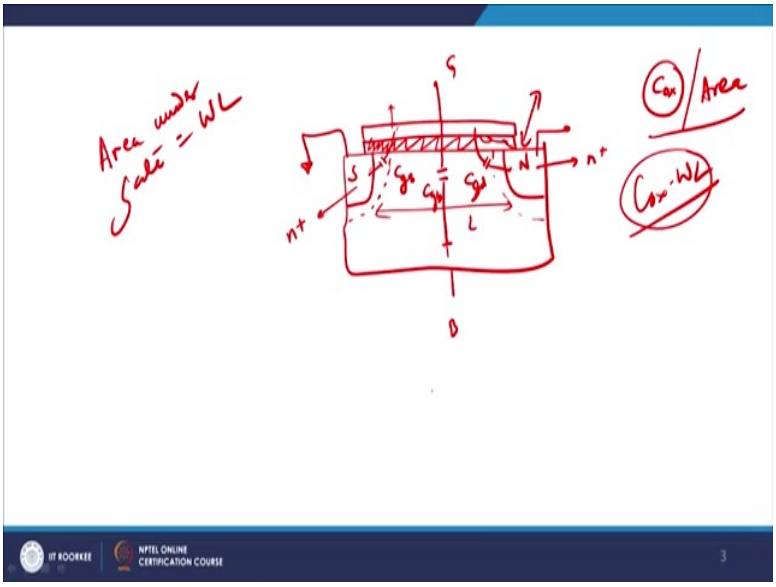

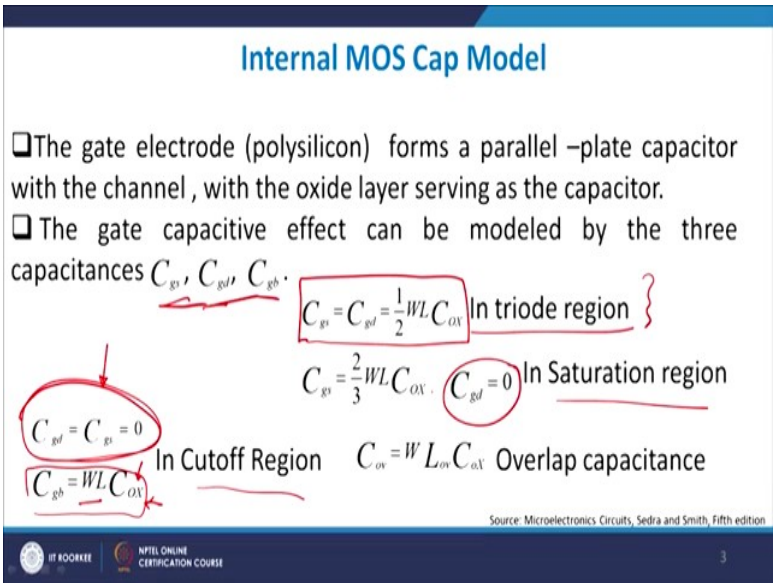

It is basically and it is divided into majorly into three or four important capacitance models. So, let us suppose this is my source and drain right and I have an overlap here, right I have a diffusion capacitance here and I also have a metal capacitance, so this is my gate and then I have my bulk, let us suppose bulk so forget the timing, i have bulk. So, I will have a depletion region here, I will have a depletion region here this I give it positive bias, this I am grounding it for all practical purposes.

This is a typical structure of a MOS device, right this is the typical structure of a MOS device. Now, if you look very carefully there will be always a gate to source capacitance, gate to source and this is C_{gs}, there will be also source to drain capacitance C_{gd}, right. So, this is C_g sorry, so this is C_{gs}, C_{gd} and you also have $C g_b$ why C_{gb}? Gate to bulk, so you have an gate to bulk, no capacitor C_{gb}.

What is the origin of these capacitances see? Gate to sources primarily because what is the basic definition of capacitance that if you have got two charges separated by a distance we refer to that as a capacitance. So, if you look at this figure here, the gate is always heavily charged because it is a metal gate and this is highly doped, so N^+ region. Similarly, this is also N^+ region, so two N^+ regions separated by a dielectric here is primarily a capacitance, right.

So, I have as C_{gs} here and I have a C_{gd} here, I have C_{gb} here. So, there are three capacitances which is available to us, let us see how it works out when you are in the triode region, in the saturation region and in the cut-off region, right. Cut-off is the most easiest one so we can we can deal with it much earlier or much faster, please assume or please understand that you also

have a C_{ox} or the oxide capacitance per unit area, what does it mean? It primarily is basically the area under the so what is the area under the? Because if this is your length, if this is your length of the channel then W is in the inside the inside the board.

So, the area under the gate is actually goes to W into L, if C_{ox} is the oxide capacitance per unit area then the total capacitance will be equal to C_{ox} into W into L, fine. So, this is what I was explaining C_{ox} therefore is the oxide capacitance per unit area right and that is what we were trying to see. If let us look at what happens in the triode, saturation and cut-off region.

In the cut-off region your C_{gd} and C_{gs} are both equals to zero, right and the reason is very simple cut-off means you do not have any inversion charge, right when there are no inversion charges available your gate voltages are relatively very, very low and therefore gate to source and gate to drain almost equals to zero, almost equals to zero they are not exactly goes to zero they are very close to zero.

Whereas gate to bulk, you will always have a charge, depletion charge is always there and therefore that will result into a C_{gb} of approximately W into C_{ox}, right this is what you get when you get C_{GB} right and this is what you get when you have cut-off region. So, when you have cut off region, you do have this C_{gd} and C_{gs} is equals to 0 and C_{gb} is equals to W into L width into length of the transistor multiplied by oxide capacitance per unit area.

What happens the next subsequent leaves the triode region? You have that C_{gs} and C_{gd} is half of WL into C_{ox}, which means that this is quite interesting and there is a debatable topic but in reality it is a safe assumption that whatever oxide capacitance you are having the can be divided into two parts source and drain.

In the being the triode region please understand your drain voltage is very, very low, source is already grounded, so the amount of charge deposited at source and drain will be almost equal to each other and therefore what we say it is half WL into C_{ox}. In the saturation region whereas C_{gd} equals to 0, let us see why is it equal to 0. In the saturation region remember (what is the) what was the concept of saturation region?

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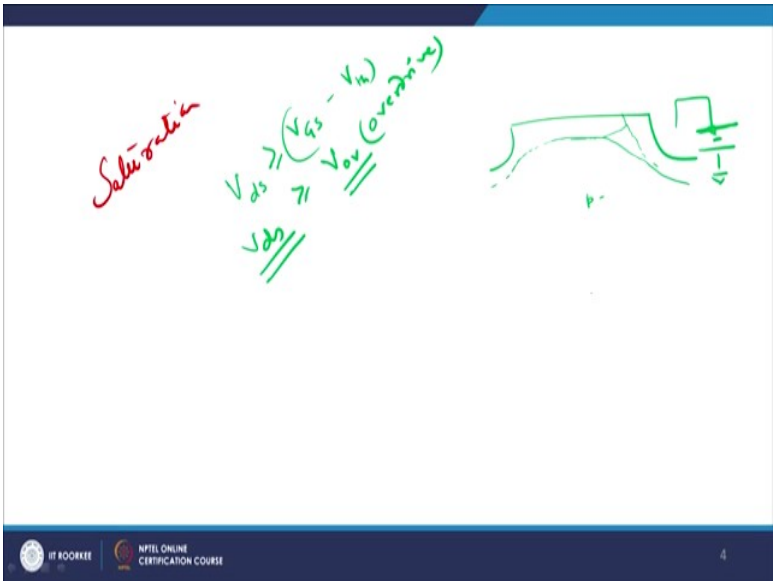

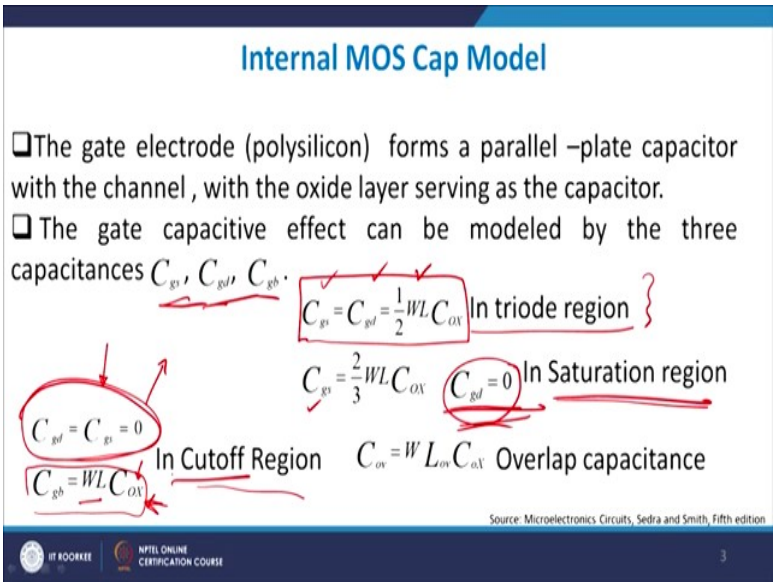

The saturation region, if you remember saturation region if you point out, right in the saturation region always V_{ds}, right V_{ds} sorry I will just come back to you V_{ds} is greater than equals to V_{gs} minus V_{th}, this is the condition for saturation which means that the V_{ds} should be at least greater up this is also referred to as V overdrive, right. So, my drain to source voltage should always be larger than the overdrive voltage, fine.

Which means that, the my V_{ds} should be typically very large but understand unlike in the previous case in this case drain in always sorry, it not grounded but I give a positive bias which means that if this is an n channel MOSFET then then this is this is p type and then if this is source, I will have a depletion region is something like this initially, right you go on

increasing the depletion region and what will happen is that depletion region will eat away into so this depletion region it away into the channel.

So, there will be no channel formation here, so there will be no charge, no charge primarily means you that C_{gd} is exactly equals to 0, that is what I am trying to say you here but C_{gd} is equals to 0 in saturation, right. And C_{gs} is 2 by 3 W L C oxides, you will ask you whether the one third C oxide goes? Well, that is a debatable topic but typically bulk takes the maximum value of the of the one third of your W by L, C oxide.

Which means that under saturation triode and cut-off region you do have the change in your overall capacitance? So, even if your bias you and you and you let the bias point move from saturation to cut off and vice versa then you will see the capacitors will go on bearing, right. In the triode region, what we see? We get C_{gs} equals to C_{gd} equals to 1 by 2 half W L oxide and then C_{gs} equals to 2 by 3 W L C oxide into C oxide where C_{gd} equals to 0 for this thing. In cut-off region, both my C_{gd} and C_{gs} are equals to 0 and all of the oxide is going to gate to bulk region for operation, fine.

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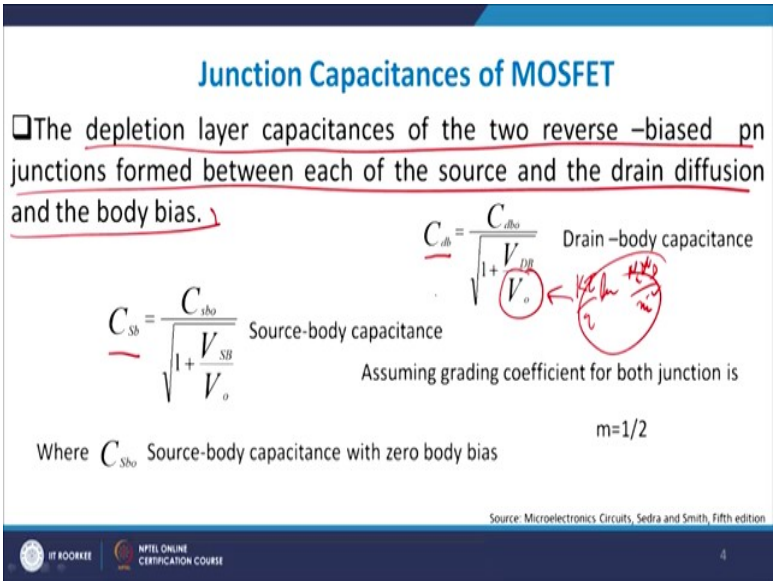

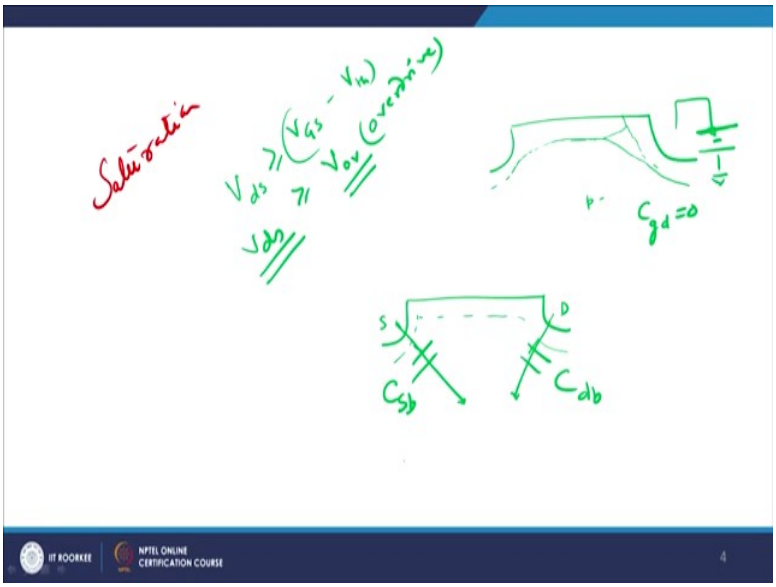

This is the basic model of a MOS capacitor. The third or the fourth type of junction capacitance which you feel is basically, please remember as I was discussing with you just now that your source and drain region, right remember is always sort of a reversed biased at least the drain region is reversed bias which means that there will be always a depletion capacitance at this particular point, right.

So, the depletion layer capacitance is of the two reversed bias pn Junction formed between each of the source and the drain diffusion of the body bias is defined as my C_{db} or drain to bulk. So, I have C_{sb} and C_{db}, C_{db} is drain to bulk and this is source to bulk, right. If you go back it is drain to bulk and then source to bulk, so we will have one capacitance here 1 capacitance, so this is C_{db}, this is C_{sb} and this will be primarily a junction capacitance which will depend upon the drain diffusion and the source diffusion. So, C_{db} is given as C_{dbo}, C_{dbo} upon 1 plus V_{db} by V_0, V_0 is basically your applied.

So, let me see C_{dbo} is the 0 bias drain to bulk, so (when he did not) when you do not apply any bias of the drain side you still will have a depletion capacitance between this drain and the bulk, right even when you do not apply any external bias there, right it will be still 0 when it is still 0 you will see that C_{db} will be equal to C_{dbo} upon V_{db}.

So, C_{dbo} is the 0 bias drain to bulk capacitance, V_{db} is the (drain to bulk capa) drain to bulk voltage which you are giving which you see and V_0 is basically the built in voltage which you see, this is a bit built-in voltage depending upon the this thing. So, it is basically K T by q is K T by q by ln of N_a, N_i, N_d upon N_i square this is what is equals to V_0.

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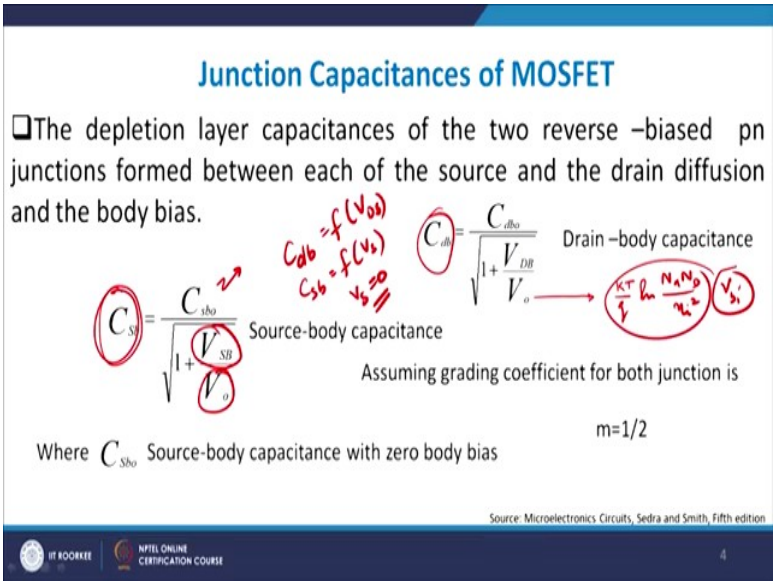

So, V_0 is basically as I discussed with you just now, V_0 is the built in voltage it is K T by q ln of N_a, N_d upon N_a square and this is basically a built in voltage and this is the minimum voltage which you need to overcome. Similarly, when you do source to bulk it is sb zero, it is a zero bias source to bulk capacitance V_{SB} is the applied source to bulk voltage right and V_0 is the built in voltage which is there with us.

So, your C_{db} and C_{sb}, please understand the values of C_{sb} and C_{db} depend upon the value of course the reverse bias which we do. Typically, source will be grounded, so this C_{sb} is almost fixed, you know they do not vary with bias but C_{db} varies with the bias because your drain to bulk will always vary right unlike, so C_{db} is a function of your drain voltage, V_{DS} whereas C_{sb} is also a function of V_s.

So, this V_D and V_S but since my V_S is equals to 0 the value of V_{sb} is almost fixed when you talk about junction capacitances, right. So, we are understood overlap capacitances and diffusion capacitances, we also learned about depletion capacitance is also known as junction capacitances and we saw that as you vary the biases the capacitance value also varies in in these particular cases. Let me now, therefore come to the high frequency model of a MOSFET and that is pretty interesting or important.

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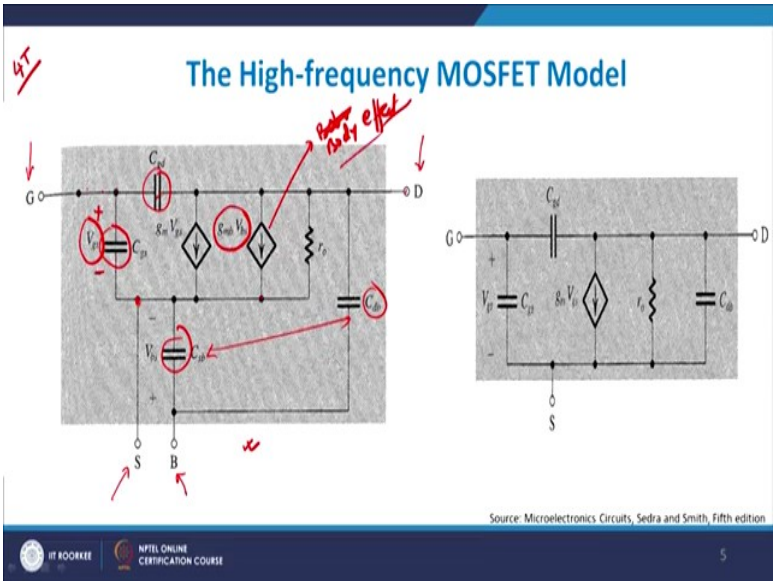

So, now if you look very carefully look at the left hand figure here, again as I discussed with you, you have got four terminals gate, you have drain right, you have got source and you have got bulk. So, it is basically behaviour it is basically a four terminal device behaviour right out of which if you look very carefully as I discussed with you gate to sources, so when you apply your gate to source voltage you apply between gate and source, so this is your V_{gs} where this is positive and this is not.

So, this is my source point, so the difference between this and this is by V_{gs} and therefore the capacitance C_{gs} appears between gate and source. Similarly, C_{gd} appears between gate and drain and C_{sb} is between source and bulk and C_{db} is between drain and bulk, so these two are actually your depletion capacitances and these two are actually your diffusion capacitance which is visible to you.

So, therefore if this this g_m times V_{gs} is nothing but the device itself, the channel current because g_m is transconductance is $\partial i \, \partial V_{gs}$, so when you multiply with V_{gs} I get the current. So, therefore I am showing it by the ideal current source here and it is basically $g_m V_{gs}$ and as you can see it is between drain and source, this is my source and this is your drain, so this is a drain and source.

This is also a current which is virtually between drain and source known as the bulk $g_{mb} V_{bs}$, this is because of the body effect, sorry body effect, right. At the body effect why? Because you always have a g_m. So, apart from g_m, so assume that you do not have any body effect then this you will not have this this current source. So, under so but if you have a body effect

by virtue of the fact that threshold voltage and therefore there is an excess current flowing. You have g_{mb} times V_m why this is true? I will just give you a small brief idea why this is true it is something like this.

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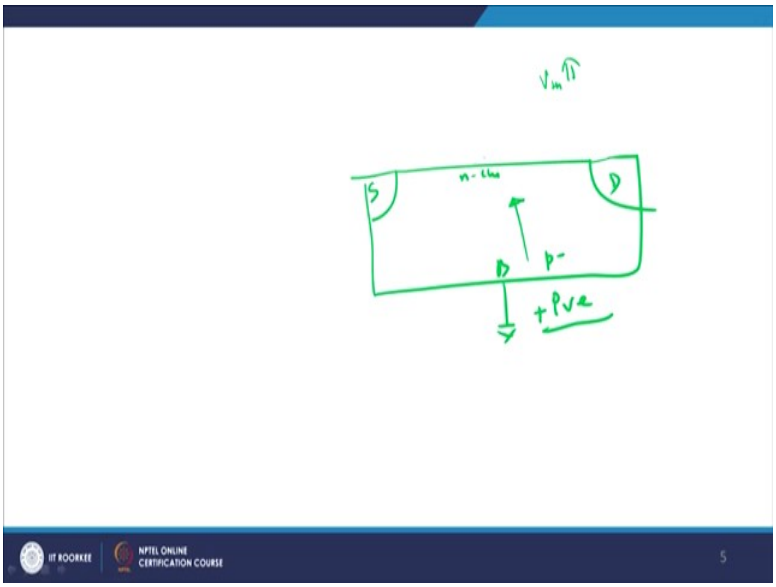

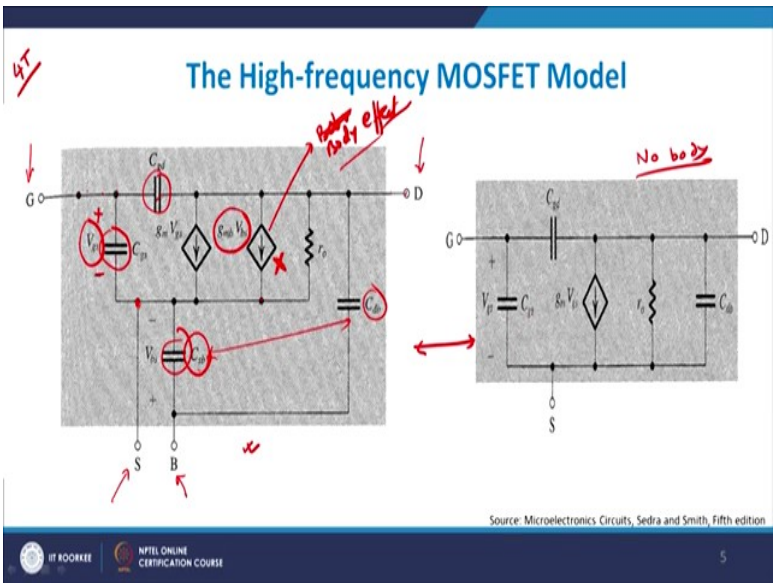

So, if you remember in our previous discussion when we are doing if this is my bulk and this is my source, right and this is my bulk and drain, if I vary the bulk potential and this was initially p type you want it to be n channel, n channel this is in channel, so this is p type and then you apply suppose let us suppose a positive bias on the bulk. It primarily means that it will push the holes towards the side and therefore you do not aid your channel and therefore your threshold voltage will actually rise because you require therefore a larger gate voltage to pull electrons near the surface, right.

As a result, what will happen is for the same amount of gate voltages earlier your current will fall down, right that is what is known as g_{mb} a V_{BS}, right. So, that current which is there between source and drain by virtue of the fourth terminal base current fourth terminal is basically referred to as $g_{mb} V_{BS}$, right. So, this is the current on the fourth because of the fourth terminal.

So, this is what you get as a fourth terminal r_o, as I discussed with your previous term r_o is but the due to channel length modulation effect the resistance offered is known as r_o, right. So, this is basically the high frequency model of a MOSFET, this has been if you look at the right hand side, this one has been done with everything else remaining the same but I have removed C_{sb} because as I discussed with you C_{sb} does not vary with bias, so let me remove it makes my life easier and I have C_{db} only here, i have also removed $g_{mb} V_{BS}$ here.

So, there is no body, so no body effect so there is no body effect on the right hand side and this is what you get finally from your from your this thing from the from the understanding purposes. So, with this let me give you a brief idea about, let me see how I can work out that I do have.

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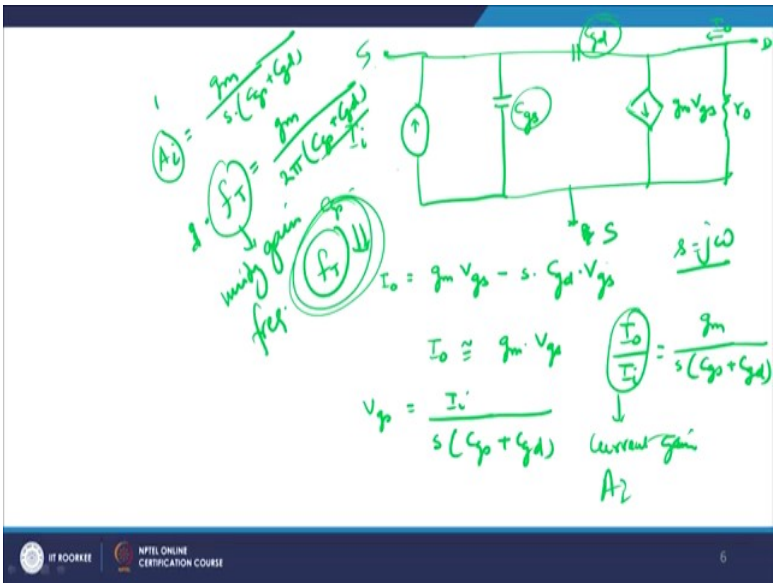

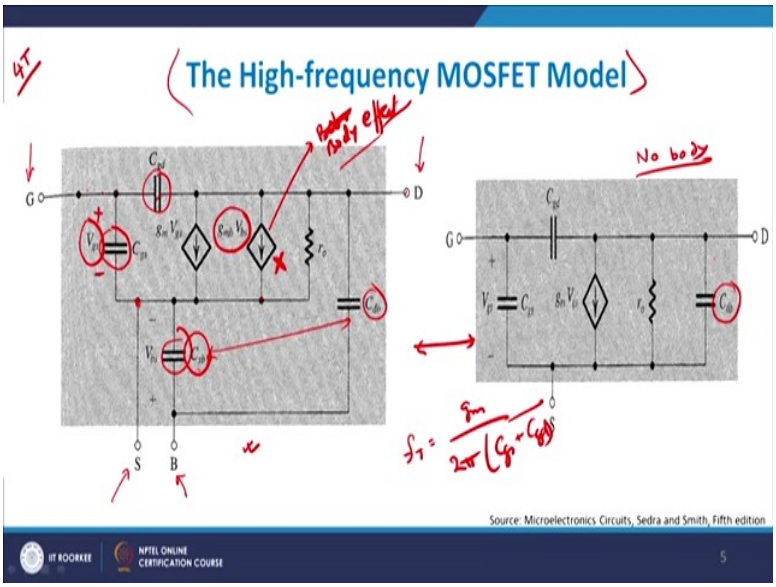

Let me say, I have a high frequency model and I have a current source here I_i and then I have V_{gs} and C_{gs} being available to us, so this is C_{gs}, right I have C_{gd} here, C_{gd} right and then you have the current source which is basically your $g_m V_{gs}$ here and then you have r_o, right and then this goes to bulk and this is your grounded, let us suppose bulk is grounded and this is your drain and this is your, so this is the C_{gs}.

So, this is a gate and source available here, right or let us suppose this is not bulk, it is supposed this is a source and therefore this is gate here and then C_{gd} gate to source, to gate to source, gate to drain you have got r_0 and this is your current source here. So, if you current is I_0 is flowing a typical two port Network, current is assumed to be flowing inside the device, so what I say? Whether I can right down is I_0 equals to g_m times V_{gs} minus s times C_{gd} multiplied by $V_{gs,}$ right.

If we look from this side it is g_m times V_{gs} current and then C_{gd} multiplied by V_{gs} into s is this current, I_0 is therefore relatively equals to g_m times V_{gs}, this is a very simple straight forward so I can write down V_{gs} to be equals to I_i upon s times C_{gs} Plus C_{gd}. So, I can write down I_0 by I_i the ratio of output current which is basically the current gain to be equals to g_m upon s times C_{gs} Plus C_{gd}, right where s equals two therefore s is basically equals to jw.

So, I get this is basically my current gain, current gain which is also referred to as A I, so I can refer to as A I therefore A I is equal to g_m upon s times $C_{gs} + C_{gd}$. Now, A I if so let us suppose I want a unity current gain, right so A I will be equals to 1 right and therefore I can safely write down to, so s if I take this if (s equals to) A I equals to 1 I take s equals to this

side and now then replace s by (2) w by 2 π F then I get f_T is equals to g_m by 2 π C_{gs} plus C_{gd}, this is referred to as unity gain frequency.

What is the meaning of unity gain frequency? It tells me that, that frequency at which the ratio of output current to input current will be approximately equals to 1 will be referred to as a unity gain frequency and it depends upon the transconductance and it also depends upon the value of C_{gs} in C_{gd}. So, you see if you increase the value of C_{gs} and C_{gd} your f_T actually starts to drop down.

So, you cannot operate at very high frequencies, right you if you want the unit again device for whatever reasons for example for matching your impedances and you want a unity gain device then if your gate to source of gate to drain capacitances becomes large then you end up having a lower f_T which means that you operate at a lower f_T or a lower frequency domain, right.

So, that is quite it and that is what I was saying that capacitance model tends to change your frequency of operation drastically that is what I wanted to just remind you in from this observations or from this basic idea, right. So, with this we come to the high frequency model once again and we saw this thing and we just now saw that my f_T will be equal to g_m upon $2\pi C_{gs}$ plus C_{gd}, right and you see the depletion capacitance which is C_{db} does not play a role as far as unity gain is concerned, right. It is only the gate to source and gate to drain capacitances which play a play important role that is what I was coming to therefore.

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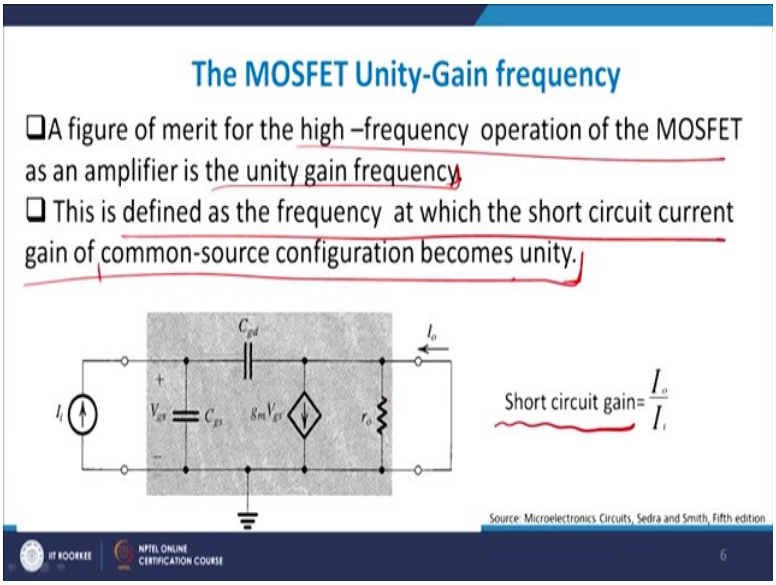

Therefore, one of the figure of merit for the high frequency operation of the MOSFET is the unity gain frequency. So, this is defined as the frequency at which the short circuit current gain of a common source configuration becomes unity right. So, whenever you short circuit gain means? We the output is basically shorted, so and therefore the current I_o is flowing by virtue of this MOS device.

So, by short circuit current is grounded and therefore in a common source configuration I_0 by I_i, I_0 is the output current, I_i is the input current if you divide then that we define that to be the short circuit gain and we just now saw this to be equals to this whatever depending on the transconductance of the device as well.

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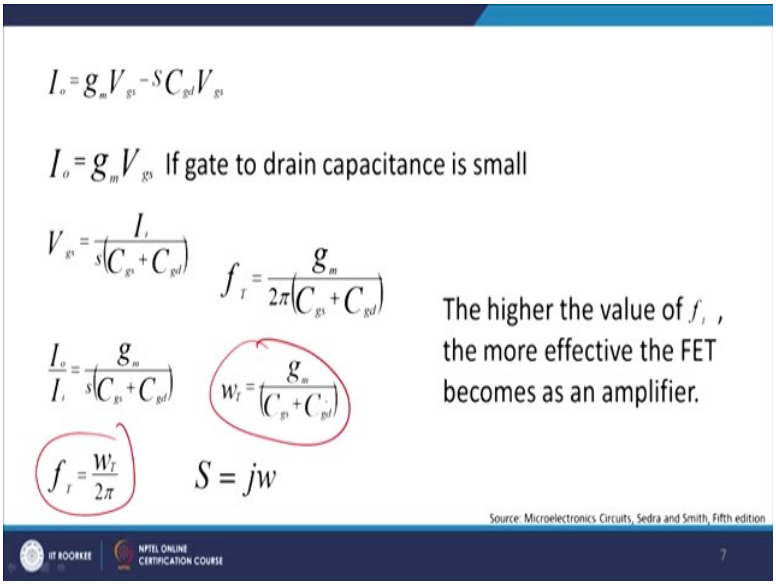

So, this is basically your MOSFET unity gain amplifier as such. As you see therefore, I have already derived this where this value and as I discussed with you f_T if you look and therefore w T if you find out is g_m by this thing, so f will because 2 g_m by 2 π C_{gs} plus C_{gd}. So, I will not go into details we have already discussed this point in details for this case. So, it becomes a much better amplifier right it becomes a much better amplifier as such in this case, ok.

Let me come to the frequency response of the common source amplifier, right. It quite an interesting study, frequency response primarily meaning means that if you are able to plot the variation of gain on the y axis.

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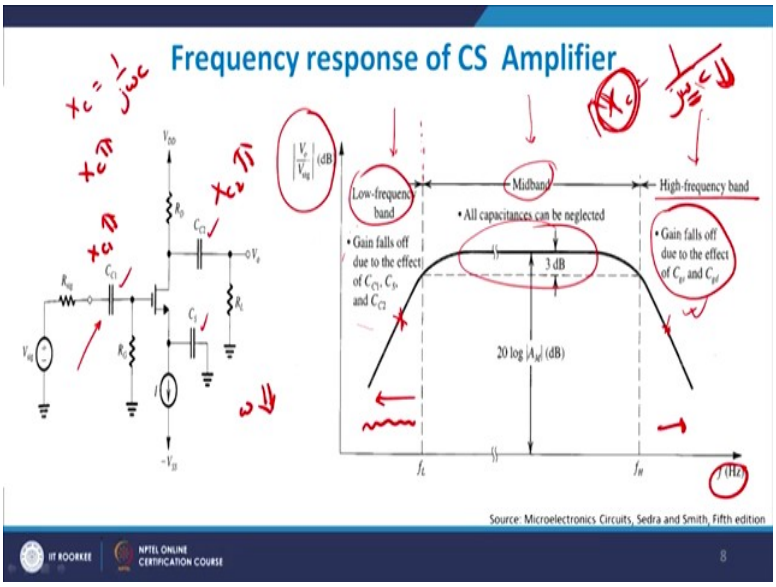

So, you have gain on the y-axis, so V_0 by V_{sig} is my gain, V_{out} by V_{sig} is my gain and then the x axis, you have do have the frequency then we define this to be as a frequency response, right. We generally divide the frequency response into three major component, one is the low frequency band which is therefore below a particular set of frequencies we define this to be the low frequency band, anything above a particular frequency is defined as high frequency band and somewhere in the middle we define this to be as the mid band.

So, typically we have three components or three frequency components of a common source amplifier, the first is basically the low frequency band, the second is high frequency band, third one is a mid-band, right. It has been seen for almost all the amplifiers that the mid band frequencies is almost constant independent of the frequency applied right, so you have a large range of frequencies across which you would expect to see almost constant values of a gain

right and typically if you operate under such a criteria or certain conditions here then your gain will be independent of frequency.

So, you vary frequency as much as you want and your gain is stable and gives you a stabilized gain but if you some or other fall in this region or in this region then you again becomes a becomes a function of your frequency, right. So you vary a frequency or gain varies very highly nonlinear approach to your design, right. Let us see what happens and why this happens? You see I had discussed with you that X_c is equals to 1 by j w c right, fine.

So, you see once you go to the low frequency domain somewhere here your w are relatively small, right, when your w are relatively small your X_c are relatively very, very large so X_{c1} is very high, similarly, X_{c2} is also very high and so on and so forth. So, when these are very high this start behaving as a open circuit right, because the impedances are very high in this case.

So, if you concentrate only forget about everything else even and concentrate only on a C_{c1} which is basically the coupling capacitor you know why, we had referred to this as coupling capacitor or a blocking capacitor? The reason being that I do not want any DC bias of V_{sig} to appear on to the gate side of my MOS device, right that was my main aim and that is the reason you are putting a coupling capacitance here.

Once you put that a coupling capacitor then at lower frequencies of w the resistance offered by the C_{c1} is typically very high and therefore most of the V_{sig} does not appear on the gate side of the MOS device and therefore again starts to fall down, right. So, it is X_{c1} starts to behave like a more and more like an open circuit and as a result the gain starts to fall down as you lower your frequency from a particular value and that is the that is what is written here that the gain falls out due to the effect of C_{c1}, C_{c2} and C_s.

So, I have this, this and this all starts to behave like an open circuit whereas at very high frequencies your depletion capacitances they become almost very, very large at very high frequencies, so and therefore as the frequency increases those values become large and as a result the gain starts to fall down, right. As you can see therefore that at very high frequencies at relatively high frequencies X_c again as I discussed with you will be 1 upon j w c.

Now, at very high frequencies this is very high agreed therefore X_c has to be low but your C becomes so small your C_{gs} and C_{gd}, gate to source and gate to drain it becomes so small that this X_c capacitance is almost negligibly, negligibly large right or it becomes very large. So, w

is very small C drops down X_c becomes very, very large and as a results as the gain starts to fall down at high frequency regions, right.

So, I just started with this thing, maybe in the next interactions we will carry forward with where we left today and give you a basic idea about the frequency response of amplifier what. We learnt today? we learned about the high frequency modelling of a MOS device, of a MOS amplifier, we also learnt how to design or how to predict a unity gain, unity gain current gain of amplifier on what factors does it depend.

We finally ended up, looking into the frequency response of a common source amplifier and we saw that mid band is the place where you should bias your device, so that it is independent frequency, at higher and lower frequencies the gain will fall down with respect to frequency. So, when the frequency increases or decreases your gain will fall down typically in high band, high frequency band and low frequency band respectively, right. So, with this let me stop here today and then when we meet next time we will start forward we will move forward ahead of this, is it ok, thank you very much!!